CoreadDvices
承芯微电子

CD08AD1500

High Performance, Low Power, 8-Bit, 1.5 GSPS A/D Converter

Version: Rev 1.0.0 Date: 2025-5-20

Features

- Dual channel ultra-high speed A/D converter
- Resolution 8 Bits
- Single+1.9V±0.1V Operation
- Inter leave Mode for 2x Sample Rate
- Multiple ADC Synchronization
- Duty Cycle Corrected Sample Clock
- Max Conversion Rate 1.5GSPS(min)
- DNL：±0.4LSB
- Serial Interface for Extended Control
- 4-bit address, 16 bit data
- Input full scale range digital

Application

- Digital oscilloscopes
- Communication receiver
- Direct RF down converter
- High speed digital acquisition
- Radar and electronic countermeasure

Description

The product features high sampling rate, low power consumption, small linear error Automatic gain and offset correction and 3-wire interface control.Gain, offset and connection of internal circuit can be realized through 3-wire interface The clock matching between channels is used for correction, and the analog input is differential input,Either AC coupling or DC coupling; Clock input circuit internal With DC offset, AC coupling input is required.

This product is compatible with foreign National Semiconductor companies The ADC08D1500 pins of the company's products are arranged in the same way, with the same function and performance It can directly replace ADC08D1500.

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Functional Block Diagram

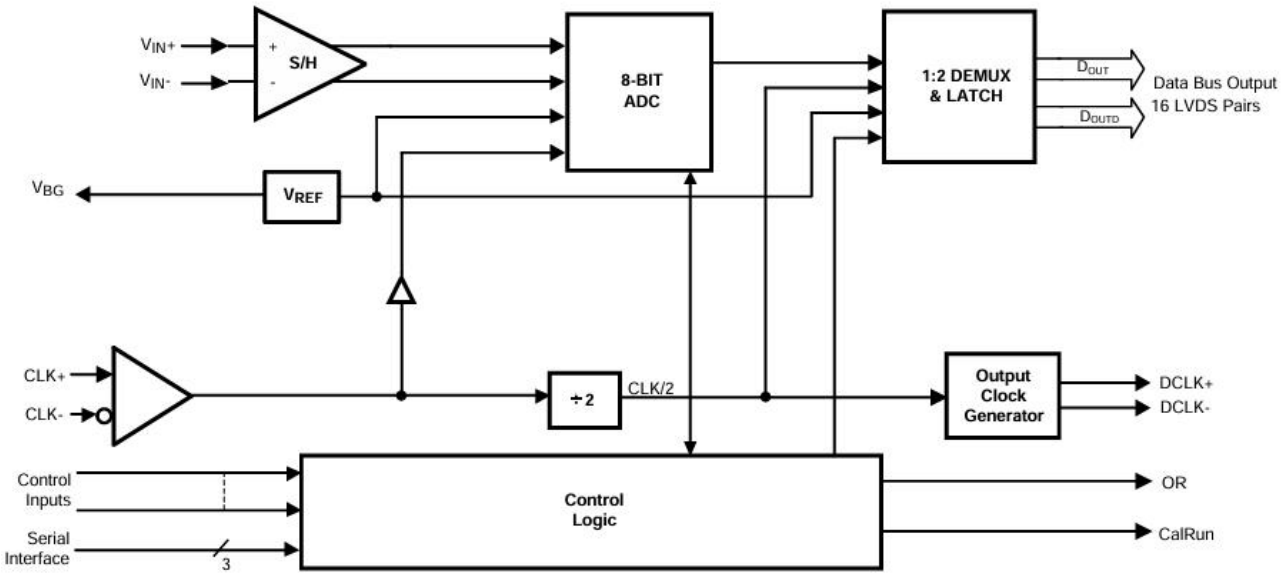
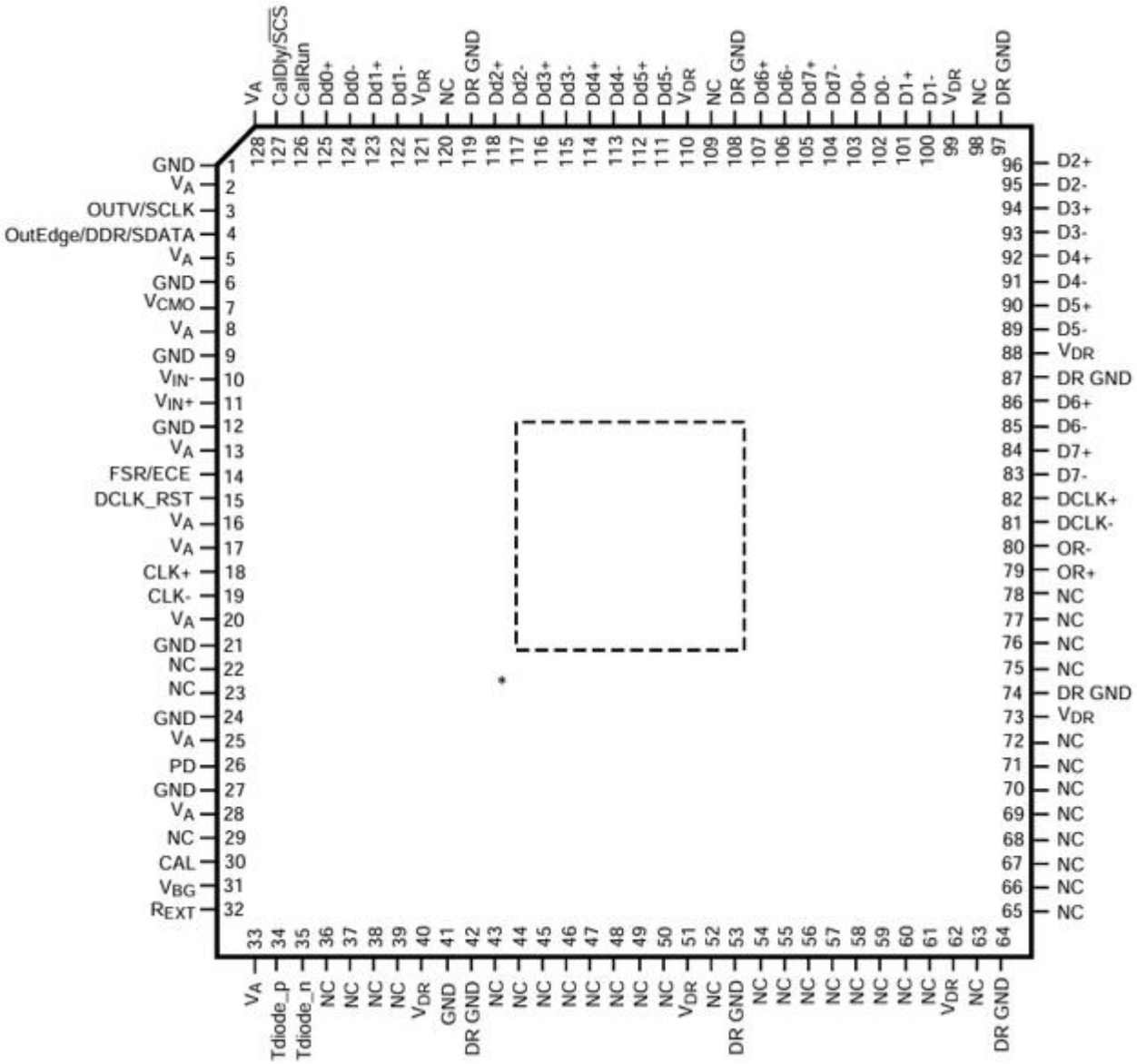


Figure 1. Functional block diagram

Pin Configurations



Pin Configuration

Pin Number	Symbol	Pin Description	Pin Number	Symbol	Pin Description
1	GND_D	Analog ground	65	D_{Q2}	Q channel data output bit D_{Q2}
2	V_{CC}	Analog Supply	66	D_{Q2}	Q channel data output bit DQ2
3	Outv/SCLK	Output voltage amplitude control/serial interface clock input	67	D_{Q3}	Q channel data output bit D_{Q3}

4	OutEdge/ DDR/DATA	Output clock edge selection/dual data rate control/serial data input	68	D_{Q3}	Q channel data output bit D_{Q3}
5	V_{CC}	Analog Supply	69	D_{Q4}	Q channel data output bit D_{Q4}
6	GND_A	Analog ground	70	D_{Q4}	Q channel data output bit D_{Q4}
7	V_{CMO}	Common mode voltage	71	D_{Q5}	Q channel data output bit D_{Q5}
8	V_{CC}	Analog Supply	72	D_{Q5}	Q channel data output bit D_{Q5}
9	GND_A	Analog ground	73	V_{DD}	Output drive power
10	IN_{I-}	I channel analog input negative	74	GND_D	Output drive ground
11	IN_{I+}	I channel analog input positive	75	D_{Q6}	Q channel data output bit D_{Q6}
12	GND_A	Analog ground	76	D_{Q6}	Q channel data output bit D_{Q6}
13	V_{CC}	Analog Supply	77	D_{Q7}	Q channel data output bit D_{Q7} (Highest bits)
14	FSR/ST1	Full scale range selection/extended control mode selection	78	D_{Q7}	Q channel data output bit D_{Q7} (Highest bits)
15	R	Clock set control input	79	DOR	Overflow in-phase output
16	V_{CC}	Analog Supply	80	DOR	Overflow inverted output
17	V_{CC}	Analog Supply	81	QCLK	Data clock inverted output
18	INCLK+	Clock input positive	82	QCLK	Data clock in-phase output
19	INCLK-	Clock input negative	83	DI7	I channel data output bit D_{I7} (Highest bits)

20	V_{CC}	Analog Supply	84	DI7	I channel data output bit D_{I7} (Highest bits)
21	GND_A	Analog ground	85	DI6	I channel data output bit D_{I6}
22	IN_{Q+}	Q channel analog input positive	86	DI6	I channel data output bit D_{I6}
23	IN_{Q-}	Q channel analog input negative	87	GND_D	Output drive ground
24	GND_A	Analog ground	88	VDD	Output drive power
25	V_{CC}	Analog Supply	89	DI5	I channel data output bit D_{I5}
26	PD	Power saving mode control	90	DI5	I channel data output bit D_{I5}
27	GND_A	Analog ground	91	DI4	I channel data output bit D_{I4}
28	V_{CC}	Analog Supply	92	DI4	I channel data output bit D_{I4}
29	PDQ	Q channel Power saving mode control	93	DI3	I channel data output bit D_{I3}
30	CAL	Correction control	94	DI3	I channel data output bit D_{I3}
31	VREF	Reference output	95	DI2	I channel data output bit D_{I2}
32	Rext	External resistance	96	DI2	I channel data output bit D_{I2}
33	V_{CC}	Analog Supply	97	GND_D	Output drive ground
34	Tdiode_p	Temperature diode positive	98	NC	Not connect
35	Tdiode_n	Temperature diode negative	99	VDD	Output drive power
36	DQd0	Q channel data output bit D_{QD0} (Lowest bits)	100	DI1	I channel data output bit D_{I1}
37	DQd0	Q channel data output bit D_{QD0} (Lowest bits)	101	DI1	I channel data output bit D_{I1}
38	DQd1	Q channel data output bit D_{QD1}	102	DI0	I channel data output bit D_{I0} (Lowest bits)
39	DQd1	Q channel data output bit D_{QD1}	103	DI0	I channel data output bit D_{I0}

					(Lowest bits)
40	VDD	Output drive power	104	DID7	I channel data output bit D_{ID7} (Highest bits)
41	GND_A	Analog ground	105	DID7	I channel data output bit D_{ID7} (Highest bits)
42	GND_D	Output drive ground	106	DID6	I channel data output bit D_{ID6}
43	DQd2	Q channel data output bit D_{QD2}	107	DID6	I channel data output bit D_{ID6}
44	DQd2	Q channel data output bit D_{QD2}	108	GND_D	Output drive ground
45	DQd3	Q channel data output bit D_{QD3}	109	NC	Not connect
46	DQd3	Q channel data output bit D_{QD3}	110	VDD	Output drive power
47	DQd4	Q channel data output bit D_{QD4}	111	DID5	I channel data output bit D_{ID5}
48	DQd4	Q channel data output bit D_{QD4}	112	DID5	I channel data output bit D_{ID5}
49	DQd5	Q channel data output bit D_{QD5}	113	DID4	I channel data output bit D_{ID4}
50	DQd5	Q channel data output bit D_{QD5}	114	DID4	I channel data output bit D_{ID4}
51	VDD	Output drive power	115	DID3	I channel data output bit D_{ID3}
52	NC	Not connect	116	DID3	I channel data output bit D_{ID3}
53	GND_D	Output drive ground	117	DID2	I channel data output bit D_{ID2}
54	DQd6	Q channel data output bit D_{QD6}	118	DID2	I channel data output bit D_{ID2}
55	DQd6	Q channel data output bit D_{QD6}	119	GND_D	Output drive ground
56	DQd7	Q channel data output bit D_{QD7} (Highest bits)	120	NC	Not connect
57	DQd7	Q channel data output bit D_{QD7} (Highest bits)	121	VDD	Output drive power
58	DQ0	Q channel data output bit D_{QD0} (Lowest bits)	122	DID1	I channel data output bit D_{ID1}

59	DQ0	Q channel data output bit D_{QD0} (Lowest bits)	123	DID1	I channel data output bit D_{ID1}
60	DQ1	Q channel data output bit D_{I1}	124	DID0	I channel data output bit D_{ID0}
61	DQ1	Q channel data output bit D_{I1}	125	DID0	I channel data output bit D_{ID0}
62	VDD	Output drive power	126	QCAL	Correction operation indication output
63	NC	Not connect	127	CalDly /DES /ST2	Power on correction delay selection/double edge sampling control/serial interface strobe
64	GND_D	Output drive ground	128	V_{CC}	Analog Supply

Timing Diagram

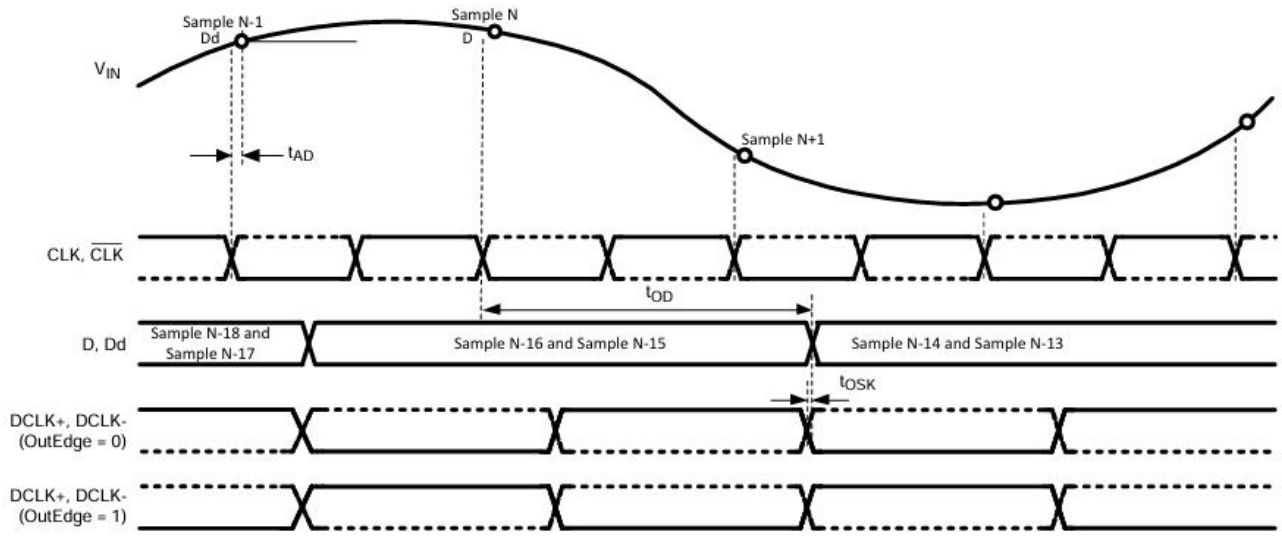


Figure 2. CD08AD1500 single data rate (SDR) timing (OutEdge is high or low)

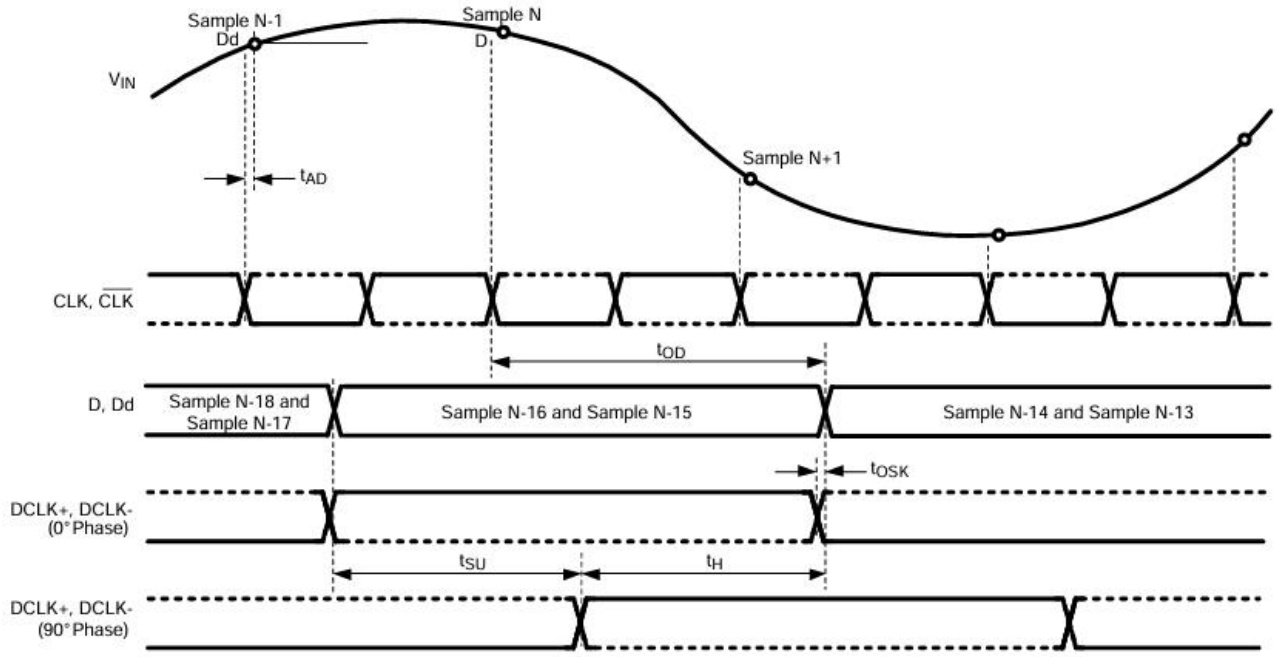


Figure 3.CD08AD1500 Double Data Rate (DDR) timing (OutEdge hanging or VCC/2)

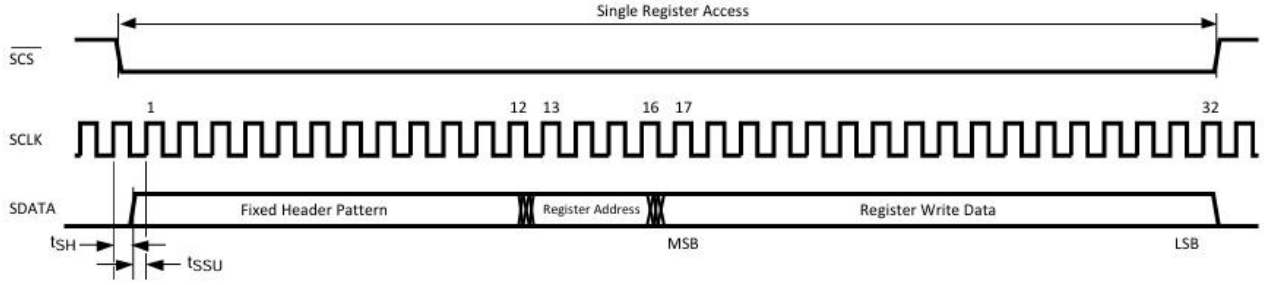


Figure 4.Serial interface timing

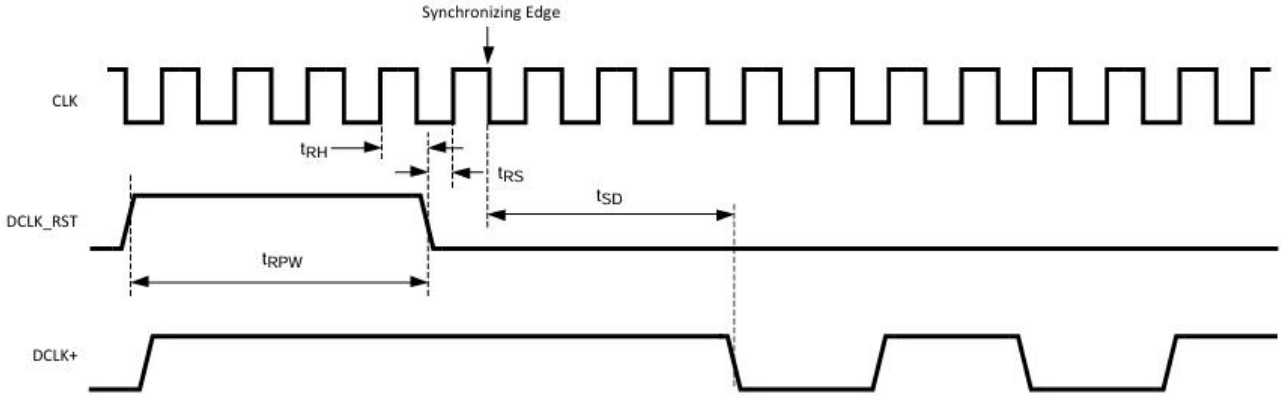


Figure 5.Clock reset timing in DDR mode when OutEdge is suspended or VCC/2

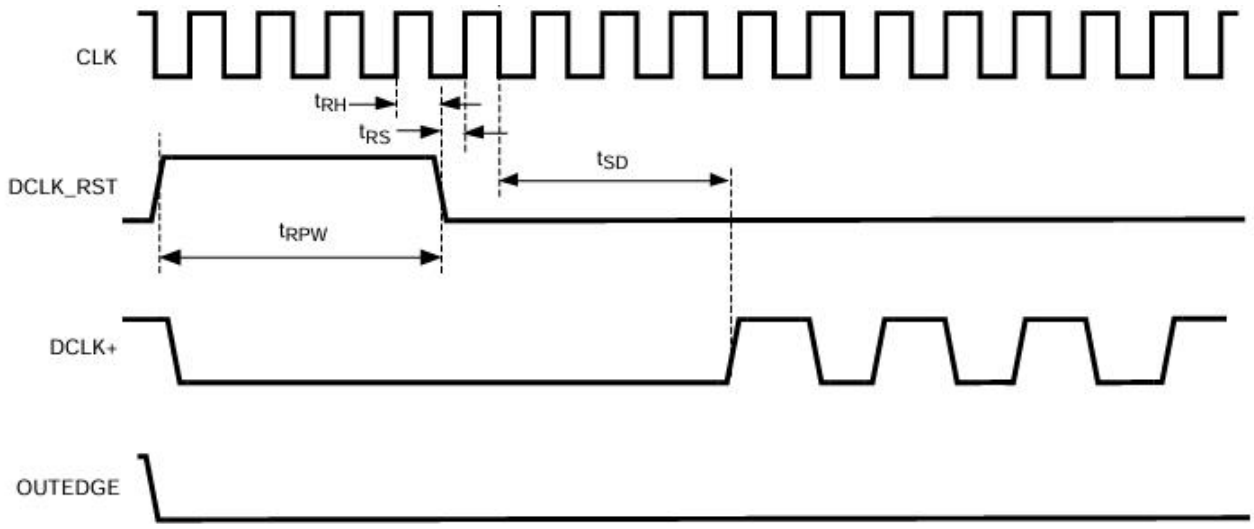


Figure 6.When OutEdge is low, the clock reset timing of SDR mode

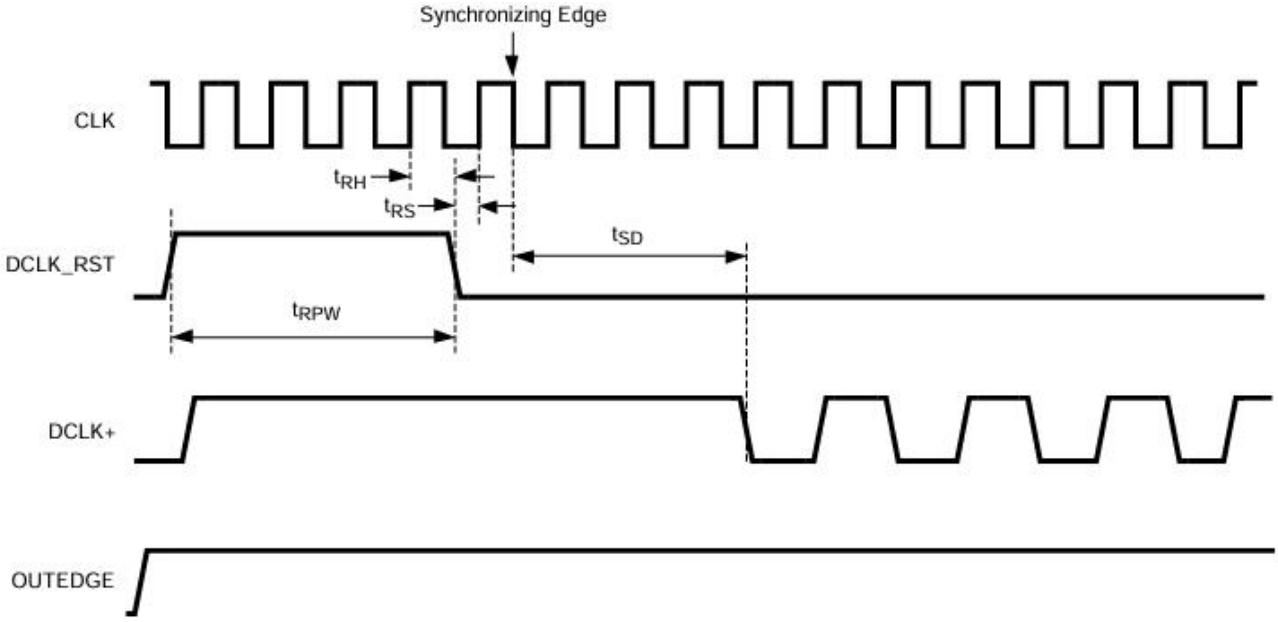


Figure 7.When OutEdge is high, the clock in SDR mode resets the timing

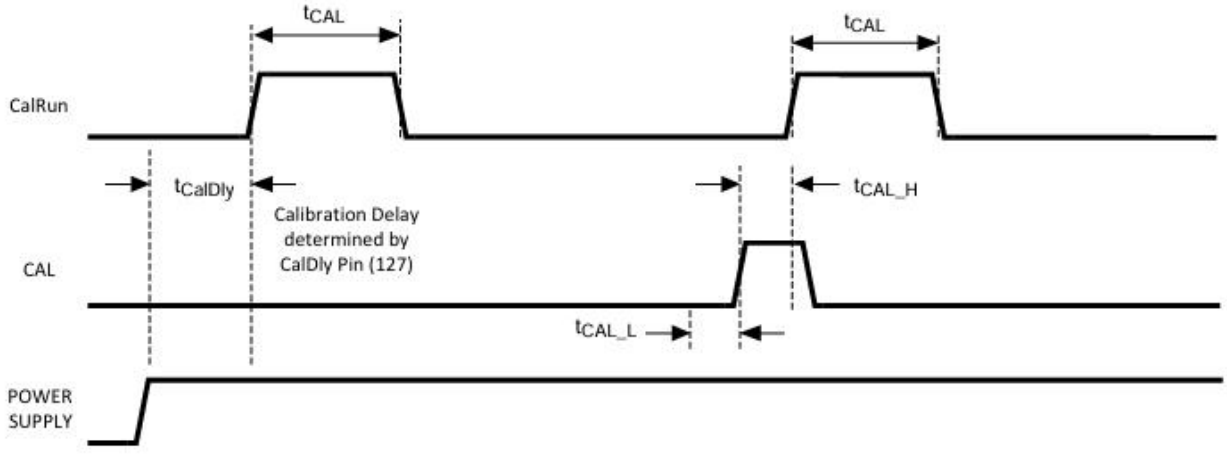


Figure 8.Self correction and instruction correction timing

Outcode

Table 1. Output Code (Standard mode, FSR high)

Equivalent decimal	VIN+—VIN-	Voltage level	Binary code	Overflow Bit
255	>460mV	>Positive Fullness Range + 1/2LSB	11111111	1
255	460mV	Positive Fullness Range + 1/2LSB	11111111	0
254	458mV	Positive Fullness Range - 1/2LSB	11111110	0
.	.		.	
.	.		.	
128	1.8mV	Bipolar 0 + 1/2LSB	10000000	0
127	-1.8mV	Bipolar 0 - 1/2LSB	01111111	0
.	.		.	
.	.		.	
1	-458mV	Negative Fullness Range + 1/2LSB	00000001	0
0	-460mV	Negative Fullness Range - 1/2LSB	00000000	0
0	< -460mV	< Negative Fullness Range + 1/2LSB	00000000	1

Recommended Operation Conditions

- Power supply voltage (V_{CC}, V_{DD}): 1.8V-2.0V
- Analog input common mode voltage: 1.26V +50mV
- Differential analog input range: 570-1100 mVpp
- Serial interface clock input frequency: 100MHz
- Clock frequency range: 200 MHz ~ 1500MHz
- Clock input duty cycle: 20%-80% (Typical 50%)
- Differential clock input amplitude: 0.5-2.0 V_{PP} (Typical 0.6 V_{PP})
- Operating temperature: -45 ~85 C

Absolute Maximum Ratings

- Power supply voltage (V_{CC}, V_{DD}): 2.2V
- V_{DD}-V_{CC}: 0V ~ 100mV
- Input current of any pin: ± 25mA
- ESD protection: human model: 2000V, machine model: 250V
- Welding resistance temperature of lead wire TH (10s): 300 ℃
- Storage temperature T_S: - 65 ℃ ~ 150 ℃
- Junction temperature T_J: 175 ℃

Electrical Characteristics

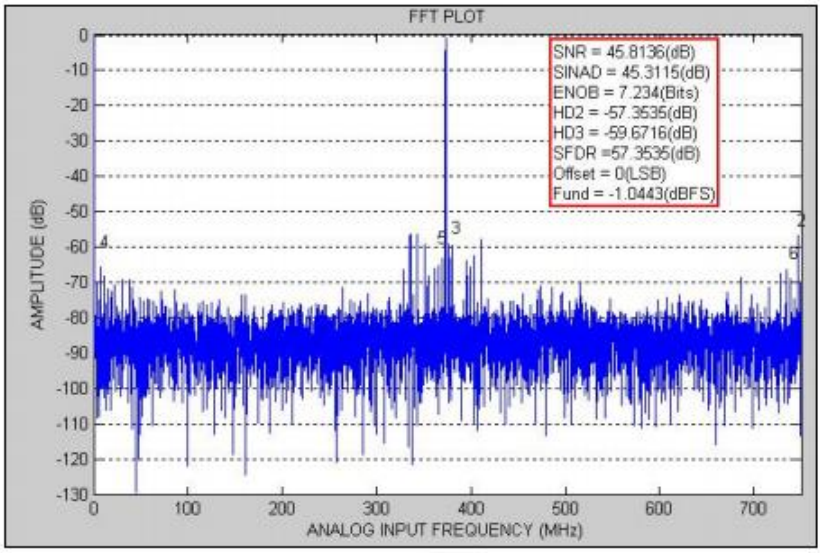
Unless otherwise specified, the electrical characteristics shall comply with Table 2. The electrical test method shall be in accordance with SJ 20961-2006. Analog input AC coupling, differential 920mVpp; Clock AC coupling input, duty cycle 50%; External resistance Rext=3300 Ω± 0.1%. Typical values in Table 3 are only reference data at 25 ℃.

parameter name	symbol	condition	MIN	TYP	MAX	Unit
Resolution	RES		8			bits
Analog supply current	I_{CC}	PD = PDQ = 0V	--	900	930	mA
Digital supply current	I_{DD}	PD = PDQ = 0V	--	220	250	mA
Power consumption	PD	PD = PDQ = 0V	--	2.0	2.2	W
Integral Non-Linearity	E_L	DC Coupled, 1MHz Sine Wave Overranged	-1.2	±0.6	1.2	LSB
Differential Non-Linearity	E_{DL}		-1.0	±0.4	1.0	LSB
Offset Error	E_O		-2.5	-0.45	-2.5	LSB
Positive Full-Scale Error	E_{FS+}		-40	±10	40	mV
Negative Full-Scale Error	E_{FS-}		-40	±10	40	mV
Bandgap Reference Output Voltage	V_{REF}	I_{REF} = ±100μA	1.20	1.27	1.33	V
Analog differential	$V_{ID1(PP)}$	FSR pin 14 is low	570	700	900	mVp-p

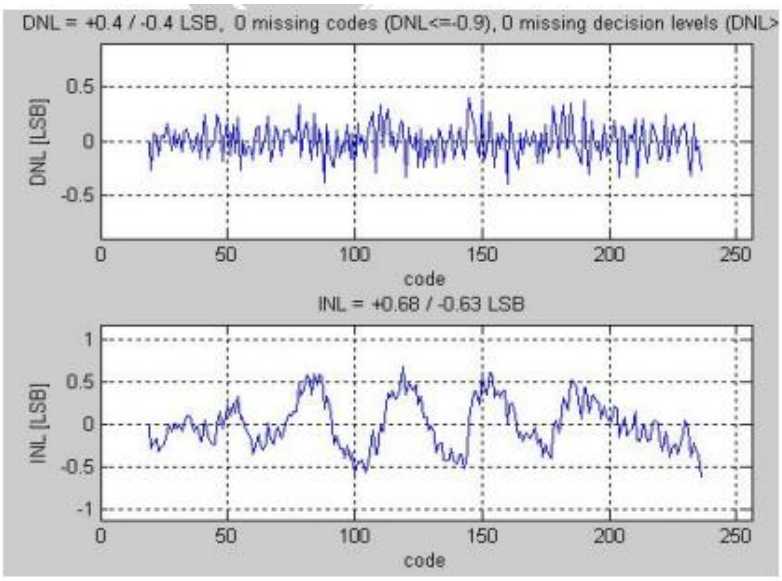
input voltage		FSR pin 14 is high	790	920	1100	mVp-p
Analog differential input resistance	RI		94	100	106	Ω
Clock input differential voltage	$V_{ID2(PP)}$		0.5	0.6	2	V
Logic Low Input Voltage	V_{IL}	Outv，R，PD, PDQ	--		0.3	V
Logic High Input Voltage	V_{IH}		1.6		--	V
Digital output high level	V_{OH}	Q_{Cal} (126 pin)	1.5	1.65	--	V
Digital output low level	V_{OL}		--	0.15	0.3	V
LVDS differential output voltage	$V_{OD\ (PP)}$	OutV= V_{CC}，V_{REF} no connect	400	700	1000	mV
		OutV= GND, V_{REF} no connect	280	500	800	mV
Out of Range Output Code	OROC	(V_{IN+}-V_{IN-}) > +Full Scale	255	--	--	--
		(V_{IN+}-V_{IN-}) < -Full Scale	--	--	0	--
Gain Flatness	ΔA	dc～500MHz	-1	±0.5	1	dBFS
Signal-to-Noise Ratio	SNR	f_{CLK}=1.5GHz, f_{IN}=373MHz	42	45.0	--	dB
Effective Number of Bits	ENOB		6.6	7.2	--	Bits
Signal-to-Noise Plus Distortion Ratio	SINAD	f_{CLK}=1.5GHz, f_{IN}=373MHz	41.5	44.5	--	dB
Spurious-Free dynamic Range	SFDR		45	54	--	dB
Total Harmonic Distortion	THD	f_{CLK}=1.5GHz ， f_{IN}=373MHz	--	--	-45	dB
Maximum conversion rate	S_{Rmax}	f_{IN} = 373MHz	1.5	--	--	GSPS
Output clock duty	Q_{DC}		45	50	55	%

cycle						
Clock setting pulse width	t_{RPW}	See Figure. 5~7 Timing	4	--	--	Clock cycle
Correction control input Low level time	t_{CAL_L}	See Figure. 8 Timing	80	--	--	Clock cycle
Correction control input High level time	t_{CAL_H}	See Figure. 8 Timing	80	--	--	Clock cycle

Main Characteristic of Curves



f_{clk}=1.5GSPS，f_{IN}=373MHz



fclk=1.5GSPS，fIN=373MHz

Application Description

1. Function Description

1) . General

The CD08AD1500 adopts a folding and interpolation structure with correction, which can reach the effective bit of 7.1 bits. The application of folding operational amplifier greatly reduces the number of comparators and power consumption. The interpolation structure reduces the number of pre amplifiers, reduces the load capacitance of the input signal, and further reduces the power consumption. In addition, device integration correction reduces the INL bow caused by folding structure. Through these technologies, a converter with ultra-high speed, high performance and low power consumption is realized.

The analog input signal within the input voltage range of the converter is digitized into 8-bit code value for output, and the conversion rate is 200MSPS ~ 1.5GSPS. Under typical circumstances, the differential input voltage is lower than the negative full scale value, which will

make the output code value all 0; If the differential input voltage is higher than the positive full scale value, the output code value will be all 1. In case of any of the above two conditions, the "I" or "Q" channel will overflow the output range. These single output code values are out of range, which means that the code values output from one channel or two channels are lower than the negative full scale value or higher than the positive full scale value. Both channel converters have a 1:2 multi-channel signal separator that meets the requirements of two LVDS output buses. The data on these output buses is output at the rate of half the sampling rate on each bus. At the same time, the user can select interlaced scanning to achieve the rate output of the sampling rate.

The output amplitude can be normal mode or low amplitude mode. Using low amplitude mode can reduce power consumption but will cause some or all data acquisition, especially in high sampling rate and boundary design systems.

a. Self correction

Power on and user command can start self calibration. Self correction is mainly used to adjust the 100 Ω analog input differential terminal resistance, minimize the full scale error, offset error, DNL and INL, and maximize SNR, THD, SINAD and ENOB. Similarly, the internal bias current is also set through the self correction process. Power on self-tuning and user command startup self-tuning can achieve these purposes. Self calibration is a device function an important component, whose purpose is to make the device achieve better performance. In addition to the power on startup, the self calibration shall be restarted whenever the control of FSR pin (pin 14) changes. To achieve better performance, we recommend that the self-tuning run for 20 seconds

or more after power on and when the device operating temperature is significantly different from the temperature required by the system performance. For more details, refer to 2.4). b. ② command correction. When the device is in power saving mode (PD or PDQ is high), self calibration cannot be initialized or run. For more detailed information, refer to 1.1). g The relationship between power saving mode self-tuning and power saving mode.

In normal operating mode, self calibration will work when the device is powered on and an effective calibration command is input. The correction command keeps the CAL pin (30 pin) low by at least one t_{CAL_L} clock cycle, and then keep the CAL pin high for at least another t_{CAL_H} Clock cycle, where t_{CAL_L} and t_{CAL_H} is defined in the electrical characteristics of the converter, see Figure 8. The time occupied by the self calibration is t_{CAL} defined in the electrical characteristics of the converter. Keeping the CAL pin high after power on will prevent the self-tuning process from running until the CAL pin appears the previously mentioned t_{CAL_L} clock cycle is followed by t_{CAL_H} Clock cycle.

CalDly (pin 127) is used to select one of the two delay times from power on to the start of self-tuning. The self-tuning delay time is set by CalDly pin, which is defined as t_{CalDly} in the electrical characteristics of the converter, as shown in Table 3. The length of these delay times is the time when the power supply voltage is powered on and stabilized to the self-tuning operation. If the PD (pin 26) is high after power on, the self-tuning delay calculator will not work until the PD pin is low again. Therefore, keeping the PD pin high after power on will further delay the start of the self-tuning cycle after power on. The best setting of the CalDly pin depends on the power on setting time of the power supply voltage.

Table 3. Power on delay time control function table (PD is low level)

CalDly (pin 127)	Power on delay selection (t_{CalDly})
H	231 input clock cycles
L	225 input clock cycles
DES (double edge sampling mode)	225 input clock cycles

Precautions for self calibration:

- During the self-tuning cycle, the overflow (QOR) output may be a useful result of the correction algorithm. During calibration, all data output and overflow output data are invalid.
- During power on correction and instruction correction, the clock of internal ADC core and output clock QCLK stop working; At this time, the input terminal resistance is adjusted to Rext/33. The correction of input resistance in the correction period is a part of the correction period in order to reduce noise. Refer to 2.4). b. Self correction. This external resistance is between pin 32 and ground, Rext must be exactly 3.3kΩ ± 0.1%. With this value, the input terminal resistance is adjusted to 100 Ω. Because Rext is also used to set the appropriate bias current for the sample/hold op amp, pre amplifier, and comparator, other Rext values cannot be used.
- As long as the calibration is running, the CalRun output is high whether it is power on self-tuning or user command to start self-tuning.

b. Capture of output data

The data output at the falling edge of clock INCLK+(pin 18), that is, the data output at DI and DQ terminals after 13 input clock cycles and the data output at DId and DQd terminals after 14 input clock cycles are valid. Before the output data is obtained, there is another internal delay called t_{OD}, as shown in the sequence diagram. As long as there is an input clock signal, the CD08AD1500 will perform data conversion. The full differential comparator design, innovative sample and hold

amplifier design, and self-tuning technology have obtained a very flat SINAD/ENOB response below 1.5GHz. The output data signal of CD08AD1500 is LVDS, and the output format is binary offset code.

c. Control mode

The multiple control pins provided realize multiple modes of user control. For example, it includes initialization of correction cycle, power saving mode and full scale range setting control. However, the CD08AD1500 also provides an extended control mode. Through the extended control mode, a serial interface is used to access the control of many advanced characteristics based on registers. This extended control mode cannot be used automatically, and users want to use the normal control mode or extended control mode at all times. When the device is in the extended control mode, many characteristics of pin based control will be replaced by those of register based control, and those pin based controls will be invalid. These pins are Outv (pin 3), OutEdge/DDR (pin 4), FSR (pin 14) and CalDly/DES (pin 127), as shown in Table 4. For more detailed information about the extended control mode, please refer to 1.2) Common/Extended Control Mode.

Table 4. Control Mode

Control input	Functional pin			
FSR/ST (pin14)	Control mode	CalDly/DES/$\overline{ST2}$ (pin 127)	OutEdge/DDR/DATA (pin4)	Outv/SCLK (pin3)
H or L (V_{CC} or GND)	Normal mode	Power on correction delay selection: Delay 2^{31}clock cycles at H; Delay 2^{25}clock cycles at L;	Single data rate mode (SDR): H or L double data rate mode (DDR): suspended or $0.5V_{CC}$	Control LVDS output amplitude: Output normal amplitude at H; Output amplitude decreases at L

		Double edge sampling: suspended or 0.5V_{CC}			
Suspended or V_{CC}/2	Extended mode	Clock and data of strobe extended mode serial interface	H	Serial data input blocked	Serial data input blocked
			L	Serial data input	Serial clock input

d. Analog input

The CD08AD1500 must be driven by a differential input signal, and single ended signal operation is not recommended. When AC coupling input, V_{CMO} (7-pin) is grounded; When DC coupling is input, the V_{CMO} pin is suspended, but the input common mode voltage must be equal to the output voltage of the V_{CMO}. Pin 14 (FSR) provides two full scale range settings. In the normal mode, the FSR setting controls the input full scale range, which is defined by the parameter analog input range in the electrical characteristics of the converter. The full scale range setting is valid for both ADC. In the extended control mode, the input full scale range is adjusted by the data input of the serial interface, which is described in 1.4) and 2.2). See Table 5 for analog input full scale range control.

FSR	Analog differential input full scale range
H	790～1100mVpp，920 mVpp（typ）
L	570～900 mVpp，700 mVpp（typ）
Suspended or V_{CC}/2	9-bit binary code input control of serial interface, 560-840 mVpp, default 700 mVpp

e. Clock input/output

The CD08AD1500 must be driven by a differential clock signal through AC coupling connection.

2.3) describes the use of the clock input pin. A differential LVDS output clock is used to latch ADC output data for subsequent devices to receive data. The CD08AD1500 provides two output clock options: one is to select whether the output data is converted at the upper edge of the output clock QCLK or at the lower edge of the output clock; the other is to select whether the output is single data rate (SDR) or dual data rate (DDR), as shown in Table 6, and the timing is shown in Figures 2 and 3.

Table 6. Output Clock Selection (FSR is H or L)

OutEdge/DDR (pin4)	Mode	Output clock
H	SDR	The frequency is 1/2 of the input frequency, and the output data is converted on the upper edge of the clock
L		The frequency is 1/2 of the input frequency, and the output data is converted at the lower edge of the clock
Suspended or $V_{CC}/2$	DDR	The frequency is 1/4 of the input frequency, and the output data is converted on the upper and lower edges of the clock

There is a duty cycle regulator inside the clock input of CD08AD1500 to improve the performance of the internal clock. You can select whether the duty cycle regulator works through the extended mode (address code 0001). The default setting is working. The duty cycle regulator allows the clock of ADC to be a signal source with a duty cycle of 20-80% (worst case).

① . Double edge sampling (DES function)

DES mode allows one input (I or Q channel) of CD08AD1500 to be sampled by two ADCs. One ADC samples the input signal at the positive edge of the input clock, and the other ADC samples the input at the negative edge of the input clock. Therefore, the signal input is sampled twice in each clock cycle, so a complete sampling rate is twice the input clock frequency, or the sampling

rate for the 1.5GHz input clock is 3GSPS。

In this mode, the interleaved output data is converted to 1:4 by a multiplexer. Since the sampling rate is twice, under the 1.5GHz input clock, any of the four data outputs will be output at a rate of 750MHz, and all data will be output in parallel. The 4-way parallel data output by each clock follows the sampling sequence from the earliest to the last: D_{Qd}, D_{Id}, D_Q, D_I, that is, D_{Qd} at the earliest, followed by DId, and finally DI; This means that it is possible to provide different sampling rates. Double edge sampling In the general control mode, only the "I" analog input (INI) is available, and the "Q" analog input (I_{NQ}) is not used. In the extended control mode, the user can select any one ("I" or "Q") as the analog input to be sampled, and the address code is 1110. See Table 7 for control functions.

The CD08AD1500 includes an automatic clock phase background correction feature, which can automatically and continuously adjust the clock phases of channel I and channel Q in DES mode. This feature eliminates the need to manually set the clock phase and provides the best bilateral edge sampling ENOB performance.

Special attention: The background correction feature in DES mode cannot replace the instruction correction to be run before entering DES mode, or the instruction correction required when the chip operating environment temperature changes greatly.

Table 7 Sampling Time of Input Channel Corresponding to Output Data

Data output (always corresponding to the falling edge of QCLK)	General sampling mode	Double edge sampling mode (DES)	
		Select I channel input	Select Q channel input*
D_I	"I" input sampling corresponds to the falling edge of the first 13 IN_{CLK}	"I" input sampling corresponds to the falling edge of the first 13 INCLK	"Q" input sampling corresponds to the falling edge of the first 13 INCLK

	cycles of the output	cycles of the output	cycles of the output
D_{Id}	"I" input sampling corresponds to the falling edge of the first 14 IN_{CLK} cycles of the output	"I" input sampling corresponds to the falling edge of the first 14 INCLK cycles of the output	"Q" input sampling corresponds to the falling edge of the first 14 INCLK cycles of the output
D_Q	"Q" input sampling corresponds to the falling edge of the first 13 IN_{CLK} cycles of the output	"I" input sampling corresponds to the rising edge of the first 13.5 INCLK cycles of the output	"Q" input sampling corresponds to the rising edge of the first 13.5 INCLK cycles of the output
D_{Qd}	"Q" input sampling corresponds to the falling edge of the first 14 IN_{CLK} cycles of the output	"I" input sampling corresponds to the rising edge of the first 14.5 INCLK cycles of the output	"Q" input sampling corresponds to the rising edge of the first 14.5 INCLK cycles of the output
*DES normal mode, only channel I samples. In the extended mode of DES, I or Q channels can be sampled.			

②. OutEdge pin settings

To make it easy to sample data in SDR mode, the output data can be converted on the positive or negative edge of the output data clock (Q_{CLK}). This can be selected via the OutEdge input (pin 4). When the OutEdge input is high, the output data is converted at the rising edge of Q_{CLK}; When the OutEdge input is low, the output data is converted at the falling edge of Q_{CLK}, as shown in Table 6. Refer to 2.4). c Output edge synchronization.

③ . Double data rate

Provides a choice of single data rate (SDR) or double data rate (DDR) output. If it is SDR, the output clock (Q_{CLK}) frequency is the same as the data rate of the two output buses. If it is DDR, the Q_{CLK} frequency is half of the data rate, and the data is sent to the output terminal at the two edges of the Q_{CLK}. The DDR clock is controlled by suspending pin 4 or V_CC/2. It is effective in the FSR (pin 14) common control mode, as shown in Table 4 and Table 6.

f. LVDS output

Data output, overflow output (D_{OR}) and clock output (Q_{CLK}) are LVDS. When the Outv input (pin 3) is high, the output current source will provide an output current of 3mA to a differential resistance load of 100 Ω; When the Outv input (pin 3) is low, the output current source will provide an output current of 2.2mA to a differential resistance load of 100 Ω, as shown in Table 8. In order to shorten LVDS line length and reduce system noise, Outv outputs.

If the input (pin 3) is low, satisfactory performance will be obtained while reducing power consumption. If the LVDS line is too long or the CD08AD1500 system is too noisy, it is necessary to connect the Outv input to the high level. When V_{REF} (pin 31) is not connected or suspended, LVDS data output has a common mode voltage of 800mV. If higher common mode voltage is required, the common mode voltage can be increased to 1.2V by connecting V_{REF} pin to VCC, as shown in Table 9.

Special attention: connecting V_{REF} pin to V_{CC} will also increase the differential LVDS output voltage by 40mV.

Table 8. LVDS Output Amplitude Control

Outv input (pin 3)	LVDS output amplitude
H	400～1000mVpp，700 mVpp(typ)
L	280～800mVpp，500 mVpp(typ)

Table 9. LVDS Output Common Mode Voltage (VOS)

VREF (pin 31)	LVDS output amplitude
H	1.2V(typ)

L	800mVp(typ)

g. Power Down

When PD (pin 26) is low, the CD08AD1500 is in normal operation. When the PD pin is high, the device is in power saving mode. In the power saving mode, the data output pins (positive and negative) are tristate, and the device power consumption is minimized. Clock output ($Q_{\overline{CLK}}$ and Q_{CLK}) and overflow output ($D_{\overline{OR}}$ and D_{OR}) are not tri state, they are pulled to the ground internally. Therefore, when I and Q are both power saving modes Clock output and overflow output cannot be connected to a DC voltage. When the PDQ pin is high or suspended, the "Q" channel will be in the power saving mode, and the "I" channel will be in the normal working state, which is not controlled by the PDQ, as shown in Table 10. Back to the normal working mode, the channel will contain meaningless information. If PD is set to high during calibration operation, the device will not enter into power saving operation and will still work normally until the calibration timing is completed. However, if the device is powered on and the PD is high, the device will enter into power saving operation, and no correction will be made until the PD becomes low. If the device is in power saving mode and requires manual calibration, calibration will not start at all. That is to say, the manual correction input is completely blocked by the power saving state. However, if the PDQ is high, the "Q" channel is in the power saving mode, the "I" channel calibration will still run, and the "Q" channel cannot be calibrated. If the "Q" channel is used later, it is necessary to make a correction after the PDQ is low.

Table 10. Power saving mode control

Power saving mode control	Operating mode

PD	PDQ	I	Q
H	H or L	Power saving mode	Power saving mode
L	H or suspended	Normal operation	Power saving mode
	L	Normal operation	Normal operation

2) . Common/extended control

The CD08AD1500 can work in either of these two modes. Common standard control mode, users can set and control the working state of devices through several pins; "Extended control mode" is to realize additional configuration and control selection through a serial interface and the setting of 9 registers. Two control modes are selected through pin 14 (FSR/ST1: full scale range selection and extended control mode selection). The selection of control mode must be a fixed choice, and these two modes cannot be switched at will when the device is working. Table 11 shows that device characteristics are affected by control mode selection.

Table 11. Device Characteristics and Modes

Characteristic	Normal control mode	Extended Control Mode
SDR or DDR mode clock	Pin 4 is suspended or VCC/2 selects DDR clock, SDR clock is selected for high or low	Select with nDE in the configuration register (1h; D10). When the device is in DDR mode, set the address 1h, and bit-8 must be 0.
DDR mode clock phase	No selection, only 0 ° phase	In the configuration register (1h; D11), select with DCP.
SDR mode, data conversion is on the rising or falling edge of QCLK	When pin 4 is high, SDR data is converted at the rising edge of QCLK+; When lead 4 is low, the falling edge switches	In the configuration register (1h; D8), select with OE
LVDS output amplitude	Pin 3 is high, normal differential data and Q_{CLK} output amplitude; When it is low, reduce the amplitude.	In the configuration register (1h; D9), select with OV

Power on correction delay	When pin 127 is low, select a short delay; For high, select a long delay.	Only a short delay
Full scale range	When pin 14 is high, the normal input full scale range; When it is low, reduce the range. Range selection is valid for both channels.	In the 1.4 register description, up to 512 steps are adjusted throughout the normal full scale range. Select the input full scale range adjustment register (3h; D7~D15)
Input maladjustment adjustment	Not adjustable	Adjust with input offset register (2h; D7~D15), up to 512 steps
Double edge sampling selection	Pin 127 suspended or $V_{CC}/2$	Control through DES enable register
Double edge sampling input channel selection	Only channel I input is available	Either I or Q channel input can be sampled by two ADC
DES sampling clock adjustment	The clock phase is automatically adjusted	Set D14 enable register (Dh) in DES to select automatic clock phase control. The clock phase can also be manually adjusted through the coarse and fine registers (Eh and Fh).

The default state of the extended control mode is set by power on reset, as shown in Table 12.

Table 12. Extended control mode operation (pin14 suspension or $V_{CC}/2$)

Characteristic	Extended Control Mode Default State
SDR or DDR mode clock	DDR mode clock
DDR mode clock phase	QCLK edge (0° phase) data change
LVDS output amplitude	Normal amplitude (700m Vpp)
Power on correction delay	Reduced latency
Analog Input Full Scale Range	Both channels are 700mVpp
Input maladjustment adjustment	None misadjusted adjust
Double edge sampling (DES)	Do not use this mode

3) . Serial interface

The 3-wire serial interface can only be activated when the device is operating in the extended control mode. The pins of these serial interfaces are serial clocks(SCLK), serial data (DATA) and serial interface selection (ST2). Eight write only registers acquire signals through the serial interface.

ST2: When accessing a register through the serial interface, this signal should be low. Relative to the establishment time and retention time of SCLK requirements must be met.

SCLK: Serial data input is obtained at the rising edge of this signal, and there is no minimum frequency requirement for SCLK.

DATA: Each register access requires an explicit 32-bit combination format for this input. This format consists of header mode, register mode

Address and register value, and the register value starts from MSB bit. The establishment time and retention time relative to SCLK must meet the requirements sequence diagram.

Each register access consists of 32 bits, as shown in the sequence diagram in Figure 4. Fixed head mode is 0000 0000 0001, the writing order is 0, and the 12 bits constitute the header mode. Next, write the address of 4-bit register, and the last 16 bit data is write to the register. The addresses of different registers are described in detail in Table 13.

When $\overline{ST2}$ is permanently kept at low level, the subsequent register access from the 33rd SCLK can be directly completed no more strobe between. Although this usage is not recommended, it is possible.

Important note: When correcting ADC, do not use the serial interface. If it is used, the performance of the device will be reduced, unless it is correct again correction of. Serial interface

register operation during register access will also reduce the dynamic characteristics of ADC.

Table 13. Register Address

4-bit address Address writing order: A3 is locked after H0 (the last bit of fixed head mode, i.e. "1"), and A0 is locked last					
A3	A2	A1	A0	Hex	Register address
0	0	0	0	0h	retain
0	0	0	1	1h	Status Configuration
0	0	1	0	2h	I channel input imbalance adjustment
0	0	1	1	3h	I channel full scale voltage regulation
0	1	0	0	4h	retain
0	1	0	1	5h	retain
0	1	1	0	6h	retain
0	1	1	1	7h	retain
1	0	0	0	8h	retain
1	0	0	1	9h	retain
1	0	1	0	Ah	Q channel input offset adjustment
1	0	1	1	Bh	Q channel full scale voltage regulation
1	1	0	0	Ch	retain
1	1	0	1	Dh	DES enable

1	1	1	0	Eh	DES coarse adjustment
1	1	1	1	Fh	DES fine regulation

Matters needing attention

1. The external resistance Rext of pin 32 must be exactly equal to 3.3kΩ ± 0.1%, and other values cannot be used, as described in 1.1). a.

2. In application, it is recommended that PCB be grounded in large area. This can eliminate the potential difference due to different grounding points, and reduce the influence of capacitance generated by the circuit board on the circuit.

3. When using, do not insert the circuit reversely, otherwise the circuit may be damaged.

4. Each power supply pin needs to be connected to a nearest 0.1 μ F and 33 μ F capacitance.

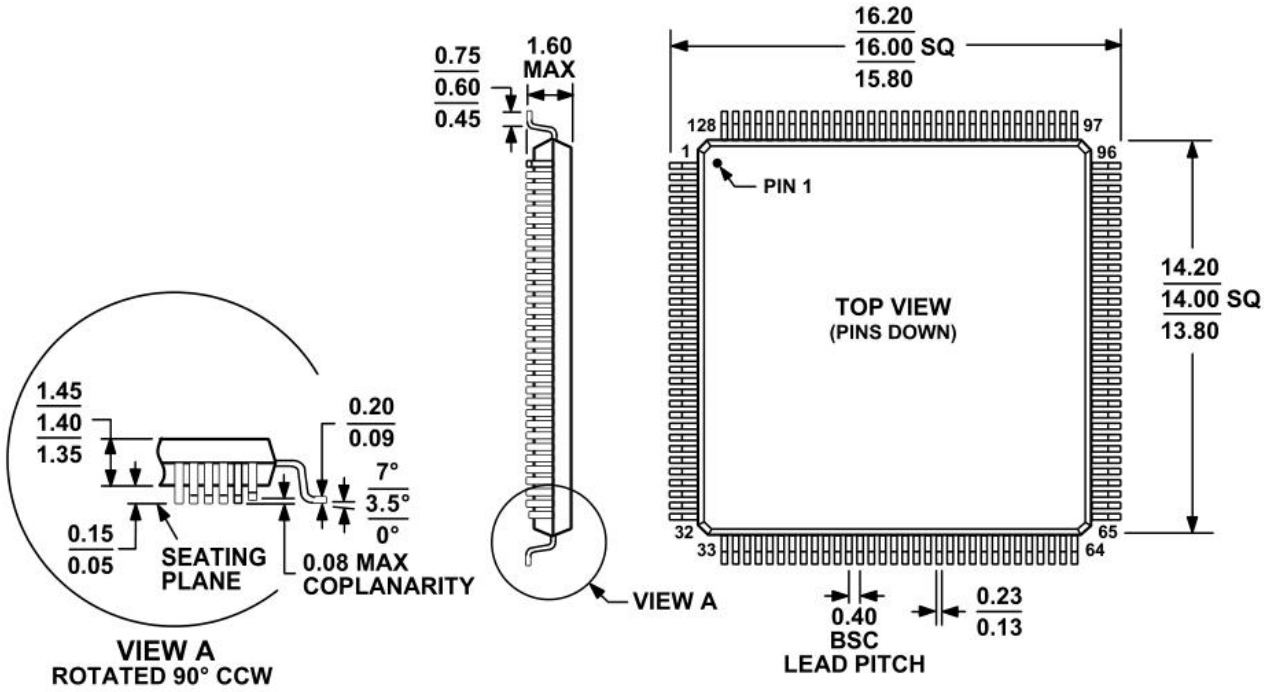
5. The routing of differential analog input must be equal.

6. The digital power supply and the analog power supply need to be separated.

7. All leading out ends of the circuit are designed with electrostatic protection structure, but large energy electric pulse may still damage the circuit, so pay attention to electrostatic protection during testing, handling and storage.

Package Outline Dimensions

TQFP-128



Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD08AD1500-500	-40℃-85℃	QFN-56	Tray, 260
CD08AD1500-370	-40℃-85℃	QFN-56	Tray, 260

Chinese version:CD08AD1500

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.5.20	Initial version	Regular update	WW	LYL	