CoreadDvices
承芯微电子

CD108S085/CD128S085

10/12-bit, 8-channel micropower DAC with rail-to-rail output

Version: Rev 1.0.0 Date: 2025-8-4

Features

- TSSOP16,QFN 16 pin package
- I / O voltage: 1.8V - 5.5V
- Core voltage: 1.8V - 3.6V
- Maximum 1MHz continuous data output rate
- Temperature range - 40 ℃ - 125 ℃
- Four wire SPI interface
- Pulse generator
- Clock calibration unit
- Precise stop pulse enable window
- The rising edge / falling edge is triggered separately or both rising edge

Application

- Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current
- Programmable Attenuators
- Voltage Reference for ADCs
- Sensor Reference Supply Voltage
- Range Detectors

Description

CD128S085/CD108S085 is a high-precision and highly integrated digital to analog converter chip. A single chip integrates an 8-channel 12 / 10-bit voltage output digital to analog converter with output buffer drive. The chip is packaged with a smaller 16-pin TSSOP; The normal operational power supply voltage range is 2.7V ~ 5.5V; The output buffer drive can ensure that the output voltage is rail to rail, so as to ensure the maximum voltage output range; The power consumption is very low. Without load, the overall consumed current is only 540uA@3V , 600uA@5V. The three-wire serial interface is adopted, and the maximum clock can reach 40MHz. It allows very flexible configuration and is compatible with the current common SPI ™, QSPI, MICROWIRE, DSP and other interface standards. It supports daisy chain working mode. A single interface can control multiple chips at the same time to ensure that multiple chips update their status at the same time.

CD128S085/CD108S085 have two external reference voltage inputs, one for channels A to D and the other for channels E to H. Each reference voltage can be configured separately, allowing the input range to be 0.5V ~ VA, so as to ensure that the chip provides the widest possible dynamic output range. The 16 shift registers at the digital input controlled by the serial interface can easily control the working mode of the chip, including sleep output state and output update

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state. All channels can be updated individually or uniformly.

The biggest feature of CD128S085/CD108S085 is that it supports both power on reset and power-off reset. The power on reset circuit ensures that when the power supply voltage rises to the effective voltage, the output of the digital to analog converter is 0V and remains in this state until a new state update command is received. When the chip power supply voltage drops below 2.7V, the power-off reset circuit resets the chip so that the output of the digital to analog converter is 0V, so as to avoid the impact of the non-0V output voltage of the digital to analog converter on the system circuit. The chip multi-channel can be flexibly configured, allowing each channel to work independently, and supports three different output impedance sleep modes. When all digital to analog converters enter sleep mode, the chip is at uW power consumption. The low power consumption of the chip makes it very suitable for portable devices.

Contents

Functional Block Diagram

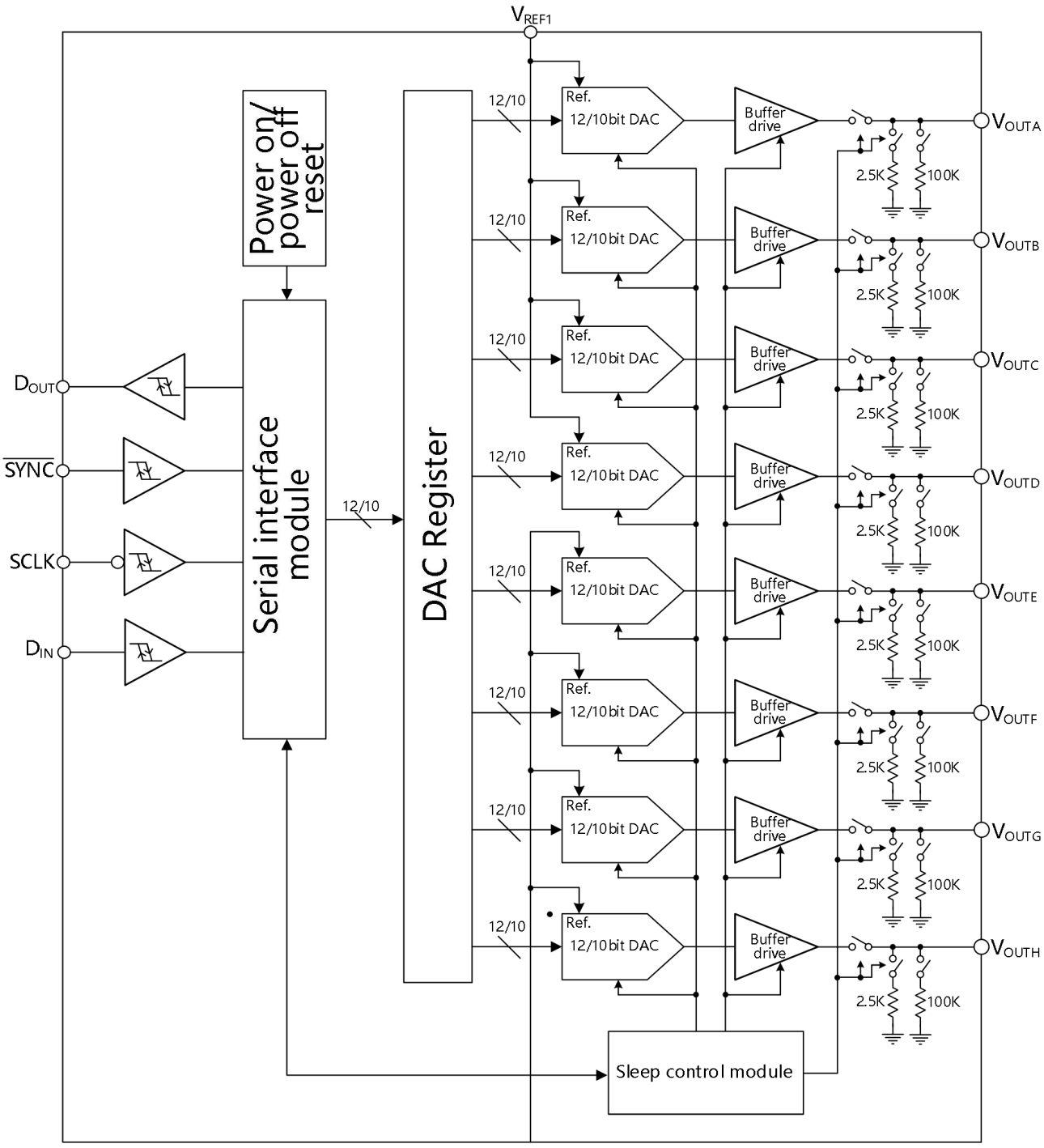

Figure 1. Functional Block Diagram

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Absolute Maximum Ratings

(T_A=25℃,unless otherwise noted.)

Parameter 1	Symbol	Value
Supply voltage to ground	V_{Aabs}	-0.3V to+7V
Digital input voltage to ground	V_{Digabs}	-0.3V to +0.3V
Reference input voltage to ground	V_{refabs}	-0.3V to +0.3V
A ~ H to ground	V_{outabs}	-0.3V to +0.3V
temperature range		
Storage Temperature	T_S	-65℃ to +150℃
Junction Temperature	T_{Jmax}	150℃
ESD characteristics		
Human Body Model		5000V
Machine Model		300V
Charge Device Model		1000V

Recommended Operating Range

Parameter	Symbol	Range		Unit
		Min	Max	
Supply Voltage	VA	2.7	5.5	V
Operation Current [1]	IA	300	700	uA
Ambient Temperature	Ta	-40	125	℃
Reference Voltage	$V_{REF1,2}$	0.5	VA	V
Output Load	CLoad	0	1500	pF
SCLK Clock Frequency	F_{SCLK}	\	40	MHz

[1]. DAC output at no load

Specifications

Static characteristic

(V_A=2.7V to 5.5V,V_{REF}1,2=V_A,C_L=200pF to ground; Ta=25℃ ,unless otherwise noted.)

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
Static characteristic						
CD128S085						
Resolution	Res_N			12		Bits
Integral Non-Linearity	INL			±2		LSB
Differential Non-Linearity	DNL	Guaranteed monotonicity		±0.2		LSB
CD108S085						
Resolution	Res_N			10		Bits
Integral Non-Linearity	INL			±0.5		LSB
Differential Non-Linearity	DNL	Guaranteed monotonicity		±0.05		LSB
Zero Code Error	ZE	IOUT = 0		+5	+15	mv(max)
Full-Scale Error	FSE	IOUT = 0		-0.1		% FSR(max)
Gain Error	GE			-0.2		% FSR(max)
Zero Code Error Drift	ZCED			-20		uV/℃
Gain Error Tempco	TC GE			-1.0		ppm/℃
Reference voltage input characteristics						
F1,2 Input Range			0.5		V_A	V
F1,2 Input Impedance				45		KΩ
Output Characteristic						
Minimum output voltage				0		V
Maximum output voltage				$V_{REF1,2}$		V
DC output impedance	Z_{OUT}			0.5		Ω
Zero Code Output	ZCO	V_A = 3V, I_{OUT} = 200uA		10		mv
		V_A = 3V, I_{OUT} = 1mA		45		mv
		V_A = 5V, I_{OUT} = 200uA		8		mv
		V_A = 5V, I_{OUT} = 1mA		34		mv
Full Scale Output	FSO	V_A = 3V, I_{OUT} = 200uA		2.984		V
		V_A = 3V, I_{OUT} = 1mA		2.933		V
		V_A = 5V, I_{OUT} = 200uA		4.987		V
		V_A = 5V, I_{OUT} = 1mA		4.955		V
Output Short Circuit Current (Source)	IOS	V_A = 3V, V_{OUT} = 0V, Input Code = FFFh		-20		mA

		V_A = 5V, V_{OUT} = 0V, Input Code = FFFh		-20		mA
Output Short Circuit Current（Sink）	IOS	V_A = 3V, V_{OUT} = 3V, Input Code = 000h		20		mA
		V_A = 5V, V_{OUT} = 5V, Input Code = 000h		20		mA
Maximum Load Capacitance	CL	R_L = ∞		1500		pF
		R_L = 2kΩ		1500		pF
Logic input characteristics[3]						
Input Low Voltage		V_A=3V			0.6	V
		V_A=5V			0.8	V
Input High Voltage		V_A=3V	2.1			V
		V_A=5V	2.4			V
Input Capacitance				3		pF
Power consumption characteristics						
Supply Voltage	V_A		2.7		5.5	V
Power quiescent current	IST	F_{SCLK}=0，output unloaded V_A = 2.7V ~ 3.6V，input code is 0x800		540		uA
		F_{SCLK}=0，output unloaded V_A =4.5V ~ 5.5V, input code is 0x800		600		uA
Reference voltage and current		V_A = 2.7V ~ 3.6V, input code is 0x800 V_A = 2.7V ~ 3.6V, input code is 0x800		73		uA
		V_A =4.5V ~ 5.5V, input code is 0x800		110		uA
Power Down Supply Current4		F_{SCLK}=0，Sync=V_A，D_{IN}=0V，DAC PD mode		10		uA

1. During the static characteristic test, the DAC output has no load.
2. Input code range during linear characteristic test: CD128S085(Code 48 to Code 4047), CD108S085(Code 12 to Code 1011).
3. The design value is not the actual test value.
4. In power-down mode, the power-off reset circuit of the chip still works, consuming about 10uA current.

Dynamic Characteristics

(V_A=2.7V to 5.5V,V_{REF}1,2=VA; C_L=200pF to Ground; Ta=25℃ ,unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Type	Max	Unit
SCLK Frequency	FSCLK				40	MHz
Output Voltage Settling Time[1]	t_S	R_L=2KΩ , C_L=200pF, 0x400 to 0xC00 Digital code change		6	8.5	uS
Output Slew Rate	SR			1		V/uS
Glitch Impulse	GI	Digital Code change from 0x7FF to 0x800		40		nV-sec
Digital Feedthrough[1]	DF			0.5		nV-sec
Digital Crosstalk[1]	DC			0.5		nV-sec
Multichannel crosstalk[1]	CROSS			1		nV-sec
Output bandwidth	MBW	$V_{REF1,2}$ = 2.5V ± 2Vpp		350		KHz
Total Harmonic Distortion Plus Noise[1]	THD+N	$V_{REF1,2}$ = 2.5V ± 0.5Vpp 100Hz < f_{IN} < 20kHz		-80		dB
Output Noise Spectral Density[1]	ONSD	Digital code 0x800, 10kHz		80		nV/sqrt(Hz)
Output Noise[1]	ON	BW = 30kHz		14		uV
Wake-Up Time	tWU	V_A=3V		5		uS
		V_A=5V		3		uS
SCLK minimum Cycle Time	1/fSCLK			25	33	nS
SCLK Minimum High time	tCH			7	10	nS
SCLK Minimum Low time	tCL			7	10	nS
YNC Minimum setup time	tSS			3	10	nS
DATA Minimum setup time	tDS			1	2.5	nS
DATA Minimum holding time	tDH			1	2.5	nS
YNC Minimum holding time	tSH			0	3	nS
YNC Minimum High time	tSYNC			5	15	nS

[1]. The design value is not the actual test value.

Pin Configurations and Function Descriptions

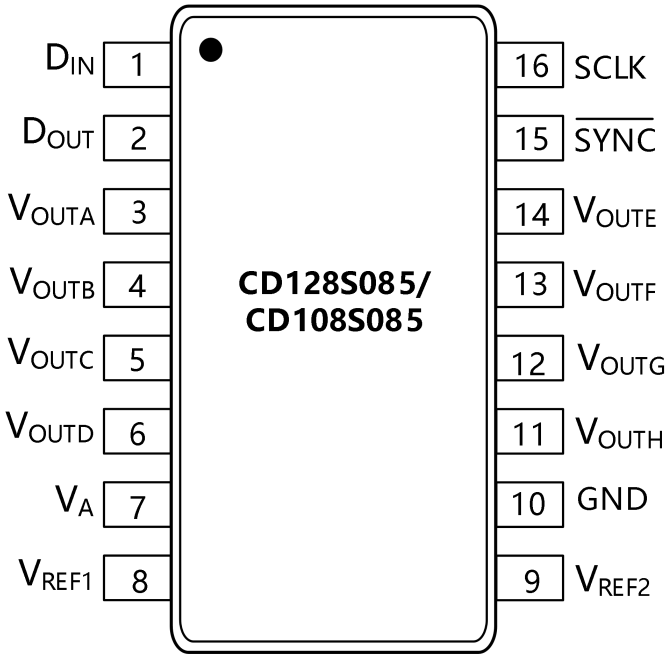

Figure 2. TSSOP-16 pin configuration

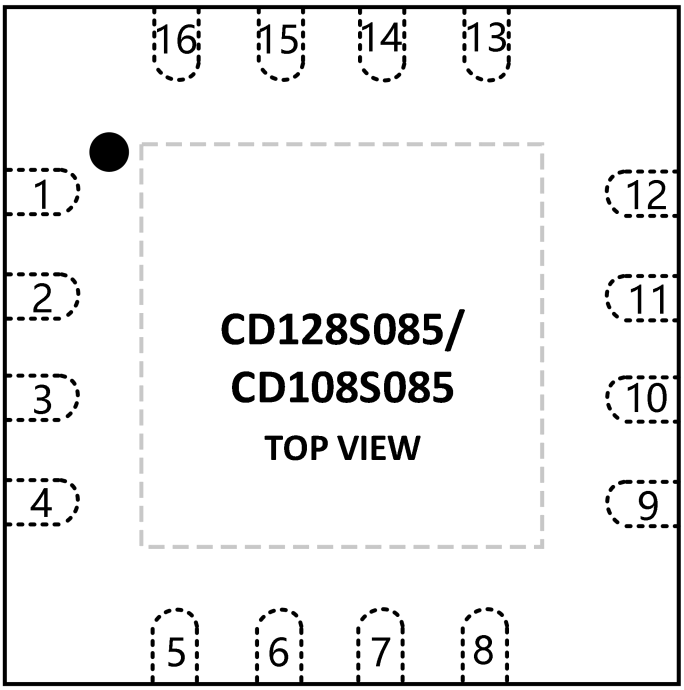

Figure 3. QFN-16 pin configuration

Pin Function Descriptions

Pin			Type	Description
Pin name	TSSOP NO.	QFN NO.		
DIN	1	15	Digital Input	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of SYNC.
DOUT	2	16	Digital output	Serial Data Output. DOUT is utilized in daisy chain operation and is connected directly to a DIN pin on another DAC128S085. Data is not available at DOUT unless SYNC remains low for more than 16 SCLK cycles.
GND	10	8	Ground	Ground reference for all on-chip circuitry.
SCLK	16	14	Digital Input	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
$\overline{SYNC}$	15	13	Digital Input	Frame Synchronization Input. When this pin goes low, data is written into the DAC's input shift register on the falling edges of SCLK. After the 16th falling edge of SCLK, a rising edge of SYNC causes the DAC to be updated. If SYNC is brought high before the 15th falling edge of SCLK, the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC.
V_A	7	5	Supply	Power supply input. Must be decoupled to GND.
V_{OUTA}	3	1	Analog output	Channel A Analog Output Voltage.
V_{OUTB}	4	2	Analog output	Channel B Analog Output Voltage.
V_{OUTC}	5	3	Analog output	Channel C Analog Output Voltage.
V_{OUTD}	6	4	Analog output	Channel D Analog Output Voltage.
V_{OUTE}	14	12	Analog output	Channel E Analog Output Voltage.
V_{OUTF}	13	11	Analog output	Channel F Analog Output Voltage.
V_{OUTG}	12	10	Analog output	Channel G Analog Output Voltage.
V_{OUTH}	11	9	Analog output	Channel H Analog Output Voltage.
V_{REF1}	8	6	Analog input	Unbuffered reference voltage shared by Channels A, B, C, and D. Must be decoupled to GND.
V_{REF2}	9	7	Analog input	Unbuffered reference voltage shared by Channels E, F, G, and H. Must be decoupled to GND.
PAD(QFN only)	--	17	Ground	Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow.

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Typical Performance Characteristics

$V_A=V_{REF}=5V$, $T_a=25℃$, unless otherwise noted.

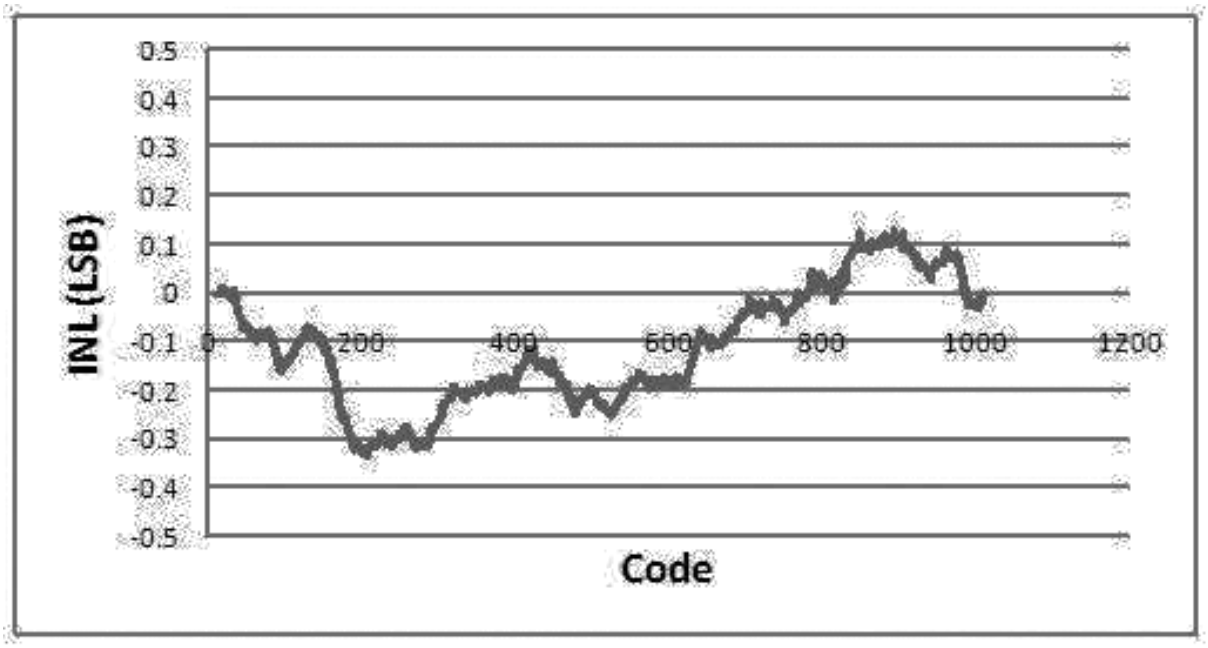

Figure 4. CD108S085 typical INL

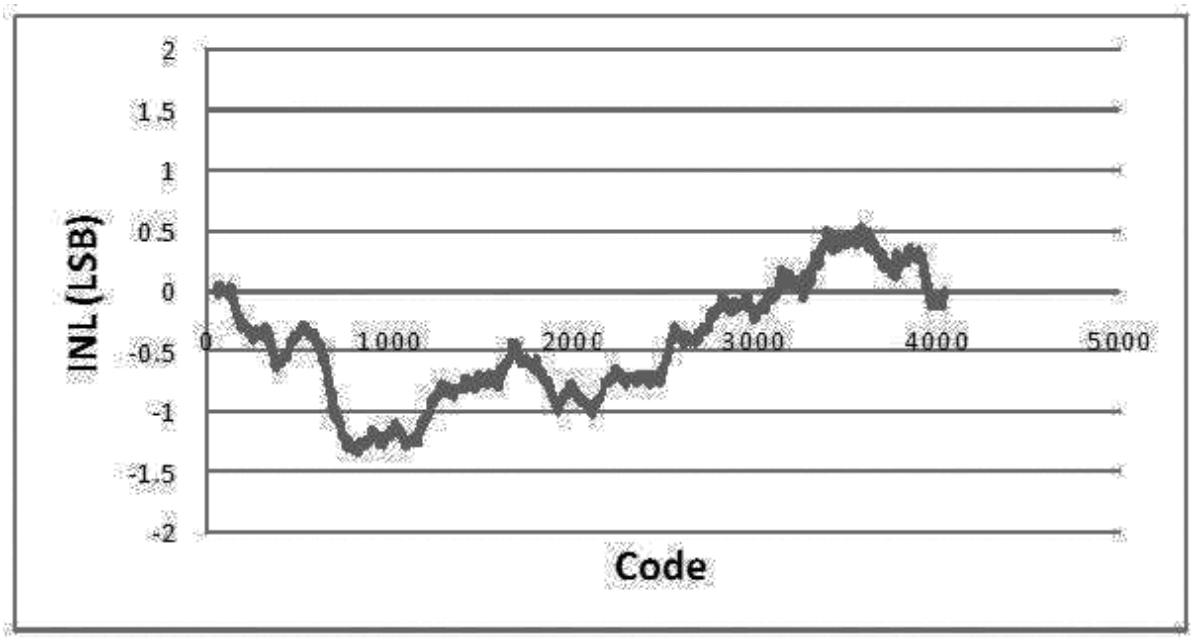

Figure 5. CD128S085 typical INL

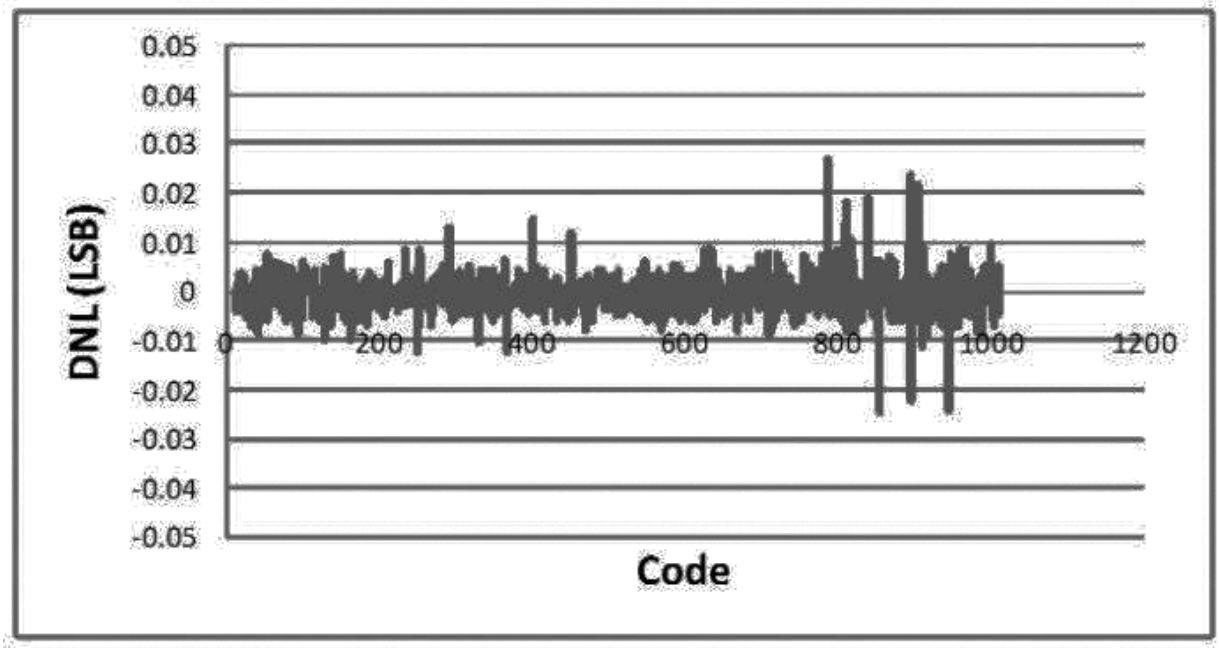

Figure 6. CD108S085 typical DNL

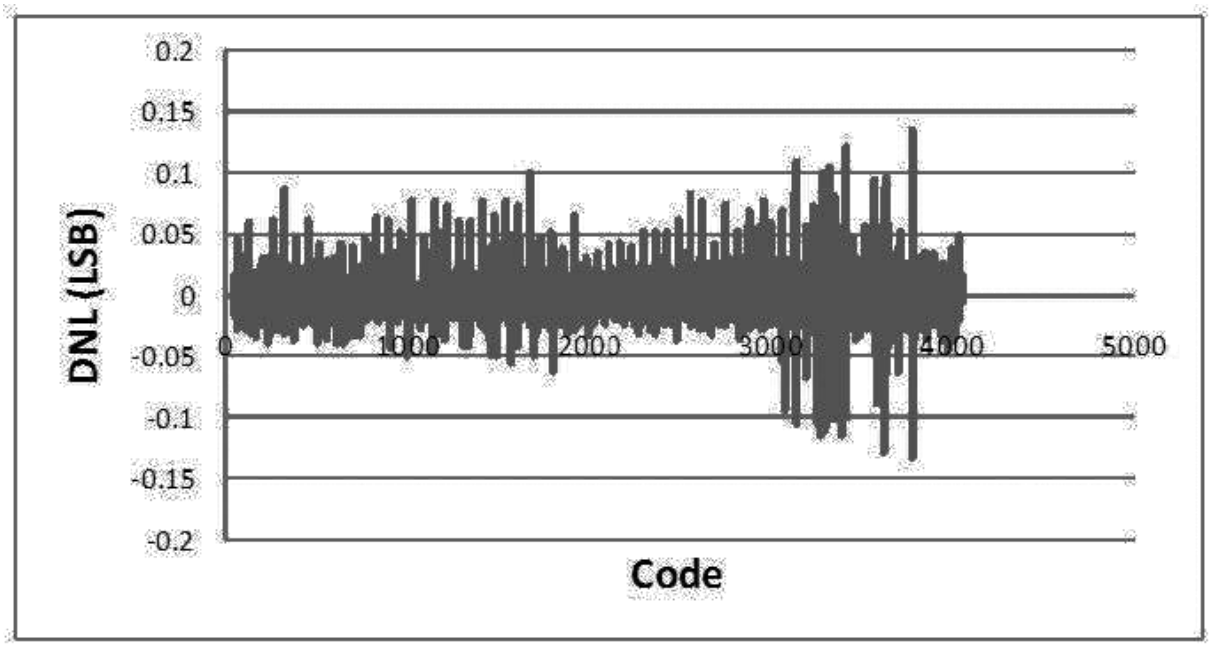

Figure 7. CD128S085 typical DNL

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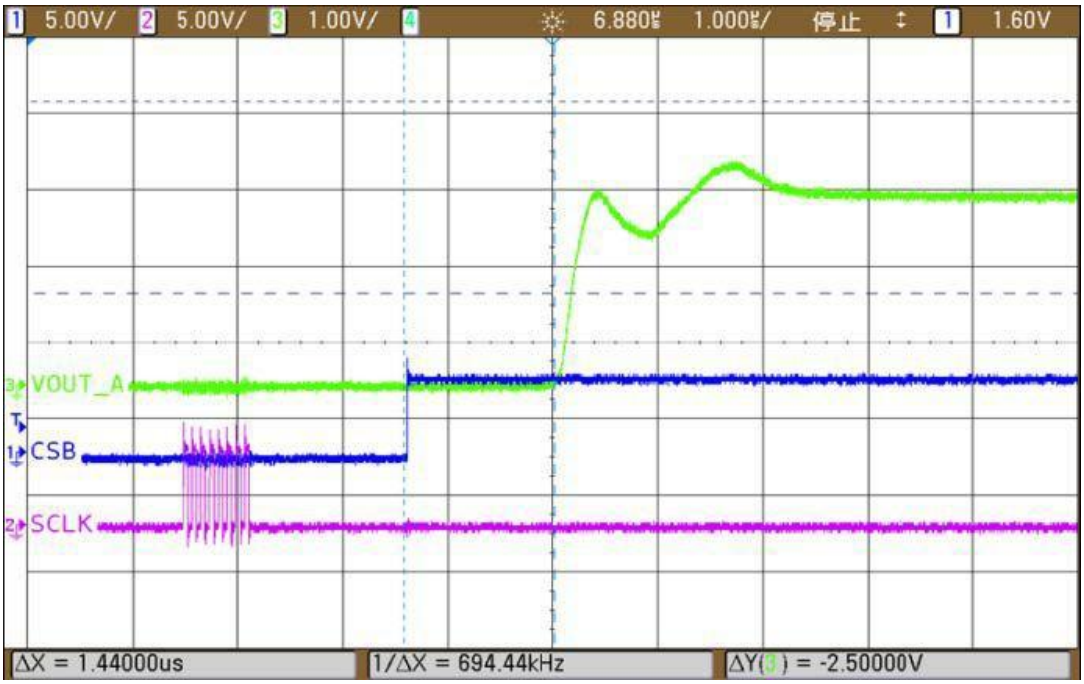

Figure 8. DAC wake-up (out of sleep) process

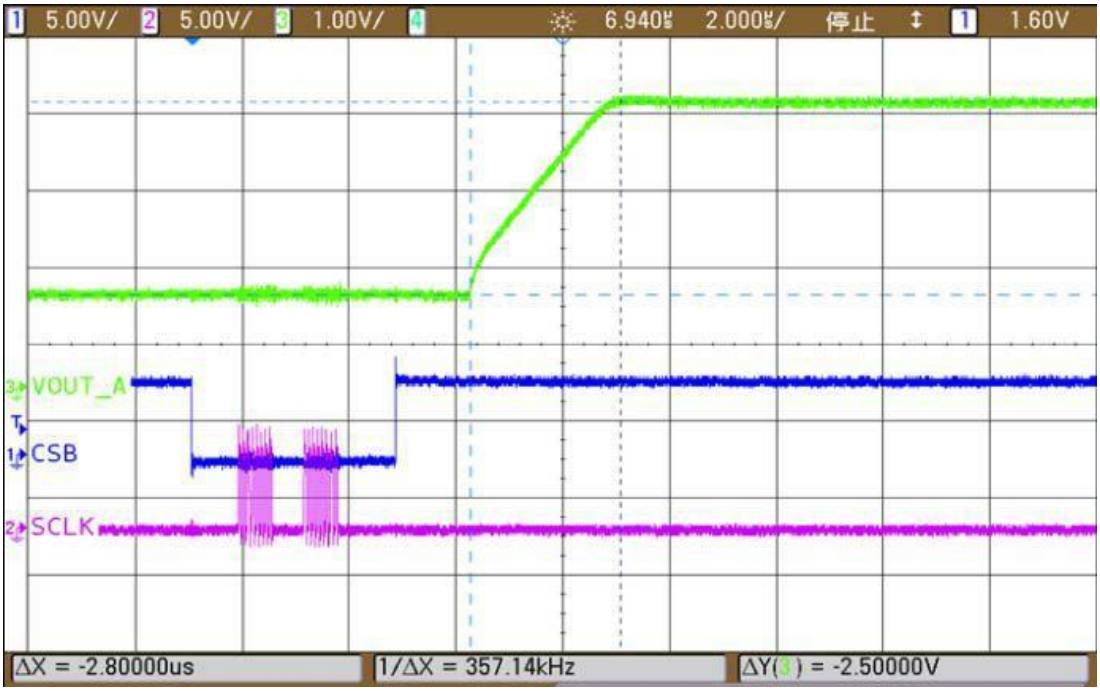

Figure 9. Output establishment process (change of 0.25 full amplitude to 0.75 full amplitude)

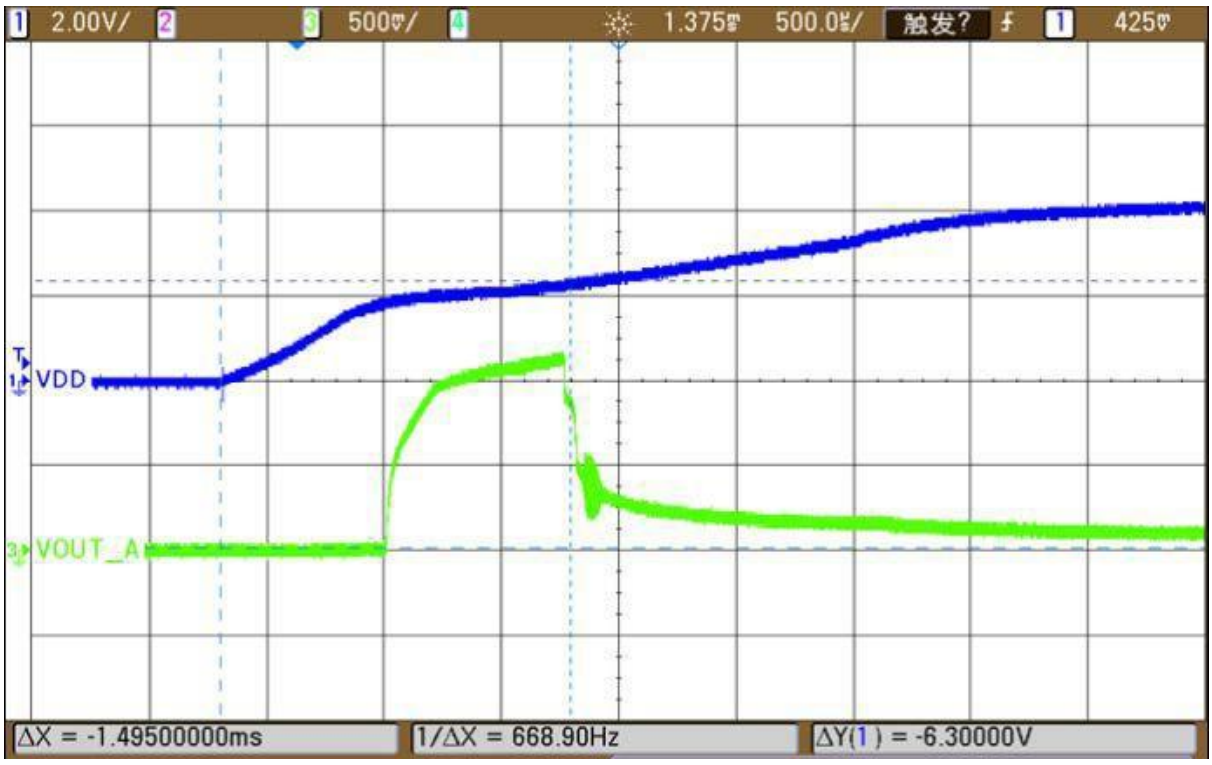

Figure 10. Power on reset

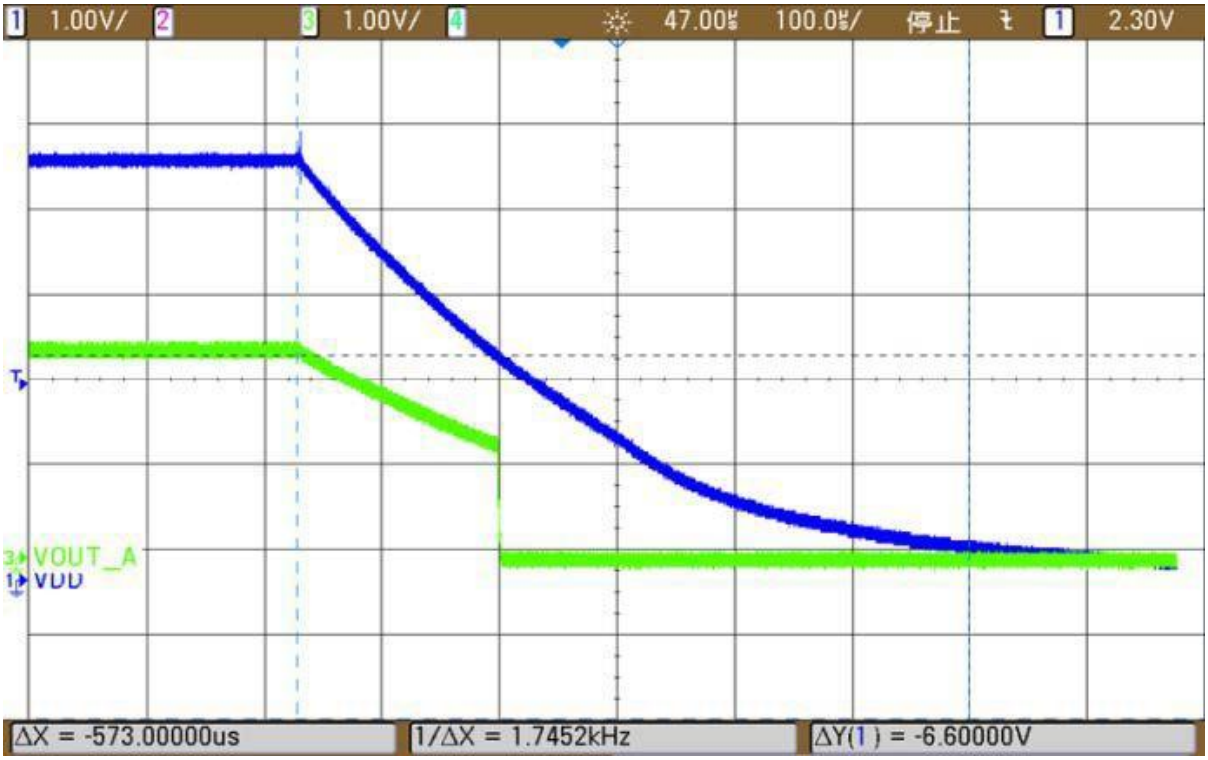

Figure 11. power off reset

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Applications Information

DAC structure

CD128S085/CD108S085 contain 8-channel DAC. Each channel contains a DAC register, a resistance string DAC and an output driver circuit. The resistance string structure DAC generates the corresponding level through the resistance string voltage division, and then the switch selects the corresponding output. In order to drive the external load, a buffer driving circuit is added at the output of each channel.

The schematic diagram of DAC structure of resistance string is shown in Figure 12. The resistance string is composed of N equivalent resistors. The reference voltage is directly added to the resistance string. The resistance partial voltage generates N output voltages, which are controlled by N switches respectively. The adjacent voltages are VLSB. Each resistance voltage can be output by closing the corresponding switch. The digital input signal controls the closing and opening of the switch. Each input code corresponds to a switch. Therefore, for 10bit accuracy, N = 1024, For 12bit accuracy, N = 4096.

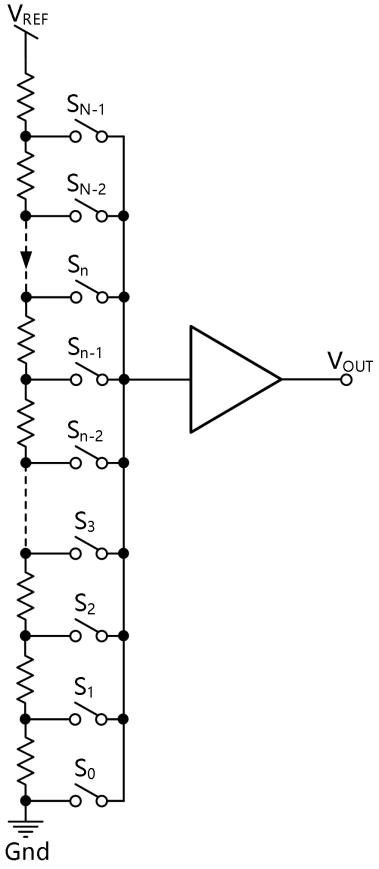

Figure. 12. structure diagram of resistance string DAC

When the input digital signal is D

$$V_{OUT} = V_{REF} \times (D/N)$$

When CD128S085, N = 4096; When CD108S085, N = 1024. The 8-channel DAC in CD128S085/CD108S085, in which the ABCD channel adopts V_{REF1} reference voltage and the EFGH channel adopts V_{REF2} reference voltage. The reference voltage is directly input from the outside, so it can be set flexibly. The digital signal D is written into the internal DAC register by the serial interface, and then controls the final output voltage of the DAC. The 8-channel DAC of CD128S085/CD108S085 can individually controlled enabled or dormant separately. The output of DAC in dormant state has three modes: high resistance, 2.5k Ω impedance to ground and 100k Ω impedance to ground, which can be selected according to actual needs

The DAC output buffer drive circuit adopts rail to rail structure, and the output voltage range is [0, VA] (the actual output voltage range is limited by the reference voltage). When the output voltage is close to 0 or VA, the linearity of the buffer drive circuit will deteriorate rapidly. Therefore, some maximum codes and minimum codes are removed from the definition of linearity index INL, which should be paid attention to in practical application. The output buffer drive circuit can drive 2K Ω resistive load and 1500pf capacitance to ground or power supply. When the load resistance decreases, the driving current increases accordingly, resulting in changes in the output voltage. Please refer to the previous characteristic description for specific results. The buffer drive circuit has built-in output short-circuit protection device, and the typical value of protection current is 20mA.

Serial Interface

Serial Interface Description

Three wire serial interface at input is compatible with SPITM, QSPI, and MICROWIRE, as well as most DSPs, and operates at clock rates up to 40MHz. The chip writes at the falling edge of the clock, and the data takes 16 cycles as a frame, that is, there are 16 falling edges of the clock in a frame of data synchronization sequence. The detailed interface timing is shown in Figure 13. Please refer to table 4 for specific values.

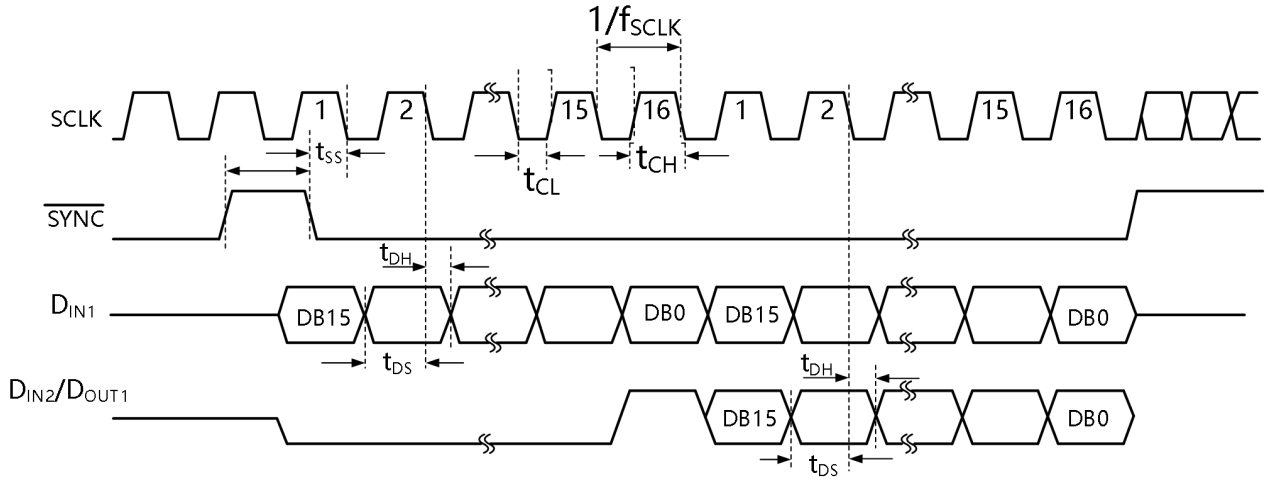

Figure 13. serial interface timing

Take writing a frame of data as an example. When the SYNC signal is pulled down, the chip write operation starts to be executed, and the data input in DIN is synchronized to the shift register through the falling edge of SCLK. In order to avoid clock errors, it is necessary to ensure the establishment time between the falling edge of sync and the falling edge of clock (timing relationship between SYNC and SCLK). When the 16th clock falling edge of SCLK arrives, the last bit data is written to the shift register. At this time, the SYNC signal becomes high and the chip starts programming operation (channel selection, mode selection and register content change, etc.). The falling edge of the clock after the sync signal becomes high will not affect the chip.

If SYNC goes high before the falling edge of the 15th clock, the write sequence operation data in the shift register will be considered invalid. When the clock edge exceeds 17 falling edges, the data of DIN will be output successively on the DOUT port. For more information on this operation mode, refer to daisy chain operation mode.

When DIN is high, the input driver needs to consume more current. When the write sequence is valid, DIN should be idle to reduce power consumption. On the other hand, when the daisy chain mode DOUT is effective output, the synchronization frame signal should be in the idle state.

Daisy-Chain Operation Mode

Daisy chain operation mode allows a single serial controller to operate multiple chips at the same time, thereby reducing the number of signal lines and simplifying the connection. In daisy chain working mode, all chips share SYNC and SCLK signals, and the DOUT signal of the previous chip is connected to the DIN of the next chip. When the serial interface receives data, it still takes the frame as the unit. When the data length exceeds one frame, the chip will successively output the data of the previous frame from the DOUT port to the subsequent chip while receiving the current frame, and then serve as the data input of the subsequent chip. When the rising edge of SYNC signal arrives, all chips will update the currently received frame data to the serial input register at the same time.

Take the three-chip daisy chain as an example. The connection is shown in Figure 14. The DOUT of DAC1 is output to the DIN of DAC2, and the DOUT of DAC2 is output to the DIN of DAC3. The timing when the serial controller sends data is shown in figure 15. When the SYNC signal is low, it sends 3 frames of data and outputs them to DAC3, DAC2 and DAC1 respectively. Pay attention to the data transmission sequence. It should be noted that DOUT is updated at the falling edge of SCLK signal and will be sampled by subsequent chips at the next falling edge of SCLK signal. In order to ensure correct sampling, it is necessary to meet the requirements of DIN signal holding time. Therefore, it is necessary to pay special attention to the delay of SYNC, SCLK, DIN and DOUT signals on the board, and add delay between din and DOUT if necessary.

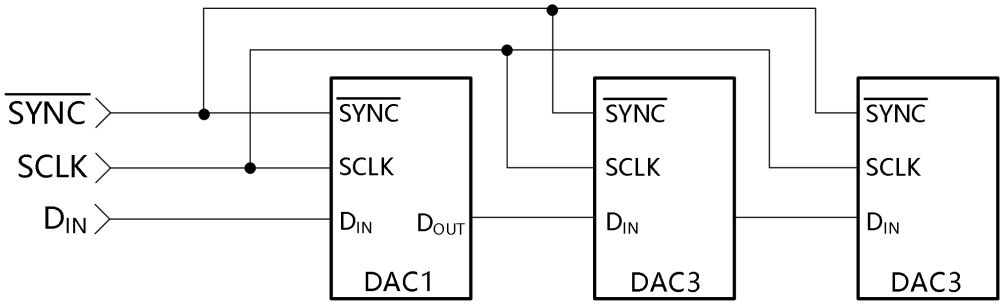

Figure 14. Daisy chain connection

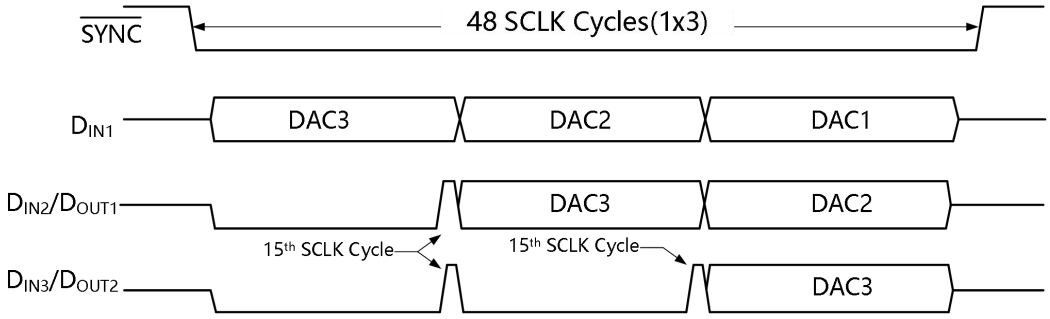

Figure 15. Daisy chain timing

Serial input register

The serial input register takes 16 bits as a frame and is recorded as DB [15:0], in which the first 4 bits DB [15:12] are mode control bits and the last 12 bits DB [11:0] are data bits. The description list of serial input register is shown in Table 6. CD108S085 is 10bitDAC, so when D [15] =0 only D [11:2] in data bit D [11:0] is valid, and the remaining D [1:0] is invalid. D [11] is MSB and D [0] is LSB. DB [15:12] divides the serial input data into four types: write data / DAC register, mode control, special command and standby mode, which correspond to different functions respectively.

Serial input register description

Type	DB[15:12]	DB[11:0]	Description
Sleep Mode	1111	xxxx_HGFEDCBA	When the corresponding bit of DB [7:0] is' 1 ', the corresponding channel enters the sleep state and outputs 2.5k Ω impedance
	1110	xxxx_HGFEDCBA	When the corresponding bit of DB [7:0] is' 1 ', the corresponding channel enters the sleep state and outputs 100k Ω impedance
	1101	xxxx_HGFEDCBA	When the corresponding bit of DB [7:0] is' 1 ', the corresponding channel enters the sleep state and high impedance outputs
Special command	1100	D11 D10 … D1 D0	Broadcast mode: the data registers and DAC registers of all channels are updated to the value of DB [11:0] at the same time.
	1011	D11 D10 … D1 D0	Channel A update: the data register and DAC register of channel A are updated to DB [11:0] at the same time, and the DAC registers of the other seven channels are also updated to the values of the corresponding data registers at the same time.
	1010	xxxx_HGFEDCBA	Update Select: The DAC outputs of the channels selected with a 1 in DB [7:0] are updated simultaneously to the values in their respective control registers.
Mode control	1001	xxxx_xxxx_xxxx	WTM mode command
	1000	xxxx_xxxx_xxxx	WTM mode command
Write data / DAC	0111	D11 D10 … D1 D0	WRM: D [11:0] write to H-channel data register only
Register			WTM: D [11:0] direct update of H-channel DAC register
	0110	D11 D10 … D1 D0	WRM: D [11:0] write to G-channel data register only WTM: D [11:0] direct update of G-channel DAC register

	0101	D11 D10 … D1 D0	WRM: D [11:0] write to F-channel data register only WTM: D [11:0] direct update of F-channel DAC register
	0100	D11 D10 … D1 D0	WRM: D [11:0] write to E-channel data register only WTM: D [11:0] direct update of E-channel DAC register
	0011	D11 D10 … D1 D0	WRM: D [11:0] write to D-channel data register only WTM: D [11:0] direct update of D-channel DAC register
	0010	D11 D10 … D1 D0	WRM: D [11:0] write to C-channel data register only WTM: D [11:0] direct update of C-channel DAC register
	0001	D11 D10 … D1 D0	WRM: D [11:0] write to B-channel data register only WTM: D [11:0] direct update of B-channel DAC register
	0000	D11 D10 … D1 D0	WRM: D [11:0] write to A-channel data register only WTM: D [11:0] direct update of A-channel DAC register

All DAC channels contain two registers: data register and DAC register. Updating the DAC register will directly update the output analog signal of the DAC. The data register temporarily stores the data input by the serial interface. The user can send a command to update the DAC register to the value in the data register. When all data registers are written, the user can send commands to control the output of all DAC channels to update at the same time.

There are two ways to update the serial interface control register: WRM (Write Register Mode) and WTM (Write Through Mode). When writing data / DAC register, only data register is updated in WRM mode, and data register and DAC register are updated at the same time in WTM mode. There are three special commands for serial input: update selection, A-channel update and broadcast mode. The update selection command can selectively update the DAC register of a channel, and then update the output of the DAC; Channel A update command updates the DAC output of all channels while writing channel A data; The broadcast command can update the data registers and DAC registers of all channels to the same value at the same time.

Sleep mode

The 8-channel DAC of CD128S085/CD108S085 can be configured as sleep mode separately. The sleep mode is completed by setting the serial input register, setting DB [15:12] as the required sleep mode, and setting the corresponding bit of the channel requiring sleep to "1". When all 8-channel DACs sleep, the bias circuit inside the chip also sleeps. However, the power-off reset circuit inside the chip is still working normally, and the typical value of current consumption is about 10uA.

Power on / power off reset

CD128S085/CD108S085 contain both power on reset and power off reset circuits. The reset circuit controls the output of all channels at the same time. After reset, the data / DAC registers of all channels are set to all 0, and the final output of DAC is also 0 level. When the power supply

voltage rises to the minimum working voltage of the chip, a reset operation is generated, and the waveform is shown in figure 10. Power off reset occurs in the process of chip power off. When the power supply voltage is lower than about 2.7V, a reset operation is generated. The waveform is shown in Figure 11.

Outline Dimensions

TSSOP16

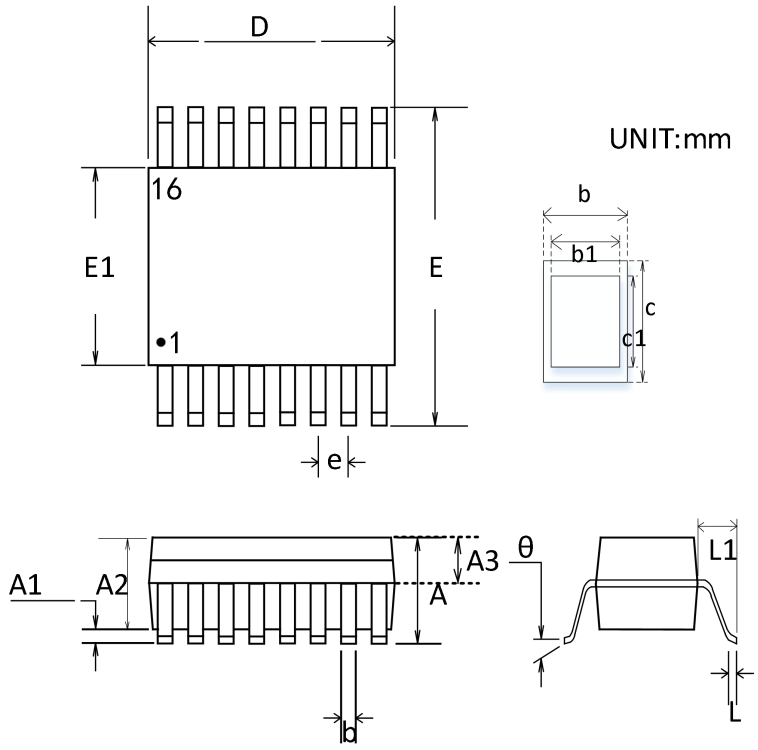

Figure 16. 16-Lead Lead Frame Chip Scale Package [TSSOP]

SYBMOL	MILLIMETER	
	MIN	MAX
A	--	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.19	0.30
b1	0.19	0.25
c	0.13	0.19

c1	0.12	0.14
D	4.9	5.1
E	6.2	6.6
E1	4.3	4.5
e	0.65 BSC	
L	0.45	0.75
L1	1.00 BSC	
θ	0	8°

QFN-16

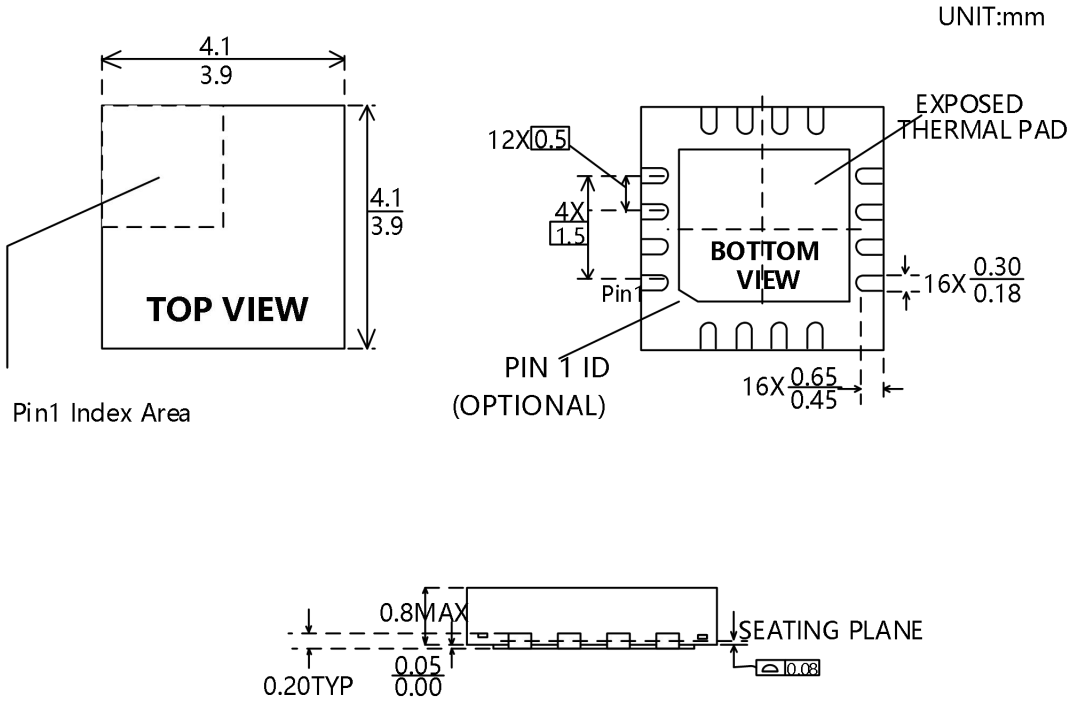

Figure 17. 16-Lead Lead Frame Chip Scale Package [QFN]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD108S085QS	-40℃~125℃	QFN16	Tape and Reel, 2500
CD108S085TS	-40℃~125℃	TSSOP16	Tape and Reel, 2500
CD108S085TS-RL	-40℃~125℃	TSSOP16	Tape and Reel, 3000
CD108S085TS-REEL	-40℃~125℃	TSSOP16	Tape and Reel, 4000
CD128S085QS	-40℃~125℃	QFN16	Tape and Reel, 2500
CD128S085TS	-40℃~125℃	TSSOP16	Tape and Reel, 2500
CD128S085TS-RL	-40℃~125℃	TSSOP16	Tape and Reel, 3000
CD128S085TS-REEL	-40℃~125℃	TSSOP16	Tape and Reel, 4000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.8.4	Initial version	Regular update	WW	LYL	

Chinese version:CD108S085/CD128S085