CoreadDvices
承芯微电子

CD53D04_CD53D14_CD53D24

2.5 V to 5.5 V, 500 µA, 4-channel, voltage output, 8/10/12-bit DAC

Version: Rev 1.0.0 Date: 2025-7-1

Features

- CD53D04: 4 buffered 8-Bit DACs in MSOP-10,QFN package
- CD53D14: 4 buffered 10-Bit DACs in MSOP-10,QFN package
- CD53D24: 4 buffered 12-Bit DACs in MSOP-10,QFN package
- Low power operation: 500uA @ 3V,
- 600uA @ 5V
- 2.5V to 5.5V power supply
- Power-down to 80nA @ 3V,200nA @
- Double-buffered input logic
- Output range:0V to VREF
- Power-on reset to 0V
- On-chip, rail-to-rail output buffer
- Temperature range -40℃ to +105℃

Application

- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators
- Industrial process controls

Description

The CD53D04/CD53D14/CD53D24 are quad 8-, 10- and 12-bit buffered voltage output DACs in MSOP10 packages that operate from a single 2.5V to 5.5V supply, consuming only 500uA at 3V. They have on- chip rail-to-rail output amplifiers with slew rate of 0.7V/us. A 3-wire serial interface compatible with standard SPI, QSPI, MICROWIRE, and DSP interface standards is used, which can operates at clock rates up to 30MHz.

The references for the four DACs are derived from one reference pin. The outputs of all DACs can be updated simultaneous. It incorporate a power-on reset circuit, and ensure that the DAC outputs power up to 0V and remains there until a valid write takes place to the device. The parts contain a power- down feature that reduces the current consumption to 200nA@5V (80nA @ 3V).

Contents

Features ..... - 1 -
Application ..... - 1 -
Description ..... - 1 -
Functional Block Diagram ..... - 3 -
Typical Application Circuit ..... - 3 -
Absolute Maximum Ratings ..... - 4 -
Recommended Operating Range ..... - 4 -
Specifications ..... - 4 -
Pin Configurations and Function Descriptions ..... - 9 -
Typical Performance Characteristics ..... - 11 -
Functional Description ..... - 12 -
The 3-wire serial interface ..... - 13 -
Outline Dimensions ..... - 17 -
Package/Ordering Information ..... - 19 -
Revision Log ..... - 20 -

Chinese version:CD53D04_CD53D14_CD53D24

Functional Block Diagram

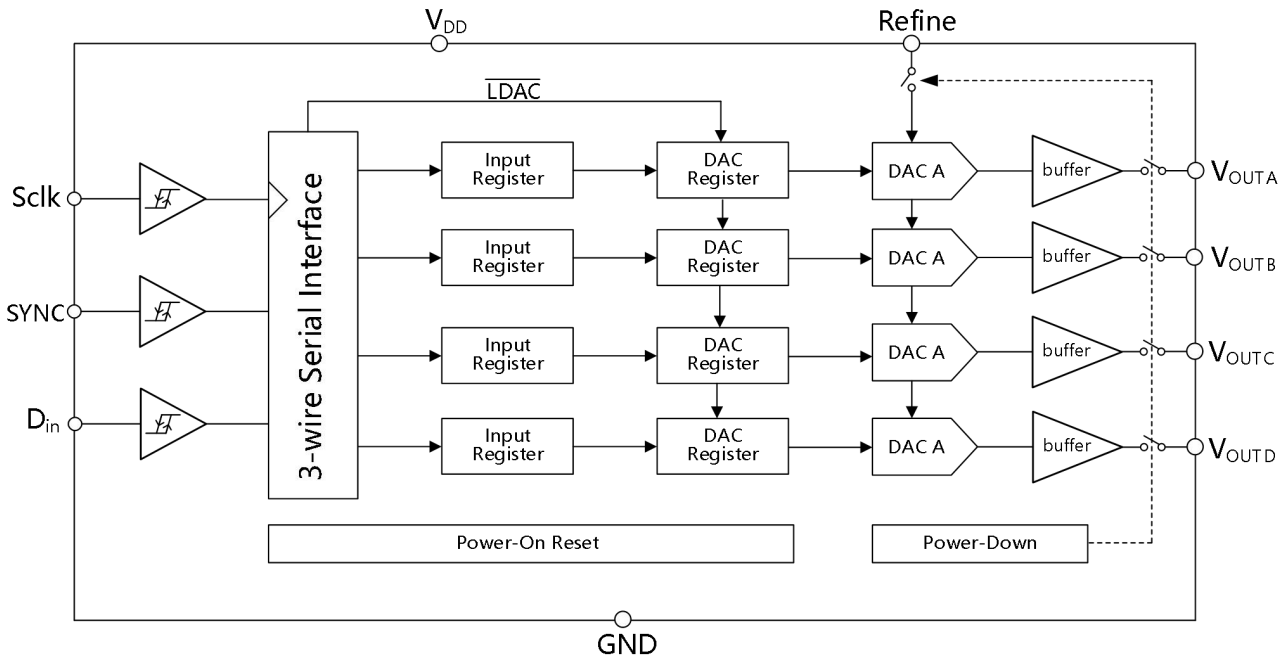


Figure 1. Functional Block Diagram

Typical Application Circuit

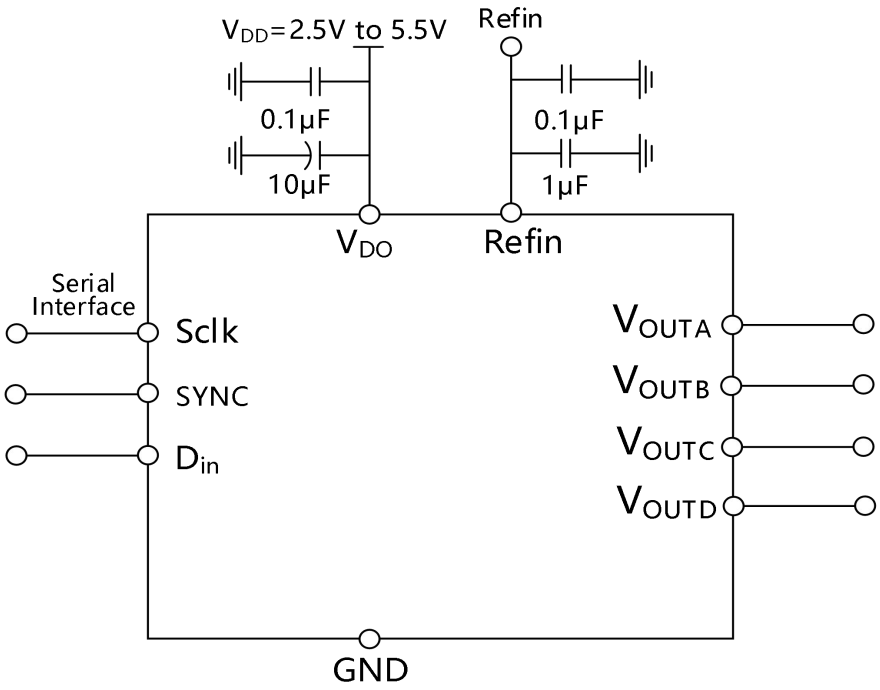


Figure 2 CD53D04/CD53D14/CD53D24 Typical Application Circuit

Absolute Maximum Ratings

(T_A=25℃,unless otherwise noted.)

Parameter 1	Symbol	Value
V_{DD} to GND	V_{DDabs}	-0.3V to+7V
Digital Input Voltage to GND	V_{Digabs}	-0.3V to V_{DD}+0.3V
Reference Input Voltage to GND	V_{refabs}	-0.3V to V_{DD}+0.3V
V_{OUT}A through V_{OUT}D to GND	V_{outabs}	-0.3V to V_{DD}+0.3V
Operating Temperature Range		
Industrial	T_P	-40℃ to +105℃
Storage Temperature Range	T_S	-65℃ to +150℃
Junction TemperatureT_J max	T_{JMAX}	150℃
Reflow Soldering		
Peak Temperature(Pb-free)		260℃
Peak Temperature(non Pb-free)		220℃
Time at Peak Temperature		10 sec to 40 sec

Recommended Operating Range

Parameter	Symbol	Range		Unit
		Min	Max	
Power supply	V_{DD}	2.5	5.5	V
Current dissipation	I_{DD}	400u	600u	A
Ambient Temperature	T_a	-40	105	℃

Specifications

(V_{DD}=2.5V to 5.5V; V_{REF}=2V; R_L=2KΩ to GND ; C_L=200pF to GND; T_A=25℃; unless otherwise noted.)

Parameter	Sym	Test Condition	Version A			Version B			Unit
			Min	Typ	Max	Min	Typ	Max	
DC Performance[1,2]									
CD53D04									
Resolution	Res_N	Monotonic	8			8			Bits

Relative Accuracy	INL	Guaranteed		±0.15	±1.15		±0.15	±0.625	LSB
Differential Non linearity	DNL			±0.02	±0.25		±0.02	±0.25	LSB
CD53D14									
Resolution	Res_N	Monotonic Guaranteed	10			10			Bits
Relative Accuracy	INL			±0.5	±4.05		±0.5	±2.5	LSB
Differential Non linearity	DNL			±0.05	±0.5		±0.05	±0.5	LSB
CD53D24									
Resolution	Res_N	Monotonic Guaranteed	12			12			Bits
Relative Accuracy	INL			±2	±16.05		±2	±10	LSB
Differential Non linearity	DNL			±0.2	±1		±0.2	±1	LSB
Offset Error				±0.4	±3		±0.4	±3	%of FSR
Gain Error				±0.15	±1		±0.15	±1	%of FSR
Lower Dead Band		Lower dead band exists only if offset error is negative					20		mV
DC Power Supply Rejection Ratio[3]	PSRR	$\triangle V_{DD}$=±10%		-60			-60		dB
DC Crosstalk[3]		R_L=2KΩ to (GND) or V_{DD}		200			200		uV
Reference Input[3]									
VREF Input Range			0.25		V_{DD}	0.25		V_{DD}	V
VREF Input Impedance			37	45		37	45		KΩ
Reference		Frequency=10KHz		-90			-90		dB

Feed through									
Output Characteristics[3]									
Minimum Output Voltage[4]				0.001			0.001		V
Maximum Output Voltage[4]				V_{DD}-0.001			V_{DD}-0.001		V
DC Output Impedance				0.5			0.5		Ω
Short Circuit Current		V_{DD}=5V		25			25		mA
		V_{DD}=3V		16			16		mA
Power-Up Time		Coming out of powerdown mode VDD = 5 V		5			5		μs
		Coming out of powerdown mode VDD = 3V		2.5			2.5		μs
Logic Input[3]									
Input Low Voltage Input	V_{IL}	VDD = 5 V ± 10%			0.8			0.8	V
		VDD = 3 V ± 10%			0.6			0.6	V
		VDD =2.5 V ± 10%			0.5			0.5	V
High Voltage Pin	V_{IH}	VDD = 5 V ± 10%	2.4			2.4			V
		VDD = 3 V ± 10%	2.1			2.1			V
		VDD =2.5 V ± 10%	2.0			2.0			V
Capacitance				3			3		pF
Power Requirements									
Power supply	V_{DD}					2.5		5.5	V
I_{DD} (Normal Mode)[4]									
V_{DD}=4.5V to 5.5V		V_{IH}=V_{DD} and V_{IL}=GND		600	900		600	900	uA

V_{DD}=2.5V to 3.6V		V_{IH}=V_{DD} and V_{IL}=GND		500	700		500	700	uA
I_{DD} (Power-Down Mode)									
V_{DD}=4.5V to 5.5V		V_{IH}=V_{DD} and V_{IL}=GND		0.2	1		0.2	1	uA
V_{DD}=2.5V to 3.6V		V_{IH}=V_{DD} and V_{IL}=GND		0.08	1		0.08	1	uA

1. DC specifications tested with the outputs unloaded.
2. Linearity is tested using a reduced code range: CD53D04 (Code 8 to Code 248); CD53D14 (Code 28 to Code 995); CD53D24 (Code 115 to Code 3981).
3. Guaranteed by design and characterization, not production tested.
4. For the amplifier output to reach its minimum voltage, offset error must be negative. For the amplifier output to reach its maximum voltage, VREF=V_{DD} and offset plus gain error must be positive.
5. I_{DD} specification is valid for all DAC codes; interface inactive; all DACs active; load currents excluded.

AC characteristic

(V_{DD}=2.5V to 5.5V; V_{REF}=2V; R_L=2KΩ to GND ; C_L=200pF to GND; Ta=25℃; unless otherwise noted.)

Parameter1	Sym	Test Condition	Min	Typ	Max	Unit
Output Voltage Setting Time						
CD53D04		1/4 scale to 3/4 scale change(0x40 to 0xC0)		6	8	uS
CD53D14		1/4 scale to 3/4 scale change(0x100 to 0x300)		7	9	uS
CD53D24		1/4 scale to 3/4 scale change(0x400 to 0xC00)		8	10	uS
Slew Rate				0.7		V/uS
Major-Code Transition Glitch Energy		1 LSB change around major carry		12		nV-sec
Digital Feedthrough				1		nV-sec
Digital Crosstalk				1		nV-sec
DAC-to-DAC Crosstalk				3		nV-sec
Multiplying Bandwidth		V_{REF}=2V±0.1V_{P-P}		200		kHz
Total Harmonic Distortion		V_{REF}=2.5V±0.1V_{P-P}; Frequency=10KHz		-70		dB

1. Guaranteed by design and characterization, not production tested.

Timing Characteristics

V_{DD} = 2.5V to 5.5V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter1, 2, 3	Limit at TMIN, TMAX		Unit	Test Conditions/Comments
	VDD=2.5V to 3.6V	VDD=3.6V to 5.5V		
t_1	40	33	ns min	SCLK cycle time
t_2	16	13	ns min	SCLK high time
t_3	16	13	ns min	SCLK low time
t_4	16	13	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	5	ns min	Data setup time
t_6	4.5	4.5	ns min	Data hold time
t_7	0	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	80	33	ns min	Minimum $\overline{SYNC}$ high time

1. Guaranteed by design and characterization, not production tested.
2. All input signals are specified with tr = tf = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
3. See Figure 3.

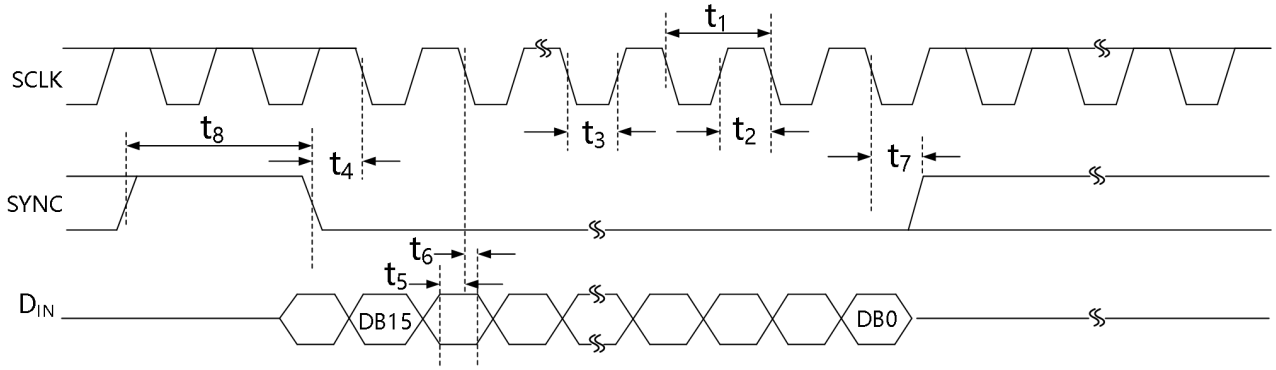


Figure 3. Serial Interface Timing Diagram

Pin Configurations and Function Descriptions

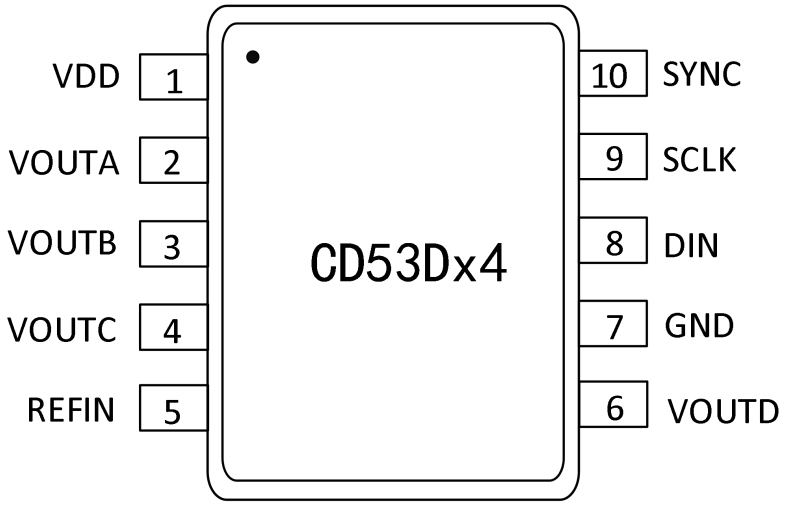


Figure 2. TSSOP-16 pin configuration

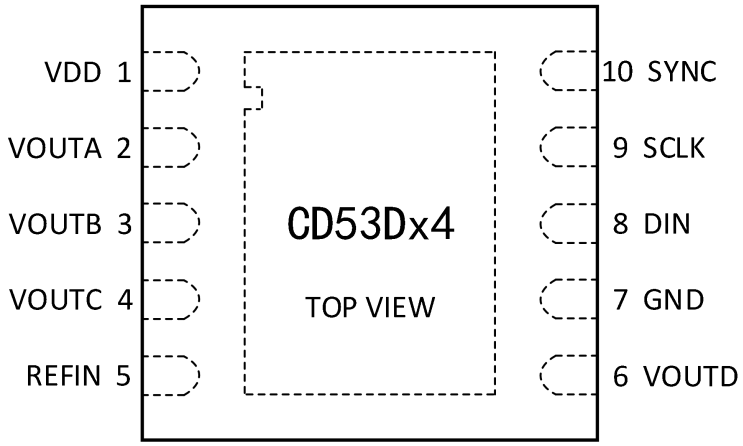


Figure 3. QFN-16 pin configuration

Pin Function Descriptions

Pin Name	Pin No.	Function	Description
VDD	1	Power	Power Supply Input. These parts can be operated from 2.5V to 5.5V and the supply can be decoupled to GND.
VOUTA	2	O	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
VOUTB	3	O	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
VOUTC	4	O	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
REFIN	5	I	Reference Input Pin for All Four DACs. It has an input range from 0.25V to V_{DD}.

VOUTD	6	O	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
GND	7	Ground	Ground Reference Point for All Circuitry on the Part.
DIN	8	I	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The Din input buffer is powered down after each write cycle.
SCLK	9	I	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock speeds up to 30MHz. The Sclk input buffer is powered down after each write cycle.
SYNC	10	I	Active Low Control Input. This is the frame synchronization signal for the input data. When goes low, it enables the input shift register and data is transferred in on the falling edges of the following 16clocks. If SYNC is taken high before the 16^{th} falling edge of Sclk, the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the device.

I：Input, O：Output

Typical Performance Characteristics

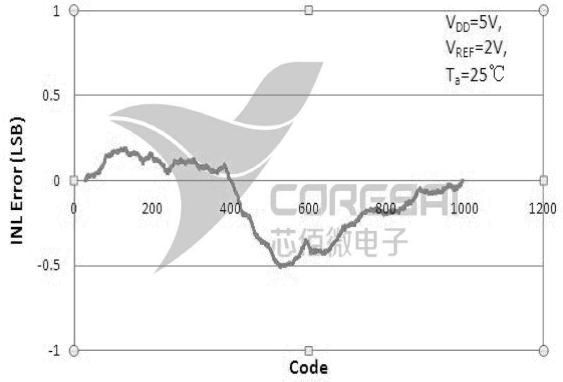


Figure 6. CD53D14 Typical INL Plot

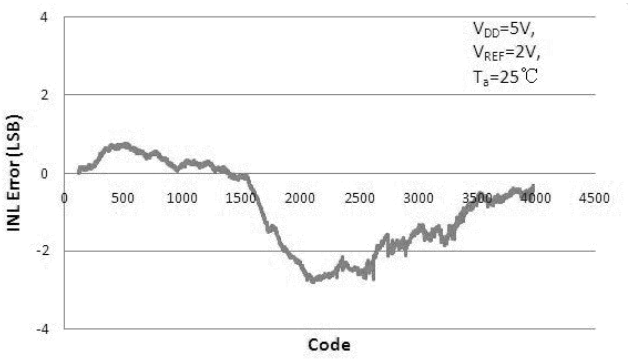


Figure 7. CD53D24 Typical INL Plot

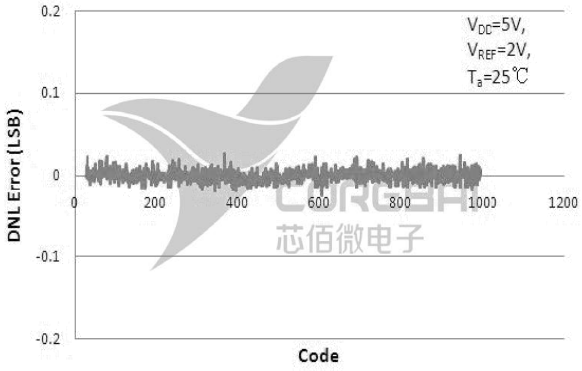


Figure 8. CD53D14 Typical DNL Plot

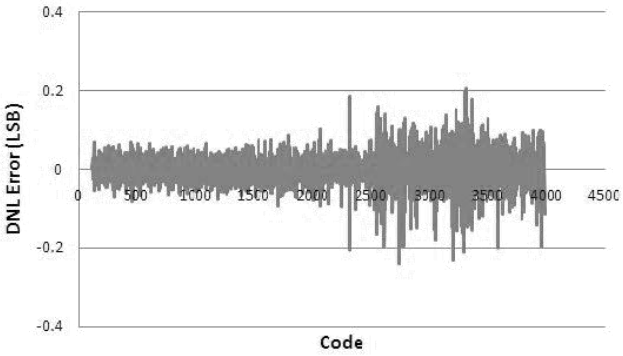


Figure 9. CD53D24 Typical DNL Plot

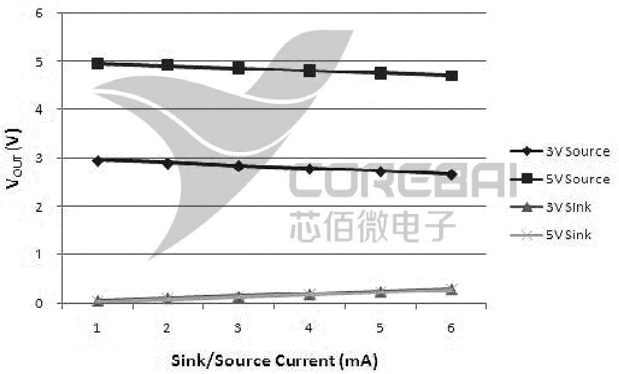


Figure 10. Vout Source and Sink Current Capability

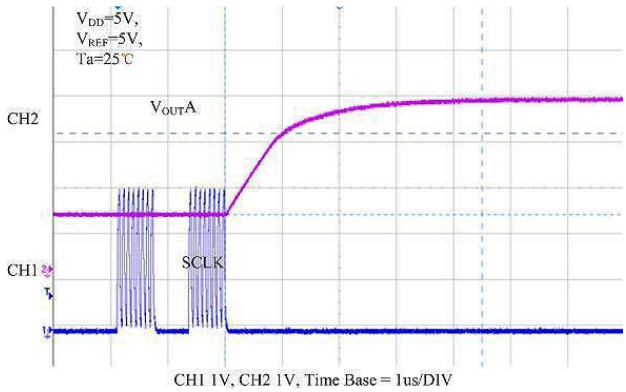


Figure 11. Half-scale setting
(0.25 to 0.75 Scale Code Change)

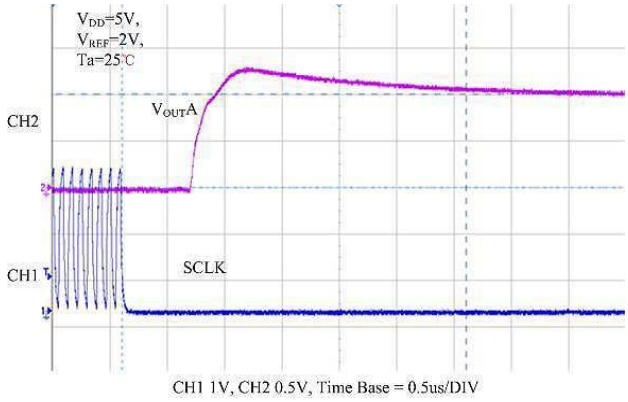


Figure 12. Exiting Power-down to Midscale

Functional Description

The CD53D04/CD53D14/CD53D24 are quad, resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10 and 12 bits, respectively. Each contains four output buffer amplifiers and is written to via a 3-wire serial interface. They operate from single supplies of 2.5V to 5.5V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/us. The four DACs share a single reference input pin. The devices have programmable power-down modes, in which all DACs can be turned off completely with a high impedance output.

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the Refin pin provides the reference voltage for the DAC. The input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N} \quad \text{.....Formula 1}$$

Where D=decimal equivalent of the binary code that is loaded to the DAC register: 0–255 for CD53D04 (8 bits)

0—1023 for CD53D14(10 bits)

0—4095 for CD53D24(12bits)

N=DAC resolution.

There is a single reference input pin for the four DACs. The reference input is not buffered. The user can have a reference voltage as low as 0.25V or as high as VDD because there is no restriction due to the headroom or foot room requirements of any reference amplifier. It is recommended to use a buffered reference in the external circuit. The input impedance is typical 45kΩ.

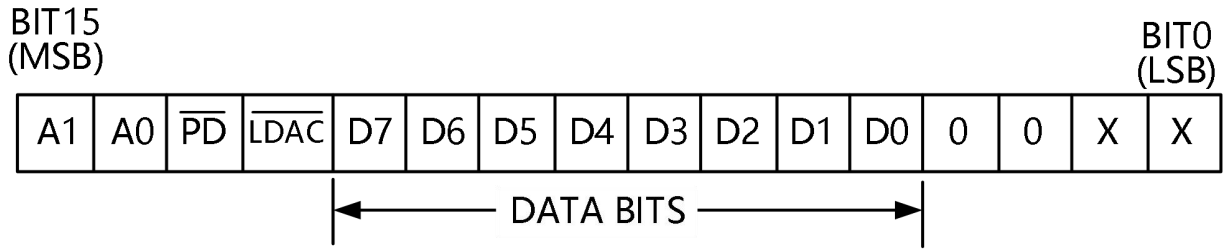
The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to VDD when the reference is VDD. It is capable of driving a load of 2kΩ to GND or VDD , in parallel with 500pF to GND or VDD. The slew rate is 0.7V/us with a half-scale

settling time to ±0.5LSB(at 12 bits) of 8us.

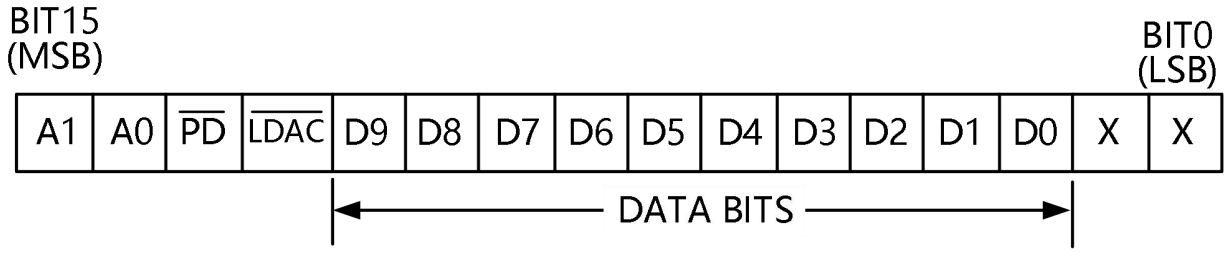
The CD54D04/CD53D14/CD53D24 are provided with a power-on reset function, so that they power up in a defined state. The power-on state uses normal operation and an output voltage set to 0V. Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device.

The CD54D04/CD53D14/CD53D24 are controlled over a versatile, 3-wire serial interface that operates at clock rates up to 30MHz and are compatible with SPI,QSPI,MICROWIRE, and DSP interface standards.

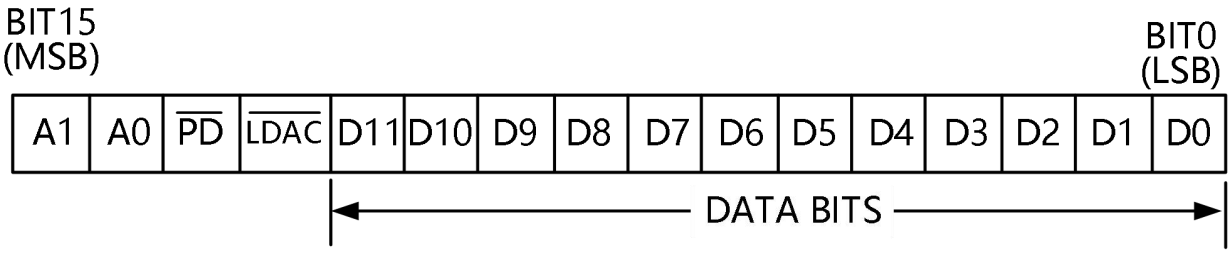
The 3-wire serial interface



(a). CD53D04 Input Shift Register Contents



(b). CD53D14 Input Shift Register Contents



(c). CD53D24 Input Shift Register Contents

Figure42. CD53D04/CD53D14/CD53D24 Input Shift Register Contents

Input Shift Register

The input shift register is 16 bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, Sclk. The 16-bit word consists of four control bits followed by 10 or 12 bits of DAC data, depending on the device type. Data is loaded MSB first (Bit15) and the first

two bits determine whether the data is for DAC A ,DAC B ,DAC C, or DAC D. Bit 13 and Bit 12 control the operating mode of the DAC. Bit 13 is $\overline{PD}$, and determines whether the part is in normal or power-down mode. Bit 12 is $\overline{LDAC}$, and controls when DAC registers and outputs are updated.

Table 6 (Address Bits)

A1	A0	DAC Addressed
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

Address and Control Bits

$\overline{PD}$ 0: All four DACs go into power-down mode, consuming only 200nA @ 5V. The DAC outputs enter a high impedance state.

1: Normal operation.

$\overline{LDAC}$ 0: All four DAC registers and, therefore, all DAC outputs updated simultaneously on completion of the write sequence.

1: Only addressed input register is updated. There is no change in the content of the DAC registers.

The CD53D24 uses all 12 bits of DAC data; the CD53D14 uses 10 bits and ignores the 2 LSB Bits. The CD53D04 uses 8 bits and ignores the last four bits. The data format is straight binary, with all 0s corresponding to 0V output and all 1s corresponding to full-scale output (VREF-1LSB).

The Sync input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can be transferred into the device only while Sync is low. To start the serial data transfer, take Sync low. After Sync goes low, serial data shifts into the device's input shift register on the falling edges of Sclk for 16 clock pulses. Any data and clock pulses after the 16th falling edge of Sclk are ignored because the Sclk and Din input buffers are powered down. No further serial data transfer occurs until Sync is taken high and low again. Sync can be taken high after the falling edge of the 16th Sclk pulse.

After the end of the serial data transfer, data automatically transfers from the input shift register to the input register of the selected DAC. If Sync is taken high before the 16th falling edge of Sclk, the data transfer is aborted and the DAC input registers are not updated.

When data has been transferred into three of the DAC input registers, all DAC registers and all DAC outputs are simultaneously updated by setting LDAC low when writing to the remaining DAC input register.

Low Power Serial Interface

To reduce the power consumption of the device even further, the interface fully powers up only when the device is being written to, that is , on the falling edge of Sync. As soon as the 16-bit control word has been written to the part, the Sclk and Din input buffers are powered down.They power up again only following a falling edge of Sync.

Double-Buffered Interface

The CD53D04/CD53D14/CD53D24 DACs have double-buffered interfaces consisting of two banks of registers - input registers and DAC registers. The input register is directly connected to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC register contains the digital code used by the resistor string.

Access to the DAC register is controlled by the LDAC bit. When the LDAC bit is set high, the DAC register is latched and hence the input register can change state without affecting the contents of the DAC register. However, when the LDAC bit is set low, all DAC registers are update after a complete write sequence.

This is useful if the user requires simultaneous updating of all DAC outputs. The user can write to three of the input registers individually and then, by setting the LDAC bit low when writing to the remaining DAC input register, all outputs update simultaneously.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been update since the last time that LDAC was brought low. Normally, when LDAC is brought low, the DAC registers are filled with the contents of the input register. In the case of the CD53D04/CD53D14/CD53D24 the part updates the DAC register only if the input register has been changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

Power-Down Mode

The CD53D04/CD53D14/CD53D24 have low power consumption, dissipation only 1.5mW with a 3V supply and 3mW with a 5V supply. Power consumption can be further reduced when the DACs are not in use by putting them into power-down mode, selected by a 0 on Bit 13 (PD) of the control word.

When the PD bit is set to 1, all DACs work normally with a typical power consumption of 600uA at 5V (500uA at 3V). However, in power-down mode, the supply current falls to 200nA at 5V (80nA at 3V) when all DACs are powered down. Not only does the supply current drop, but also the output stage is internally switched from the output of the amplifier, making it open-circuit. This has the advantage that the output is three-stated while the part is in power-down mode,

and provides a defined input condition for whatever is connected to the output of the DAC amplifier.

The bias generator, the output amplifier, the resistor string, and all other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 5us. This is the time from the falling edge of the 16th Sclk pulse to when the output voltage deviates from its power down voltage.

Typical Application Circuit

The CD53D04/CD53D14/CD53D24 can be used with a wide range of reference voltages where the devices offer full, one-quadrant multiplying capability over a reference range of 0V to VDD. More typically, these devices are used with a fixed, precision reference voltage.

If an output range of 0V to VDD is required, the simplest solution is to connect the reference input to VDD. As this supply is not very accurate and can be noisy, the CD53D04/CD53D14/CD53D24 can be powered from the reference voltage; for example, using a 5V reference. The current required is 600uA supply current and approximately 112uA into the reference input. This is with no load on the DAC outputs. When the DAC outputs are loaded, the reference also needs to supply the current to the loads.

Decoding Multiple CD53D04/CD53D14/CD53D24

The SYNC pin on the CD53D04/CD53D14/CD53D24 can be used in applications to decode a number of DACs. In this application, all the DACs in the system receive the same serial clock and serial data, but SYNC can only be active to one of the devices at any one time, allowing access to only one DAC in this system. The 74HC139 can be used as a 2-to-4-line decoder to address any of the DACs in the system. To prevent timing errors, the enable input must be brought to its inactive state while the coded address inputs are changing state.

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the CD53D04/CD53D14/CD53D24 is mounted is designed so that the analog and digital sections are separated and confined to certain areas of the board. If the CD53D04 / CD53D14/ CD53D24 are in a system where multiple devices require an A_{GND}- to-D_{GND} connection, the connection is made at one point only. The star ground point is established as close as possible to the device.

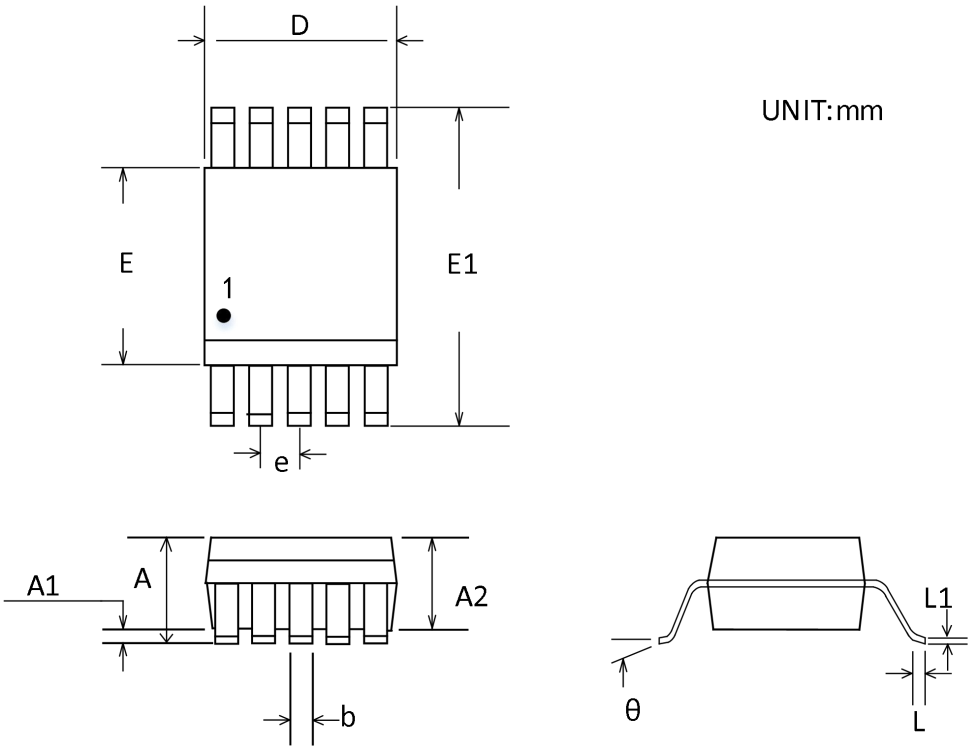
The CD53D04/CD53D14/CD53D24 has ample supply bypassing of 10uF in parallel with 0.1uF on the supply located as close to the package as possible, ideally right up against the device. The 10uF capacitors are the tantalum bead type. The 0.1uF capacitor has low effective series

resistance (ESR) and effective series inductance (ESI).

The power supply lines of the CD53D04/CD53D14/CD53D24 use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks are shielded with digital ground to avoid radiating noise to other parts of the board, and are never run near the reference inputs .Avoid crossover of digital and analog signals. Traces on opposite sides of the board run at right angles to each other. This reduces the effects of feedthrough through the board.

Outline Dimensions

MSOP-10



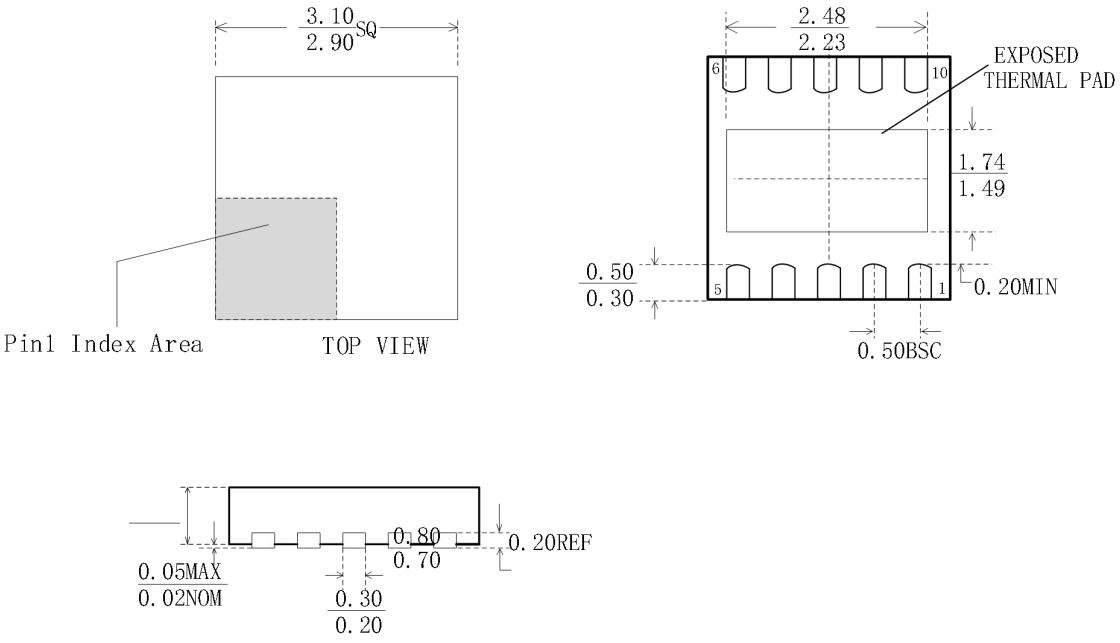
UNIT:mm

SYBMOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.10
A1	0.05	--	0.15
A2	0.75	0.85	0.95
b	0.15	--	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10

E1	4.65	4.90	5.15
e	0.50 BSC		
L	0.40	0.55	0.70
L1	0.13	--	0.23
θ	0	--	6°

QFN-10

UNIT:mm



Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD53D04AMS	-40℃~105℃	MSOP-10	Tape and Reel, 3000
CD53D04BMS	-40℃~105℃	MSOP-10	Tape and Reel, 3000
CD53D04AQF	-40℃~105℃	QFN-10	Tape and Reel, 5000
CD53D04BQF	-40℃~105℃	QFN-10	Tape and Reel, 5000
CD53D14AMS	-40℃~105℃	MSOP-10	Tape and Reel, 3000
CD53D14BMS	-40℃~105℃	MSOP-10	Tape and Reel, 3000
CD53D14AQF	-40℃~105℃	QFN-10	Tape and Reel, 5000
CD53D14BQF	-40℃~105℃	QFN-10	Tape and Reel, 5000
CD53D24AMS	-40℃~105℃	MSOP-10	Tape and Reel, 3000
CD53D24BMS	-40℃~105℃	MSOP-10	Tape and Reel, 3000
CD53D24AQF	-40℃~105℃	QFN-10	Tape and Reel, 5000
CD53D24BQF	-40℃~105℃	QFN-10	Tape and Reel, 5000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.7.1	Initial version	Regular update	WW	LYL	