CoreadDvices
承芯微电子

CD8511_CD8512_CD8514

Precision, Micropower, CMOS, Rail-to-Rail, Input/Output Operational Amplifiers

Version: Rev 1.0.0 Date: 2025-6-3

Features

- Low Offset Voltage: 40uV (Maximum)
- Input Offset Drift: 0.05μV/°C
- High Gain Bandwidth Product: 350KHz
- Rail-to-Rail Input and Output • High Gain,
- High Slew Rate: 0.17V/μs
- Low Noise: 1.6uVp-p (0.01~10Hz)
- Low Power Consumption: 60μA /op amp
- Overload Recovery Time:6us
- Low Supply Voltage: +2.5 V to +5.5 V
- No External Capacitors Required
- Extended Temperature: -40°C to +125°C

Application

- Temperature Sensors
- Medical/Industrial Instrumentation
- Pressure Sensors
- Battery-Powered Instrumentation
- Active Filtering
- Weight Scale Sensor
- Strain Gage Amplifiers
- Power Converter/Inverter

Description

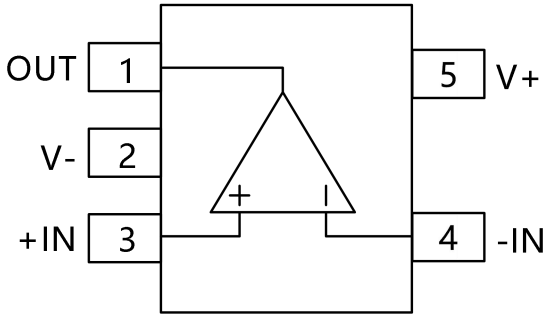
The CD8511, CD8512, CD8513, CD8514(dual version &shutdown) series of CMOS operational amplifiers use auto-zero techniques to simultaneously provide very low offset voltage (40μV max) and near-zero drift over time and temperature. This family of amplifiers has ultralow noise, offset and power.

This miniature, high-precision operational amplifiers offset high input impedance and rail-to-rail input and rail-to-rail output swing. With high gain-bandwidth product of 350KHz and slew rate of 0.17V/μs. Single or dual supplies as low as +2.5V(±1.25V) and up to +5.5V (±2.75V) may be used.

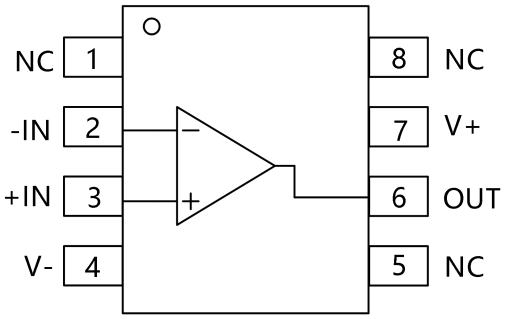
The CD8511, CD8512, CD8513, CD8514 (dual version with shutdown) are specified for the extended industrial and automotive temperature range (-40°C to 125°C). The CD8511 single amplifier is available in 5-lead SOT23, 8-lead MSOP8 and 8-lead SOIC packages, The CD8512 dual amplifier is available in 8-lead SOIC, 8-lead TDFN2x2 and 8-lead TSSOP narrow surface mount packages, The CD8513(dual version with shutdown) comes in Micro-SIZE MSOP10. The CD8514 quad is available in 14-lead SOIC and 14-lead narrow TSSOP packages.

Contents

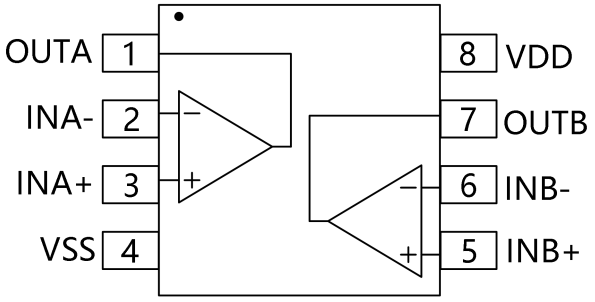
Pin Configurations



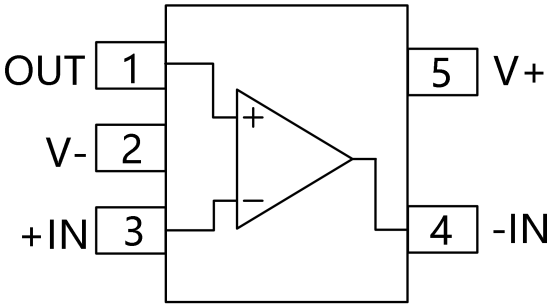
SOT23-5



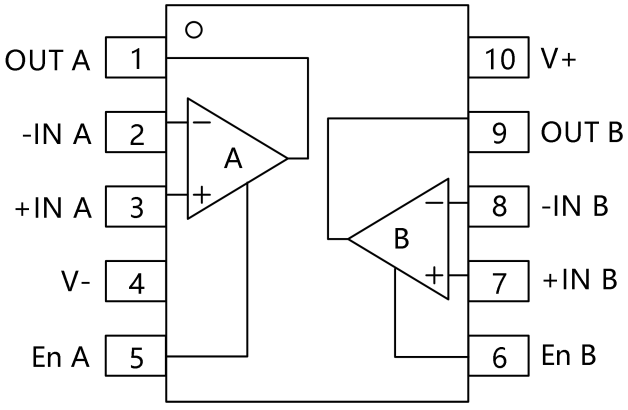
SOIC-8(SOP8) , MSOP-8



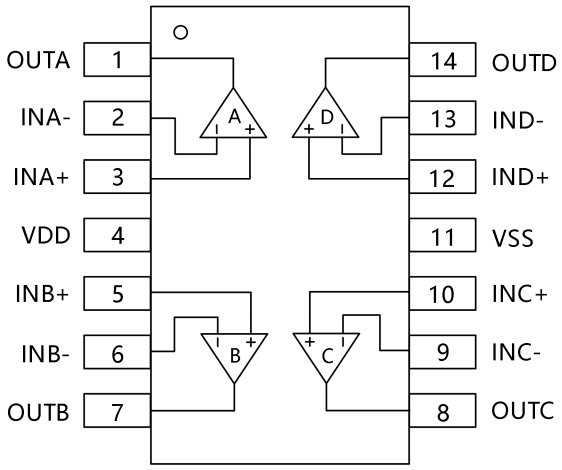
SOIC-8(SOP8),MSOP-8,TDFN2x2-8



SOT23-5



MSOP-10



SOIC-14(SOP14),TSSOP-14

Note : NC indicates no internal connection

Chinese version:CD8511_CD8512_CD8514

Absolute Maximum Ratings

Parameter	Range
Supply Voltage (VS)	7V
Input Voltage	– 0.5 to (V+) + 0.5V
Input Current	±10mA
Storage Temperature Range	−65℃ to +150℃
Operating Temperature Range	−40℃ to +125℃
Junction Temperature Range	−65℃ to +150℃
Lead Temperature (Soldering,10 sec)	300℃
Package Thermal Resistance @ T_A= +25°C	
SOT23-5,SOT23-6	200°C/W
MSOP-10, SOIC-8	150°C/W
SOIC-14, TSSOP-14	100°C/W
HBM	2000V
MM	400V

Electrical characteristics

Boldface limits apply over the specified temperature range, T_A = –40°C to +125°C.(At T_A = +25°C, Vs=5V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.)

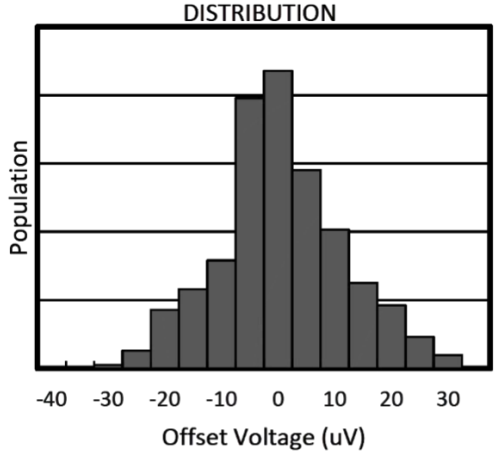
PARAMETER	CONDITION	CD8511 , CD8512 CD8513 , CD8514			
		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Input Offset Voltage (V_{OS})	V_{CM} = Vs/2		7	40	μV
VS Temperature (dVos/dT)			0.05	0.2	μV/℃
VS Power Supply (PSRR)	V_S = +2.5V to +5.5V, V_{CM} = 0	110	130		dB
Channel Separation, dc			0.1		μV/V
INPUT BIAS CURRENT					
Input Bias Current (I_B)	V_{CM} = Vs/2		50		pA
Input Offset Current (Ios)			10		pA
NOISE PERFORMANCE					
Input Voltage Noise (e_np-p)	f=0.01Hz to 10Hz		1.6		μVpp
Input Voltage Noise (e_np-p)	f=0.01Hz to 1Hz		0.48		uVpp
Input Voltage Noise Density (e_n)	f=1KHz		70		$nV/\sqrt{Hz}$

Input Current Noise Density (i_n)	f=10Hz		8		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range (V_{CM})		(V-)-0.1		(V+)+0.1	V
Common-Mode Rejection Ratio (CMRR)	(V–) – 0.1V < V_{CM} < (V+)+ 0.1V	110	130		dB
INPUT CAPACITANCE					
Differential			1		pF
Common-Mode			5		pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain (A_{OL})	R_L=10KΩ, V_O=0.3V to 4.7V, -40°C~125℃	110	130		dB
DYNAMIC PERFORMANCE					
Slew Rate (SR)	G=+1		0.17		V/μs
Gain-Bandwidth Product (GBW)			350		MHz
Overload Recovery Time			6		us
OUTPUT CHARACTERISTICS					
Output Voltage High (V_{OH})	R_L=100 KΩ to GND	4.99	4.998		V
	R_L=10 KΩ to GND	4.95	4.98		V
Output Voltage Low (V_{OL})	R_L=100 KΩ to V+		1	10	mV
	R_L=10 KΩ to V+		10	30	mV
Short-Circuit Current (I_{SC})			25		mA
POWER SUOOLY					
Operating Voltage Range		2.5		5.5	V
Quiescent Current (I_Q)			60	87	mA
SHUTDOWN					
T_{OFF}			2		μs
T_{ON}			1		us
V_L (shutdown)		0		+0.8	V
V_H (amplifier is active)		0.75(V+)		V+	V
Input Bias Current of Enable Pin			50		pA
I_{QSD}			1	5	uA

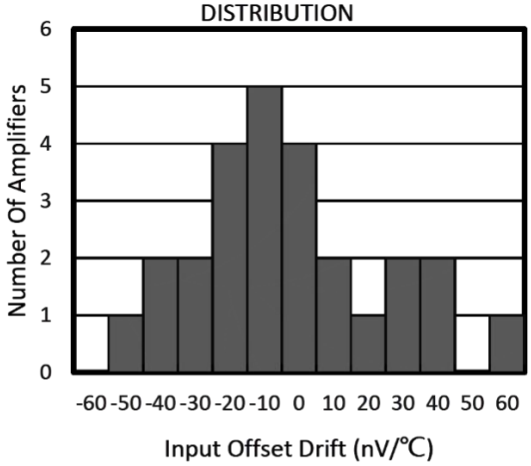
Typical Characteristics

At T_A = +25℃, Vs=5V, R_L = 10kΩ connected to $V_S/2$, V_{OUT} = $V_S/2$, unless otherwise noted.

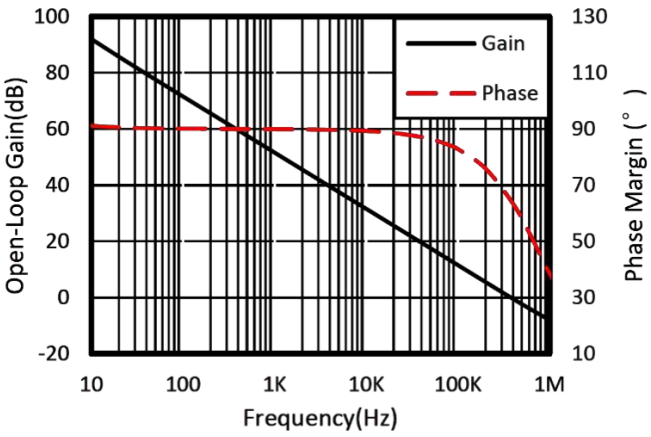
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



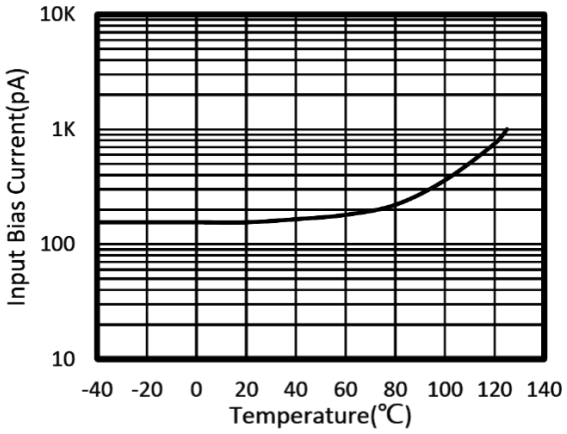
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



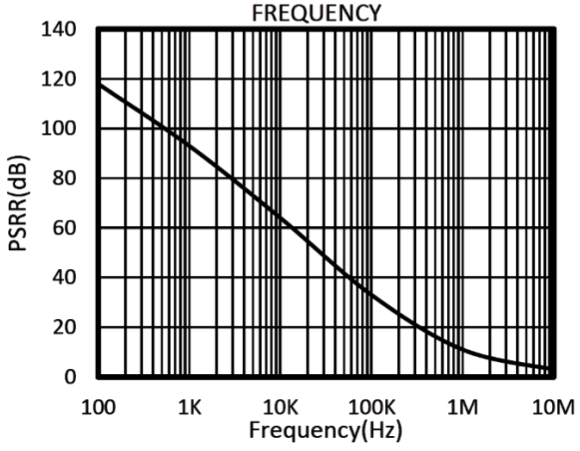
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



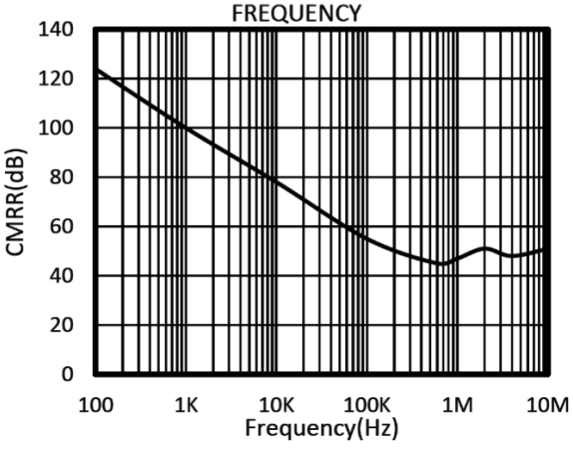
INPUT BIAS CURRENT vs TEMPERATURE



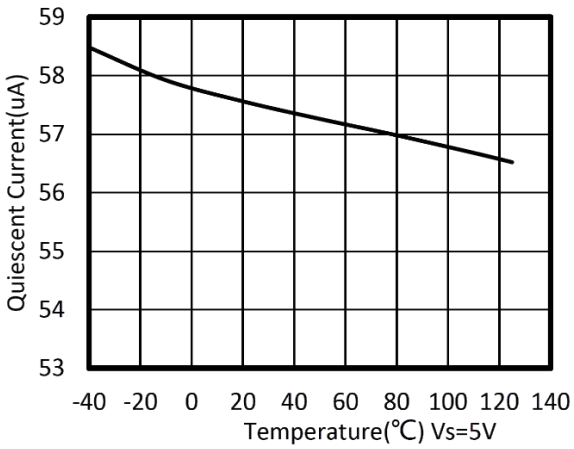
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



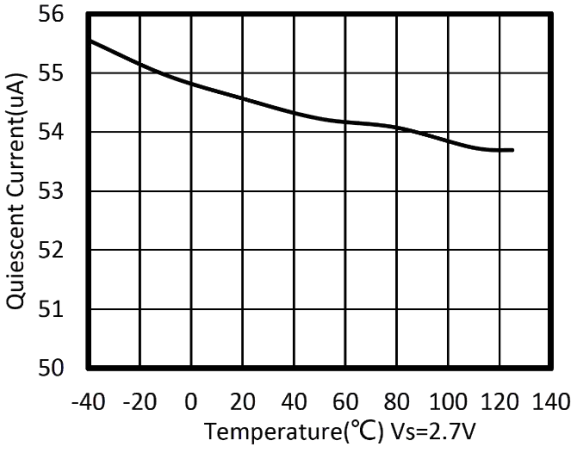
COMMON-MODE REJECTION RATIO vs FREQUENCY



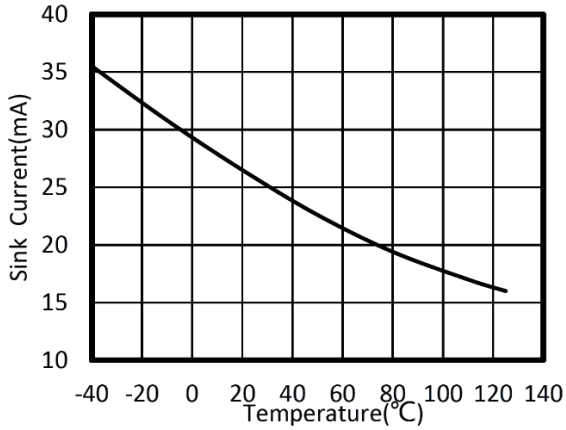
QUIESCENT CURRENT vs TEMPERATURE



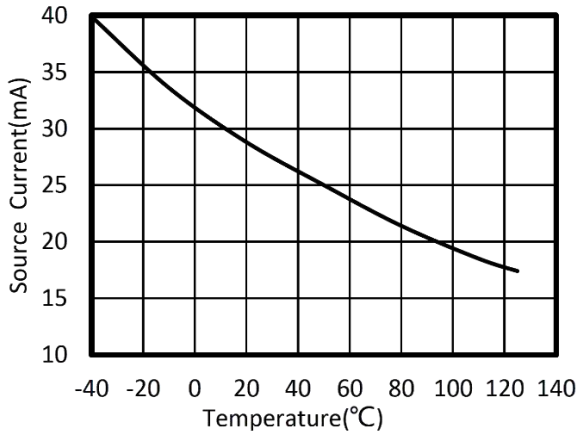
QUIESCENT CURRENT vs TEMPERATURE



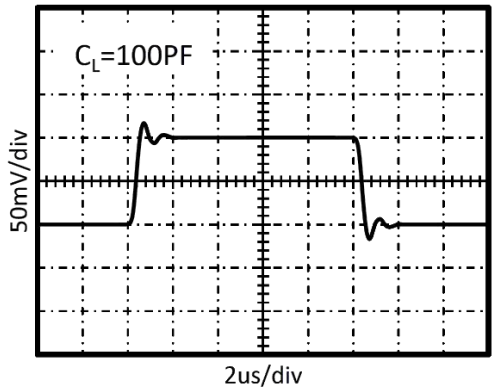
SINK CURRENT vs TEMPERATURE



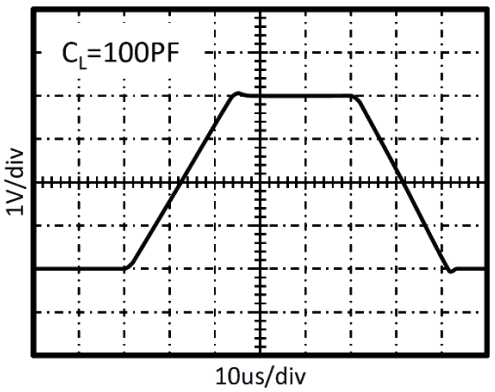
SOURCE CURRENT vs TEMPERATURE



SMALL-SIGNAL STEP RESPONSE

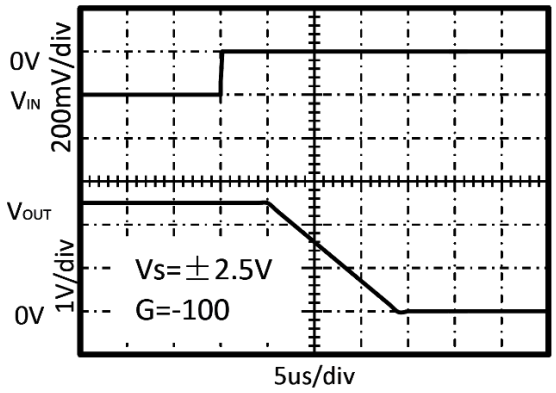


LARGE-SIGNAL STEP RESPONSE

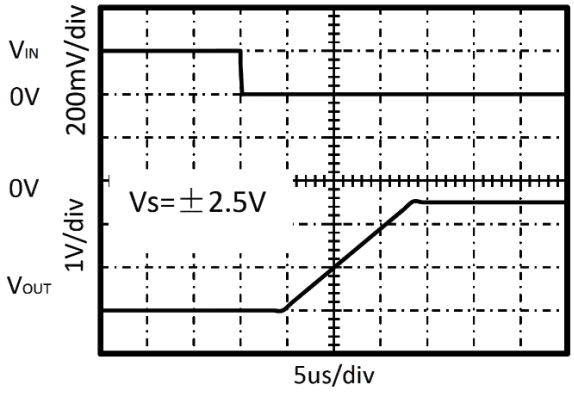


Chinese version:CD8511_CD8512_CD8514

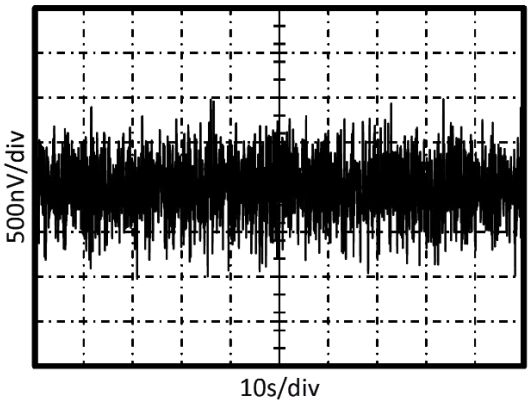
POSITIVE OVERVOLTAGE RECOVERY



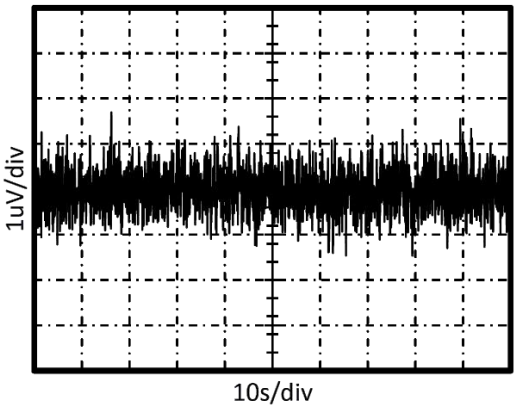
NEGATIVE OVERVOLTAGE RECOVERY



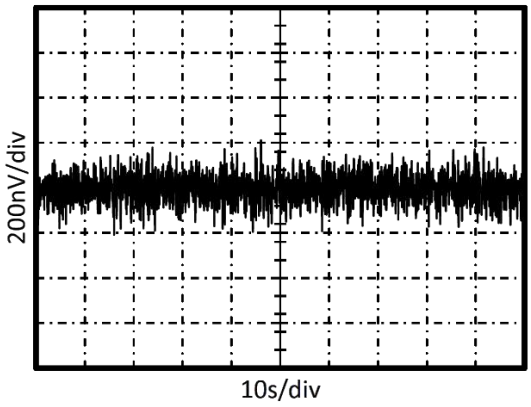
0.01Hz TO 10Hz NOISE AT Vs=5V



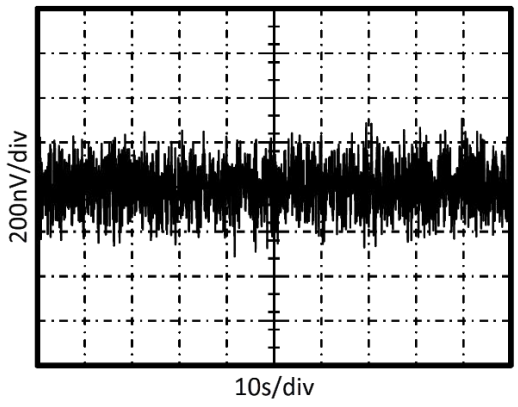
0.01Hz TO 10Hz NOISE AT Vs=2.7V



0.01Hz TO 1Hz NOISE AT Vs=5V



0.01Hz TO 1Hz NOISE AT Vs=2.7V



Chinese version:CD8511_CD8512_CD8514

Application Information

The CD8511, CD8512, CD8513, CD8514 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1μF capacitor placed closely across the supply pins.For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.Use low thermoelectric-coefficient connections (avoid dissimilar metals).Thermally isolate components from power supplies or other heat-sources.Shield op amp and input circuitry from air currents, such as cooling fans.Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1μV/°C or higher, depending on materials used.

Operating Voltage

The CD8511, CD8512, CD8513, CD8514 series op amps operate over a power-supply range of +2.5V to +5.5V (±1.25V to ±2.75V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

CD8513 Enable Function

The enable/shutdown digital input is referenced to the V–supply voltage of the amp. A logic high enables the op amp. A valid logic high is defined as > 75% of the total supply voltage. The valid logic high signal can be up to 5.5V above the negative supply, independent of the positive supply voltage. A valid logic low is defined as<0.8V above the V– supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin must be connected to a valid high or low voltage, or driven, not left open circuit.

The logic input is a high-impedance CMOS input, with separate logic inputs provided on the dual version. For battery operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time includes one full autozero cycle required by the amplifier to return to VOS

accuracy. Prior to this time, the amplifier functions properly, but with unspecified offset voltage. Disable time is 1μs. When disabled, the output assumes a high-impedance state. This allows the CD8513 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.

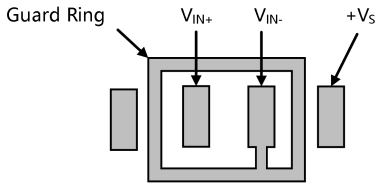
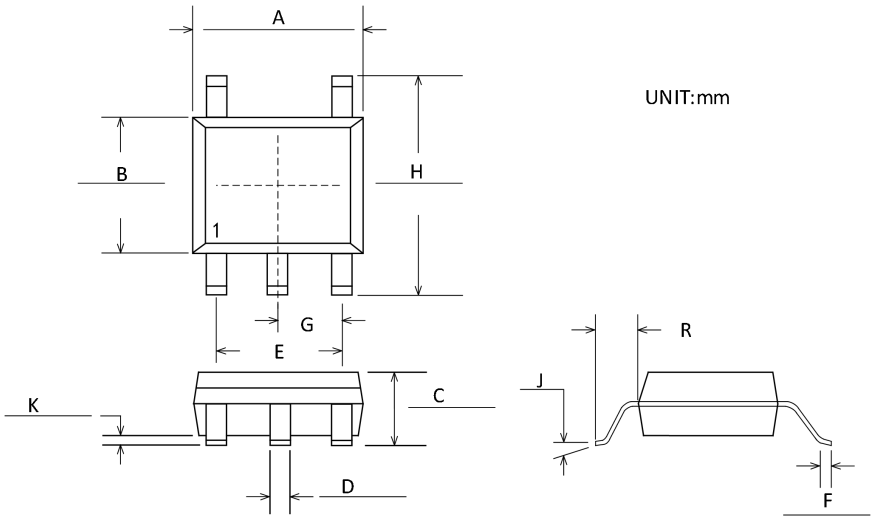


Figure 1. The Layout of Guard Ring

Package Outline Dimensions

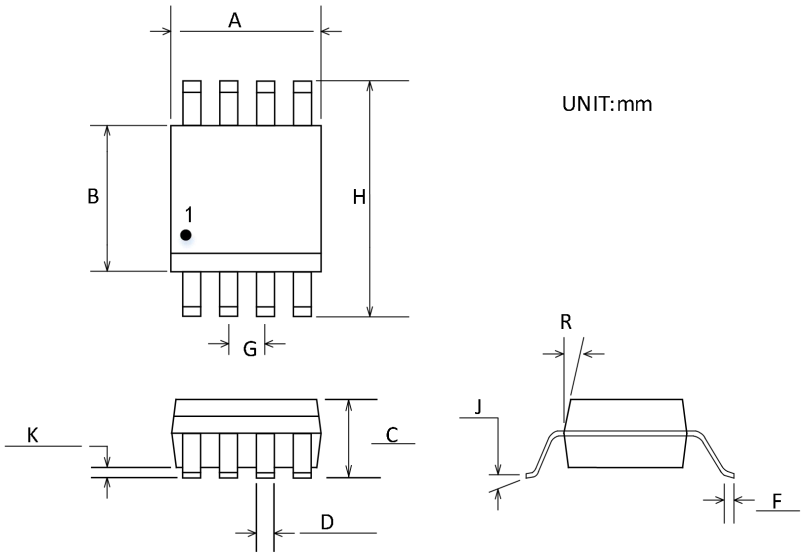
SOT23-5



Symbol	Dimensions In Millimeters	
	Min	Max
A	2.80	3.00
B	1.50	1.70
C	0.95	1.45
D	0.35	0.50
E	1.90BSC	
F	0.35	0.55
G	0.95BSC	
H	2.60	3.00
J	0°	10°
K	0.05	0.15
R	0.60BSC	

Chinese version:CD8511_CD8512_CD8514

MSOP-8

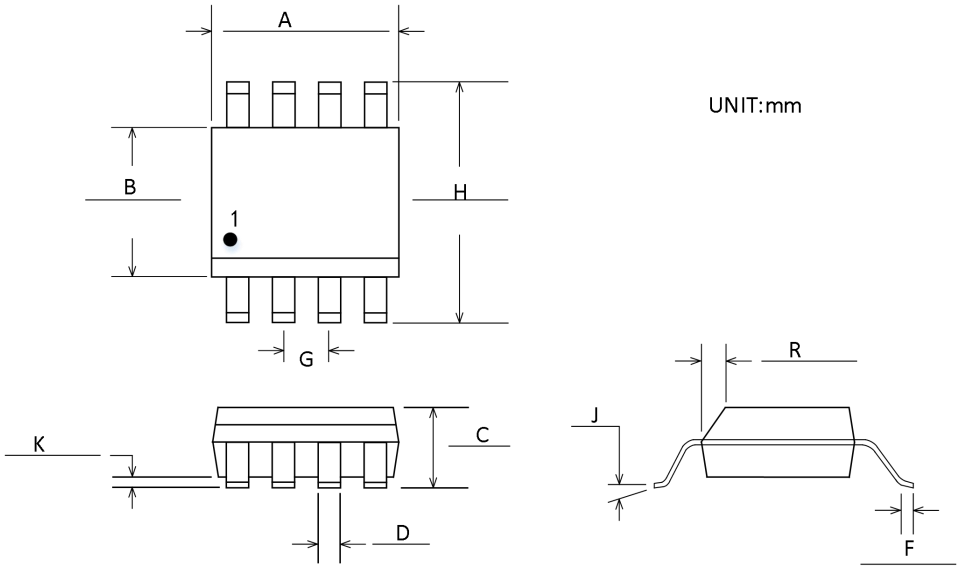


UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	2.80	3.20
B	2.80	3.20
C	1.10MAX	
D	0.25	0.40
F	0.40	0.80
G	0.65BSC	
H	4.65	5.15
J	0°	6°
K	0.05	0.15
R	15°MAX	

Chinese version:CD8511_CD8512_CD8514

SOP-8

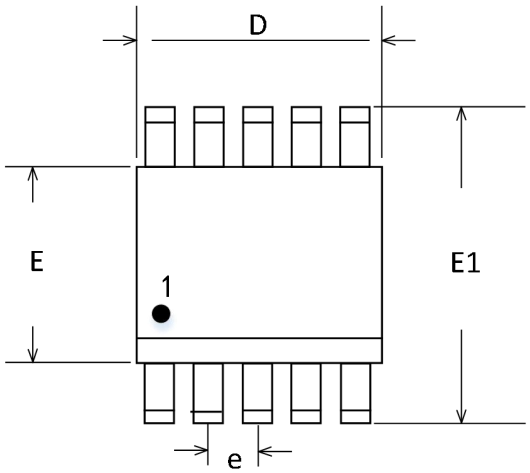


UNIT:mm

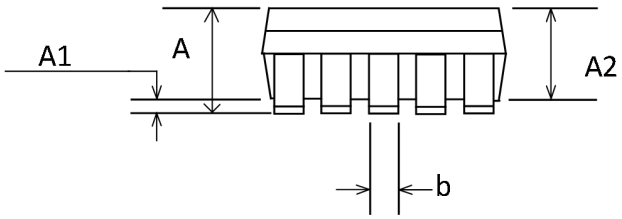
Symbol	Dimensions In Millimeters	
	Min	Max
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.31	0.51
F	0.40	1.27
G	1.27BSC	
H	5.80	6.20
J	0°	8°
K	0.10	0.25
R	0.25	0.50

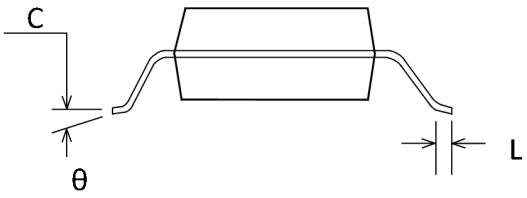
Chinese version:CD8511_CD8512_CD8514

MSOP-10



UNIT:mm

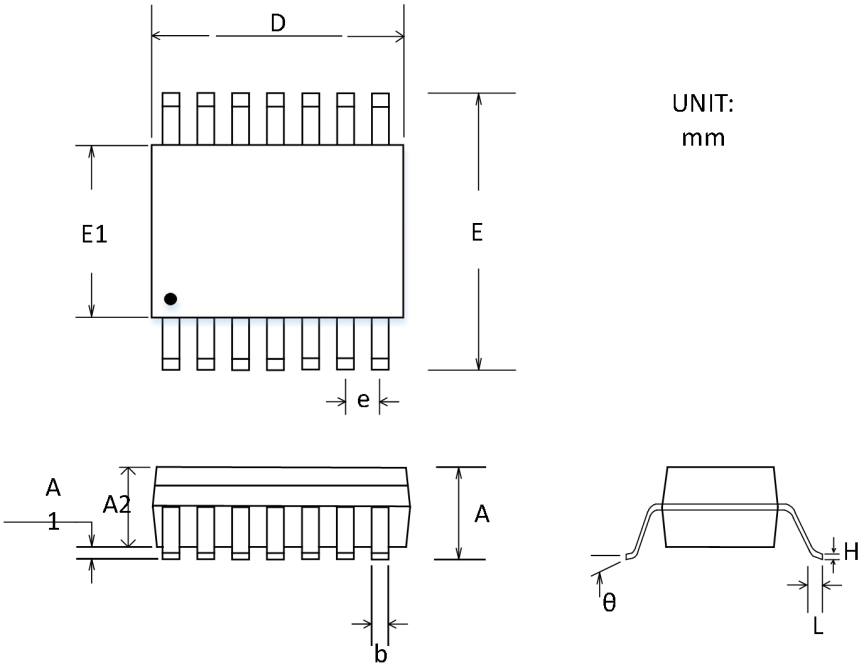




Symbol	Dimensions In Millimeters	
	Min	Max
A	0.820	1.100
A1	0.020	0.150
A2	0.750	0.950
b	0.180	0.280
c	0.090	0.230
D	2.900	3.100
E	2.900	3.100
E1	4.750	5.050
e	0.50 BSC	
L	0.400	0.800
θ	0°	6°

Chinese version:CD8511_CD8512_CD8514

TSSOP-14

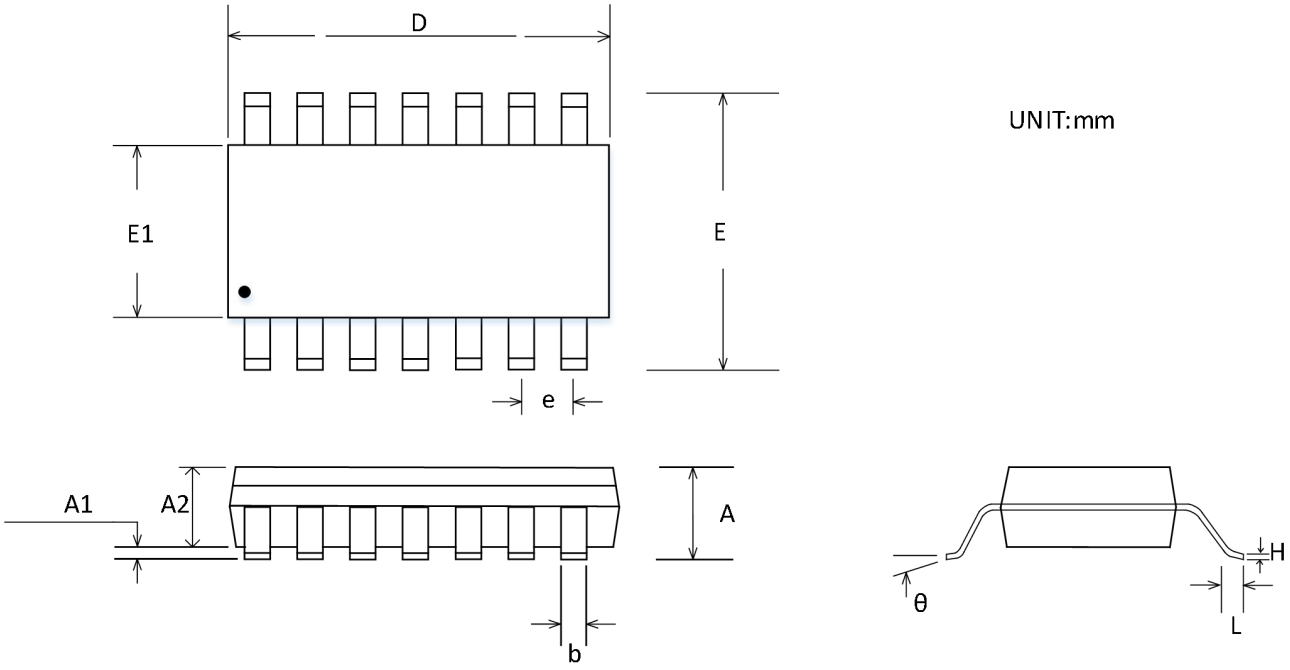


UNIT:
mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.20MAX	
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
D	4.90	5.10
E	6.40BSC	
E1	4.30	4.50
e	0.65BSC	
H	0.09	0.20
L	0.45	0.75
θ	0°	8°

Chinese version:CD8511_CD8512_CD8514

SOP-14



UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
b	0.31	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.27BSC	
H	0.17	0.25
L	0.40	1.27
θ	0°	8°

Chinese version:CD8511_CD8512_CD8514

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD8511AST5	-40℃~125℃	SOT23-5	Tape and Reel, 3000
CD5811BST5	-40℃~125℃	SOT23-5	Tape and Reel, 3000
CD8511AS8	-40℃~125℃	SOIC-8(SOP8)	Tape and Reel, 2500
CD8511AS8-RL	-40℃~125℃	SOIC-8(SOP8)	Tape and Reel, 3000
CD8511AS8-REEL	-40℃~125℃	SOIC-8(SOP8)	Tape and Reel, 4000
CD8511AMS8	-40℃~125℃	MSOP-8	Tape and Reel, 3000
CD8512AS8	-40℃~125℃	SOIC-8(SOP8)	Tape and Reel, 2500
CD8512AS8-RL	-40℃~125℃	SOIC-8(SOP8)	Tape and Reel, 3000
CD8512AS8-REEL	-40℃~125℃	SOIC-8(SOP8)	Tape and Reel, 4000
CD8512AMS8	-40℃~125℃	MSOP-8	Tape and Reel, 3000
CD8512ATDE8	-40℃~125℃	TDFN-2x2-8	Tape and Reel, 3000
CD8513AMS	-40℃~125℃	MSOP-10	Tape and Reel, 3000
CD8514AS14	-40℃~125℃	SOIC-14(SOP14)	Tape and Reel, 2500
CD8514AS14-RL	-40℃~125℃	SOIC-14(SOP14)	Tape and Reel, 3000
CD8514AS14-REEL	-40℃~125℃	SOIC-14(SOP14)	Tape and Reel, 4000
CD8514ATS14	-40℃~125℃	TSSOP-14	Tape and Reel, 2500
CD8514ATS14-RL	-40℃~125℃	TSSOP-14	Tape and Reel, 3000
CD8514ATS14-REEL	-40℃~125℃	TSSOP-14	Tape and Reel, 4000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.3	Initial version	Regular update	WW	LYL	

Chinese version:CD8511_CD8512_CD8514