CoreadDvices
承芯微电子

CD8531_CD8532_CD8534

Precision, Low Noise, CMOS, Rail-to-Rail, Input/Output Operational Amplifiers

Version: Rev 1.0.0 Date: 2025-5-26

Features

- Single-supply operation: 2.7 V to 5.5 V
- High output current: ±250 mA
- Low supply current: 750 μA/amplifier
- Wide bandwidth: 3 MHz
- Slew rate: 5 V/μs
- No phase reversal
- Low input currents
- Unity gain stable
- Rail-to-rail input and output

Application

- Multimedia audio
- LCD drivers
- ASIC input or output amplifiers
- Headphone drivers

Description

The CD8531, CD8532, and CD8534 are single, dual, and quad rail-to-rail input/output single-supply amplifiers featuring 250mA output drive current. This high output current makes these amplifiers excellent for driving either resistive or capacitive loads. AC performance is very good with 3 MHz bandwidth,5 V/μs slew rate, and low distortion. All are guaranteed to operate from a 2.7 V single supply as well as a 5.5 V supply.

The very low input bias currents enable the CD8531, CD8532, and CD8534 to be used for integrators, diode amplification, and other applications requiring low input bias current. Supply current is only 750 μA per amplifier at 5 V, allowing low current applications to control high current loads.

The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs, or other wide output swing devices in single-supply systems.

The CD8531/CD8532/CD8534 are specified over the extended industrial temperature range (−40°C to +125°C). The CD8531 is available in 8-lead SOIC, 5-lead SC70, and 5-lead SOT-23 packages. The CD8532 is available in 8-lead SOIC, 8-lead MSOP, and 8-lead TSSOP surface-mount packages. The CD8534 is available in narrow 14-lead SOIC and 14-lead TSSOP surface-mount packages.

Chinese version:CD8531_CD8532_CD8534

Contents

Pin Configurations

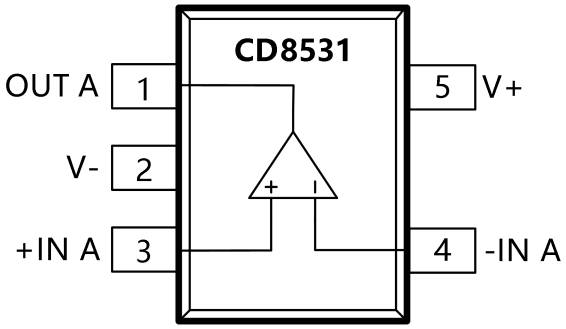

Figure 1 .SC70-5/SOT-23-5

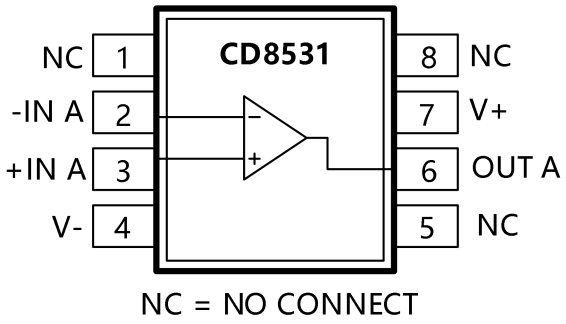

Figure 2 .SOP-8

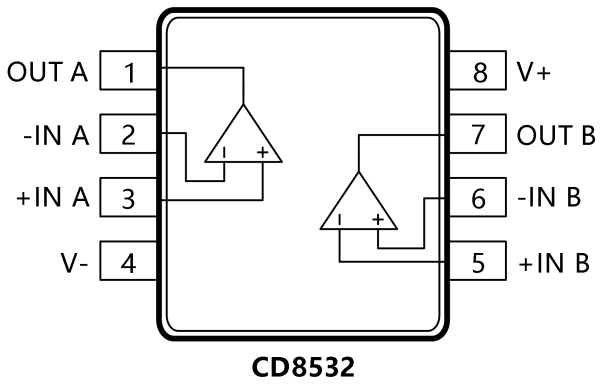

Figure 3. SOP-8/TSSOP-8/MSOP-8

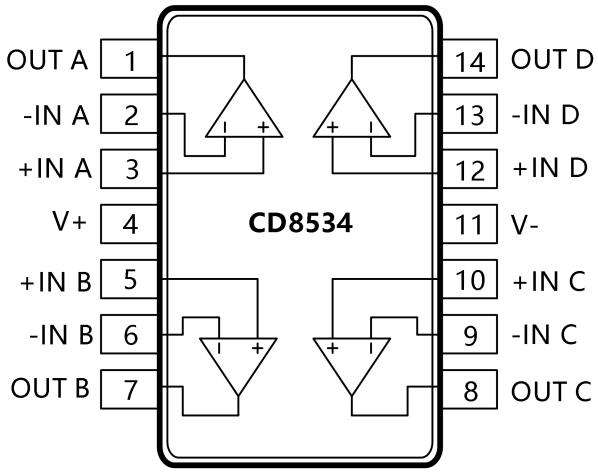

Figure 4. SOP-14/TSSOP-14

Absolute Maximum Ratings

Parameter	Range
Supply Voltage (VS)	7V
Input Voltage	GND to VS
Differential Input Voltage	±6 V
Storage Temperature Range	−65℃ to +150℃
Operating Temperature Range	−40℃ to +125℃
Junction Temperature Range	−65℃ to +150℃
Lead Temperature (Soldering,60 sec)	300℃

Electrical characteristics

V_S=3.0V, V_{CM}=1.35V, T_A=25℃, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		--	--	25	mV
		−40℃ ≤ T_A ≤ +125℃	--	--	30	mV
Input Bias Current	I_B		--	5	50	pA
		−40℃ ≤ T_A ≤ +125℃	--	--	60	pA
Input Offset Current	I_{OS}		--	1	25	pA
		−40℃ ≤ T_A ≤ +125℃	--	--	30	pA
Input Voltage Range			0	--	3	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=0V to 2.7V	38	45	--	dB
Large Signal Voltage Gain	A_{VO}	R_L=2kΩ, V_O=0.5V to 2.2V	--	25	--	V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta_T$		--	20	--	μV/℃
Bias Current Drift	Δ_{IB}/Δ_T		--	50	--	fA/℃
Offset Current Drift	Δ_{IOS}/Δ_T		--	20	--	fA/℃
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10mA	2.85	2.92	--	V
		−40℃ ≤ T_A ≤ +125℃	2.8	--	--	V
Output Voltage Low	V_{OL}	I_L = 10mA	--	60	100	mV
		−40℃ ≤ T_A ≤ +125℃	--	--	125	mV
Output Current	I_{OUT}		--	±250	--	mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1MHz, A_V = 1	--	60	--	Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	45	55	--	dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V	--	0.70	1	mA
		−40℃ ≤ T_A ≤ +125℃	--	--	2.5	mA
DYNA PEMIC RFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	--	3.5	--	V/μs
Settling Time	T_S	To 0.01%	--	1.6	--	μs
Gain Bandwidth Product	GBP		--	2.2	--	MHz
Phase Margin	ϕo		--	70	--	Degrees

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Channel Separation	CS	f = 1kHz, R_L = 2kΩ	--	65	--	dB
NOISE PERFORMANCE						
Voltage Noise Density	en	f = 1kHz	--	45	--	$\mathbf{nV/\sqrt{Hz}}$
		f = 10kHz	--	30	--	$\mathbf{nV/\sqrt{Hz}}$
Current Noise Density	in	f = 1kHz	--	0.05	--	$\mathbf{pA/\sqrt{Hz}}$

VS = 5.0V, V_{CM} = 2.5V, TA = 25℃, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		--	--	25	mV
		−40℃ ≤ T_A ≤ +125℃	--	--	30	mV
Input Bias Current	I_B		--	5	50	pA
		−40℃ ≤ T_A ≤ +125℃	--	--	60	pA
Input Offset Current	I_{OS}		--	1	25	pA
		−40℃ ≤ T_A ≤ +125℃	--	--	30	pA
Input Voltage Range			0	--	5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to 5V	38	47	--	dB
Large Signal Voltage Gain	A_{VO}	R_L=2kΩ, V_O=0.5V to 4.5V	15	80	--	V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta_T$	−40℃ ≤ T_A ≤ +125℃	--	20	--	μV/℃
Bias Current Drift	Δ_{IB}/Δ_T		--	50	--	fA/℃
Offset Current Drift	Δ_{IOS}/Δ_T		--	20	--	fA/℃
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10mA	4.9	4.94	--	V
		−40℃ ≤ T_A ≤ +125℃	4.85	--	--	V
Output Voltage Low	V_{OL}	I_L = 10mA	--	50	100	mV
		−40℃ ≤ T_A ≤ +125℃	--	--	125	mV
Output Current	I_{OUT}		--	±250	--	mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1MHz, A_V = 1	--	40	--	Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7V to 5.5V	45	55	--	dB
Supply Current/Amplifier	I_{SY}	V_O = 0V	--	0.75	1.25	mA
		−40℃ ≤ T_A ≤ +125℃	--	--	1.75	mA
DYNA PEMIC RFORMANCE						

Slew Rate	SR	R_L = 2 kΩ	--	5	--	V/μs
Full-Power Bandwidth	BW_P	1% distortion	--	350	--	KHz
Settling Time	t_S	To 0.01%	--	1.4	--	μs
Gain Bandwidth Product	GBP		--	3	--	MHz
Phase Margin	ϕo		--	70	--	Degrees
Channel Separation	CS	f = 1 kHz, RL = 2 kΩ	--	65	--	dB
NOISE PERFORMANCE						
Voltage Noise Density	en	f = 1 kHz	--	45	--	$nV/\sqrt{Hz}$
		f = 10 kHz	--	30	--	$nV/\sqrt{Hz}$
Current Noise Density	in	f = 1 kHz	--	0.05	--	$pA/\sqrt{Hz}$

Typical Characteristics

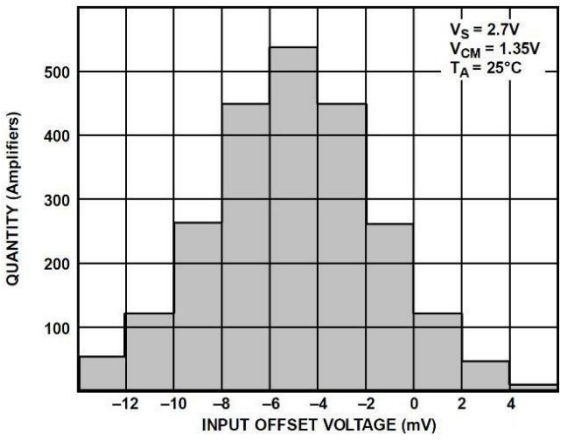

Figure 5. Input Offset Voltage Distribution

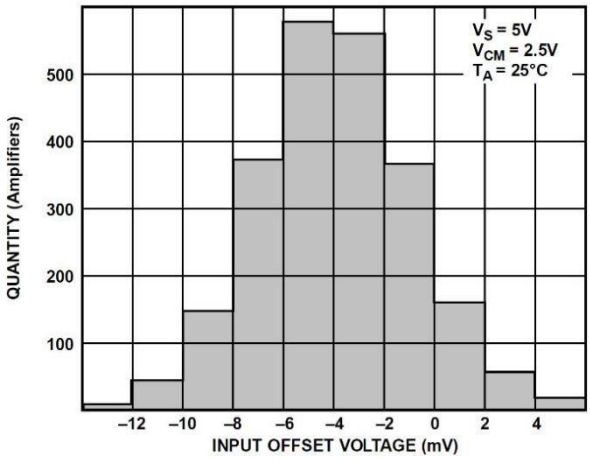

Figure 6. Input Offset Voltage Distribution

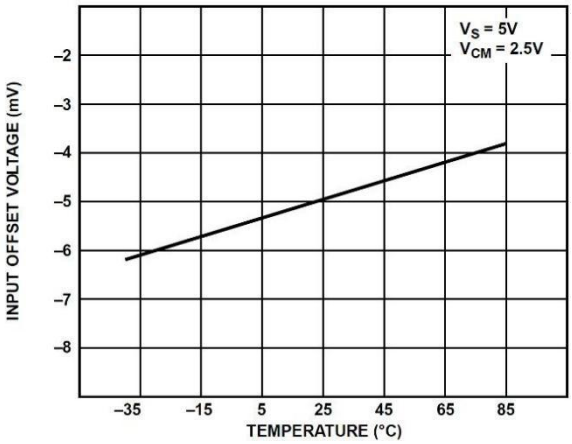

Figure 7. Input Offset Voltage vs. Temperature

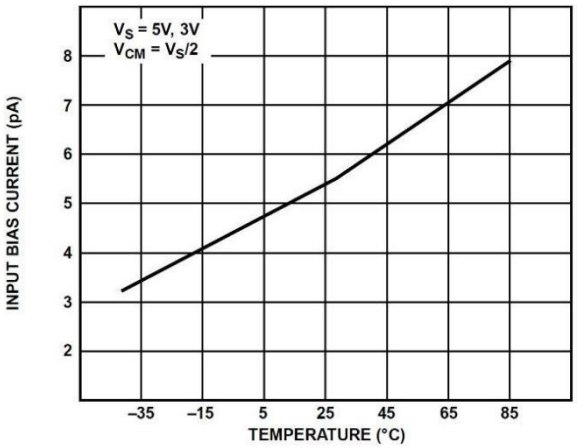

Figure 8. Input Bias Current vs. Temperature

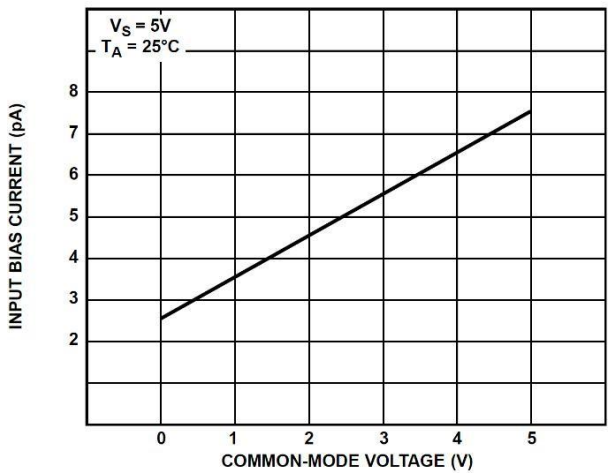

Figure 9. Input Bias Current vs. Common-Mode Voltage

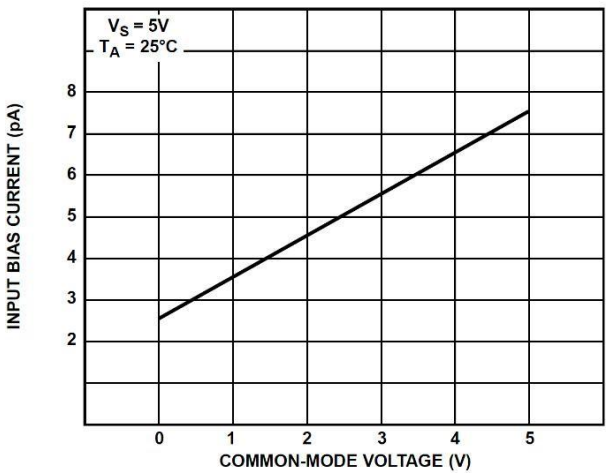

Figure 10. Input Offset Current vs. Temperature

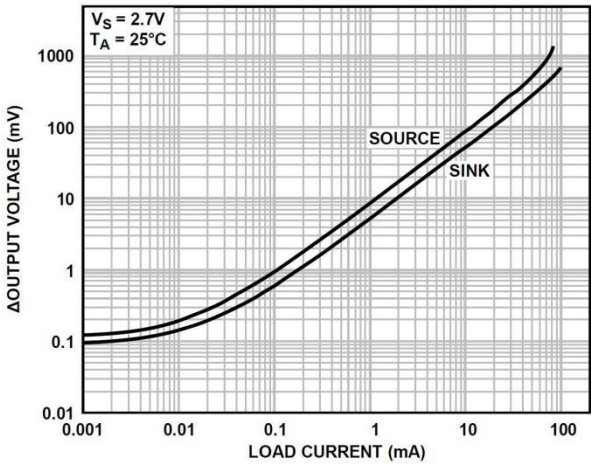

Figure 11. Output Voltage to Supply Rail vs. Load Current

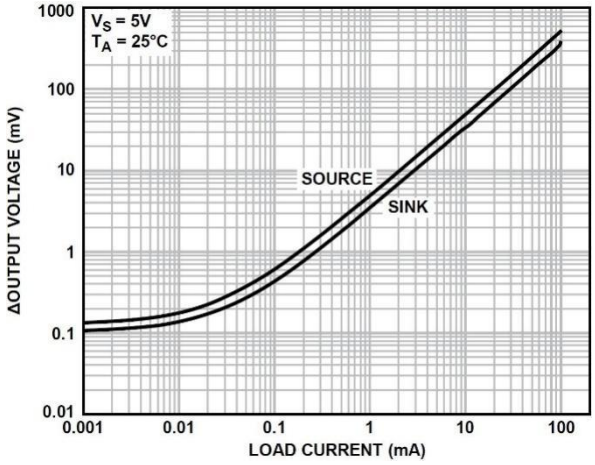

Figure12. Output Voltage to Supply Rail vs. Load Current

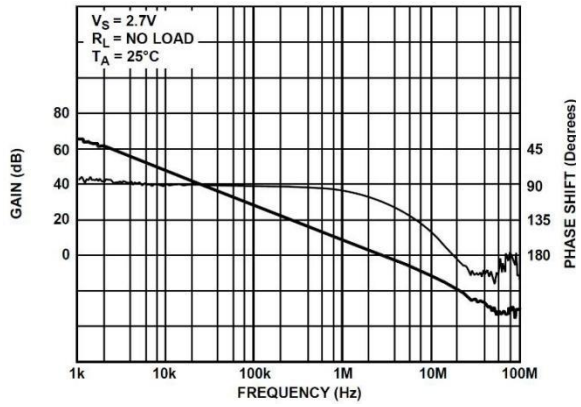

Figure 13. Open-Loop Gain and Phase Shift vs. Frequency

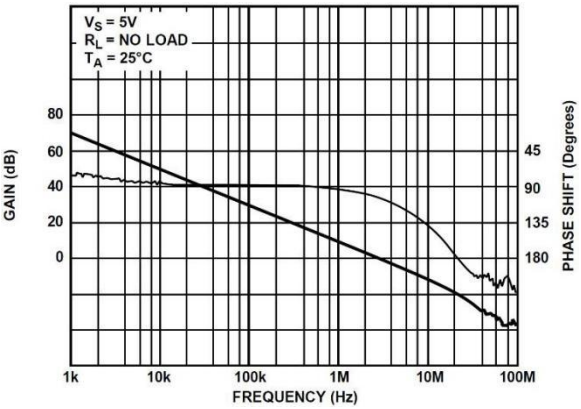

Figure 14. Open-Loop Gain and Phase Shift vs. Figure Frequency

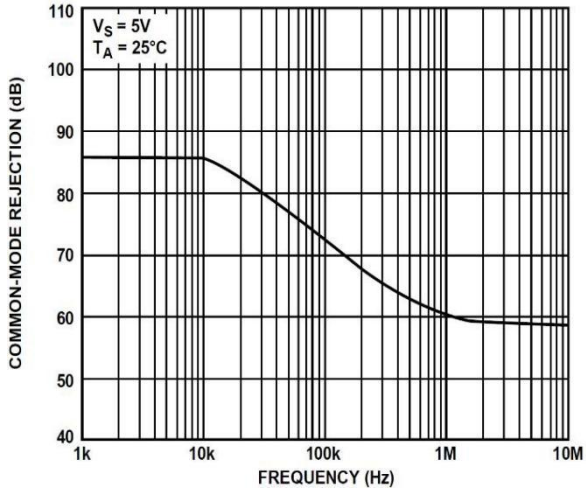

Figure 15. Common-Mode Rejection vs. Frequency

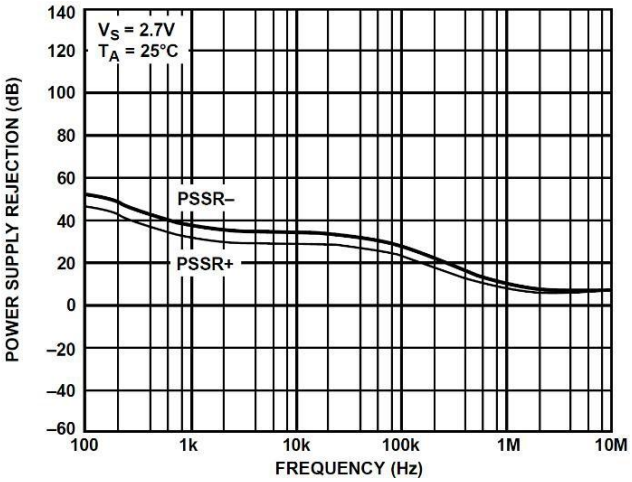

Figure16. Power Supply Rejection vs. Frequency

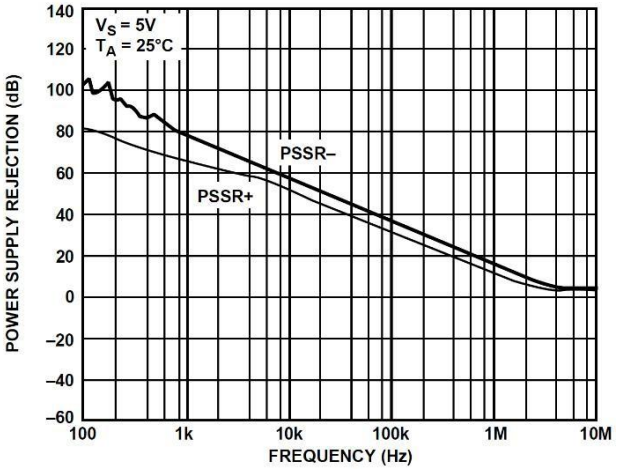

Figure 17. Power Supply Rejection vs. Frequency

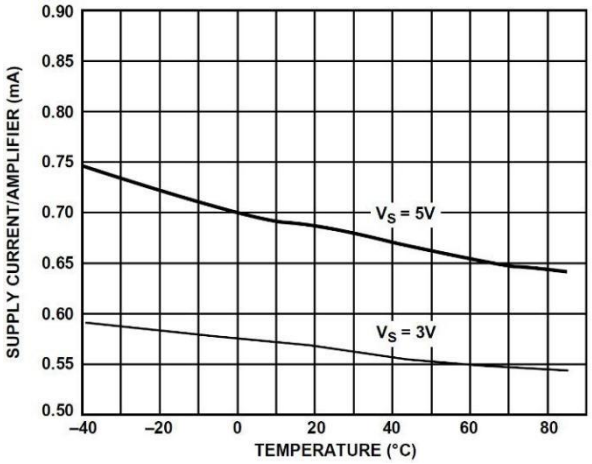

Figure 18. Supply Current per Amplifier vs. Figure Temperature

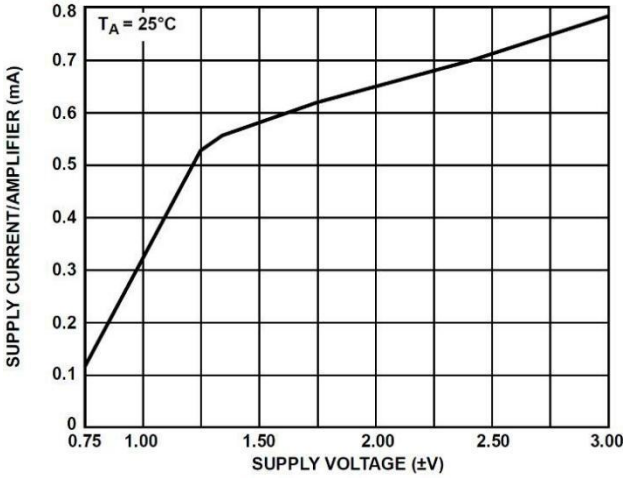

Figure 19. Supply Current per Amplifier vs.Supply Voltage

Theory Of Operation

The CD8531/CD8532/CD8534 are all CMOS, high output current drive, rail-to-rail input/output operational amplifiers. Their high output current drive and stability with heavy capacitive loads make the CD8531/CD8532/CD8534 excellent choices as drive amplifiers for LCD panels.

Figure 20 illustrates a simplified equivalent circuit for the CD8531/CD8532/CD8534. Like many rail-to-rail input amplifier configurations, it comprises two differential pairs, one N-channel (M1 to M2) and one P-channel (M3 to M4). These differential pairs are biased by 50 μA current sources, each with a compliance limit of approximately 0.5 V from either supply voltage rail. The differential input voltage is then converted into a pair of differential output currents. These differential output currents are then combined in a compound folded-cascade second gain stage (M5 to M9). The outputs of the second gain stage at M8 and M9 provide the gate voltage drive to the rail-to-rail output stage. Additional signal current recombination for the output stage is achieved using M11 to M14.

To achieve rail-to-rail output swings, the CD8531/CD8532/ CD8534 design employs a complementary, common source output stage (M15 to M16). However, the output voltage swing is directly dependent on the load current because the difference between the output voltage and the supply is determined by the CD8531/CD8532/CD8534’ s output transistors on channel resistance. The output stage also exhibits voltage gain by virtue of the use of common source amplifiers; as a result, the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a strong dependence on the total load resistance at the output of the CD8531/ CD8532/CD8534.

Short-Circuit Protection

As a result of the design of the output stage for the maximum load current capability, the CD8531/CD8532/CD8534 do not have any internal short-circuit protection circuitry. Direct connection of the output of the CD8531/CD8532/CD8534 to the positive supply in single-supply applications destroys the device. In applications where some protection is needed, but not at the expense of reduced output voltage headroom, a low value resistor in series with the output, as shown in Figure 21, can be used. The resistor, connected within the feedback loop of the amplifier, has very little effect on the performance of the amplifier other than limiting the maximum available output voltage swing. For single 5 V supply applications, resistors less than 20 Ω are not recommended.

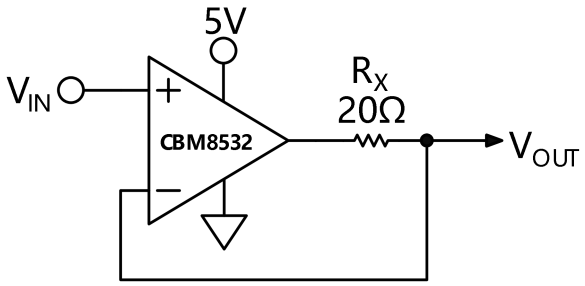

Figure 21. Output Short-Circuit Protection

Power Dissipation

Although the CD8531/CD8532/CD8534 are capable of providing load currents to 250 mA, the usable output load current drive capability is limited to the maximum power dissipation allowed by the device package used. In any application, the absolute maximum junction temperature for the CD8531/CD8532/CD8534 is 150°C. The maximum junction temperature should never be exceeded because the device could suffer premature failure. Accurately measuring power dissipation of an integrated circuit is not always a straightforward exercise; therefore, Figure 22 is provided as a design aid for either setting a safe output current drive level or selecting a heat sink for the package options available on the CD8531/CD8532/CD8534.

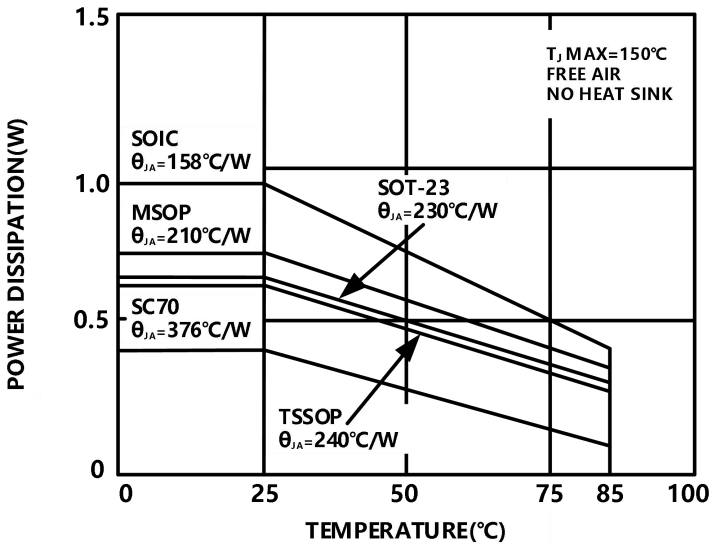

Figure 22. Maximum Power Dissipation vs. Ambient Temperature T_J

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Applications Information

HIGH OUTPUT CURRENT, BUFFERED REFERENCE/REGULATOR

Many applications require stable voltage outputs relatively close in potential to an unregulated input source. This low dropout type of reference/regulator is readily implemented with a rail-to-rail output op amp and is particularly useful when using a higher current device, such as the CD8531/CD8532/CD8534. A typical example is the 3.3V or 4.5V reference voltage developed from a 5V system source. Generating these voltages requires a three terminal reference, such as the REF196 (3.3V) or the REF194 (4.5V), both of which feature low power, with sourcing outputs of 30 mA or less. Figure 23 shows how such a reference can be outfitted with an CD8531/CD8532/CD8534 buffer for higher currents and/or voltage levels, plus sink and source load capability.

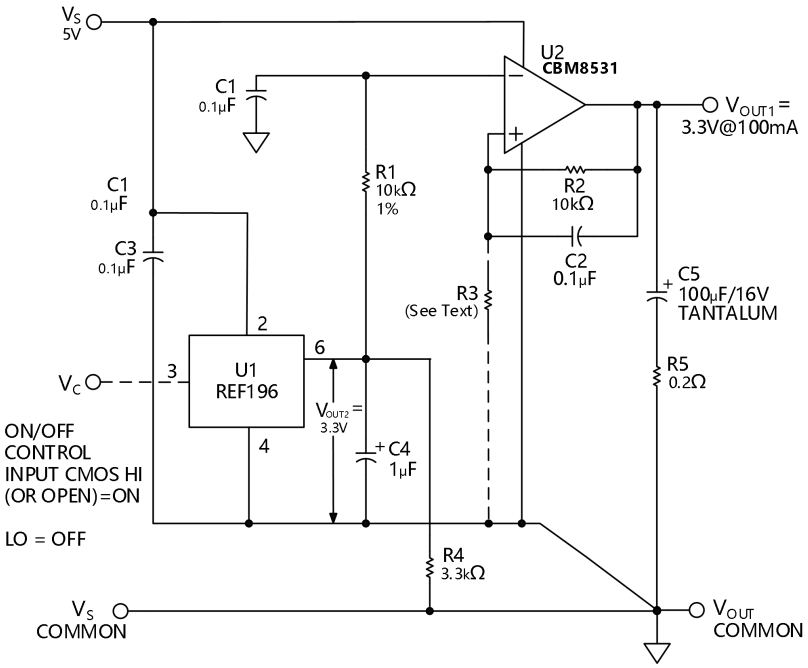


Figure 23. High Output Current Reference/Regulator

The low dropout performance of this circuit is provided by stage U2, an CD8531 connected as a follower/buffer for the basic reference voltage produced by U1. The low voltage saturation characteristic of the CD8531/CD8532/CD8534 allows up to 100mA of load current in the illustrated use, as a 5V to 3.3V converter with good dc accuracy. In fact, the dc output voltage change for a 100mA load current delta measures less than 1mV. This corresponds to an equivalent output impedance of < 0.01 Ω. In this application, the stable 3.3 V from U1 is applied to U2 through a noise filter, R1 to C1. U2 replicates the U1 voltage within a few millivolts, but at a higher current output at VOUT1, with the ability to both sink and source output current(s), unlike most IC references. R2 and C2 in the feedback path of U2 provide additional noise filtering.

Transient performance of the reference/regulator for a 100mA step change in load current is also quite good and is largely determined by the R5 to C5 output network. With values as shown, the transient is about 20mV peak and settles to within 2mV in less than 10μs for either polarity. Although room exists for optimizing the transient response, any changes to the R5 to C5 network should be verified by experiment to preclude the possibility of excessive ringing with some capacitor types.

To scale VOUT2 to another (higher) output level, the optional resistor R3 (shown dotted in Figure 23) is added, causing the new VOUT1 to become

$$V_{OUT1} = V_{OUT2} \times (1 + \frac{R2}{Rt})$$

The circuit can either be used as shown, as a 5 V to 3.3 V reference/regulator, or with on/off control. By driving Pin 3 of U1 with a logic control signal as noted, the output is switched on/off. Note that when on/off control is used, R4 must be used with U1 to speed on/off switching.

SINGLE-SUPPLY HEADPHONE AMPLIFIER

Because of its speed and large output drive, the CD8531/ CD8532/CD8534 make an excellent headphone driver, as illustrated in Figure 24. Its low supply operation and rail-to-rail inputs and outputs give a maximum signal swing on a single 5V supply. To ensure maximum signal swing available to drive the headphone, the amplifier inputs are biased to V+/2, which in this case is 2.5V. The 100kΩ resistor to the positive supply is equally split into two 50kΩ resistors, with their common point bypassed by 10μF to prevent power supply noise from contaminating the audio signal.

The audio signal is then ac-coupled to each input through a 10μF capacitor. A large value is needed to ensure that the 20 Hz audio information is not blocked. If the input already has the proper dc bias, the ac coupling and biasing resistors are not required. A 270μF capacitor is used at the output to couple the amplifier to the headphone. This value is much larger than that used for the input because of the low impedance of the head-phones, which can range from 32Ω to 600Ω. An additional 16Ω resistor is used in series with the output capacitor to protect the output stage of the op amp by limiting the capacitor discharge current. When driving a 48Ω load, the circuit exhibits less than 0.3% THD+N at output drive levels of 4Vp-p.

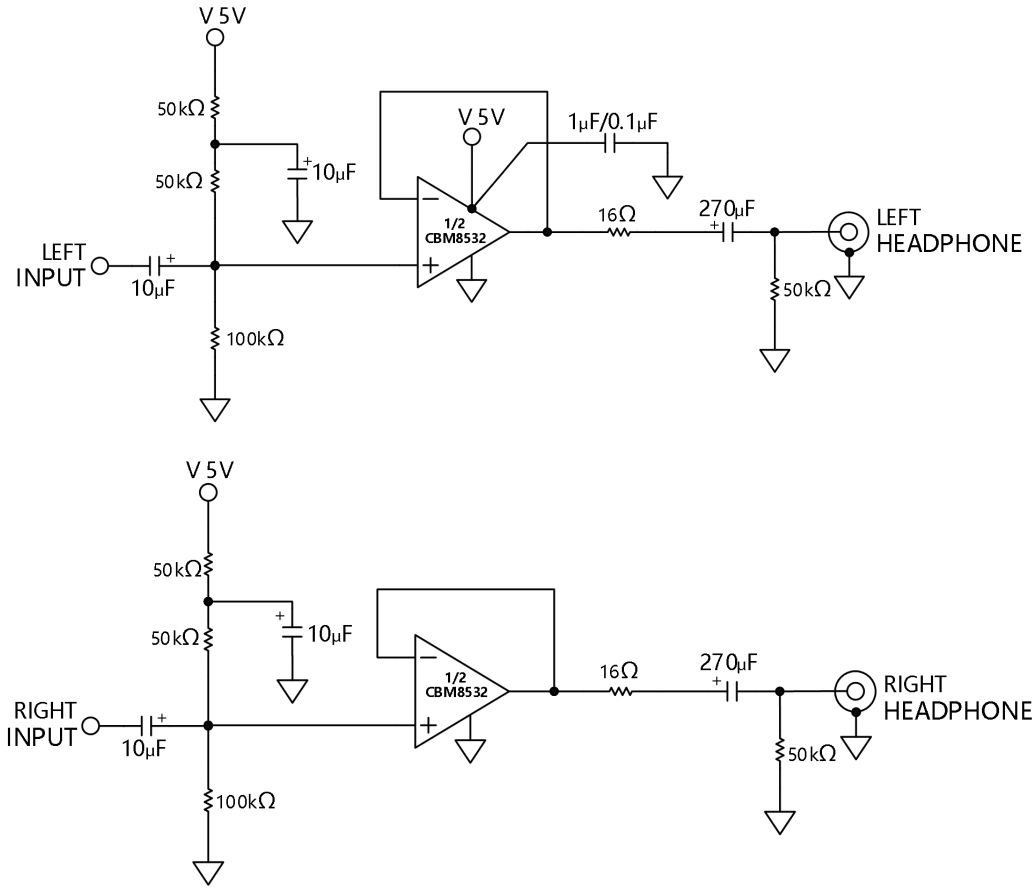


Figure 24. Single-Supply, Stereo Headphone Driver

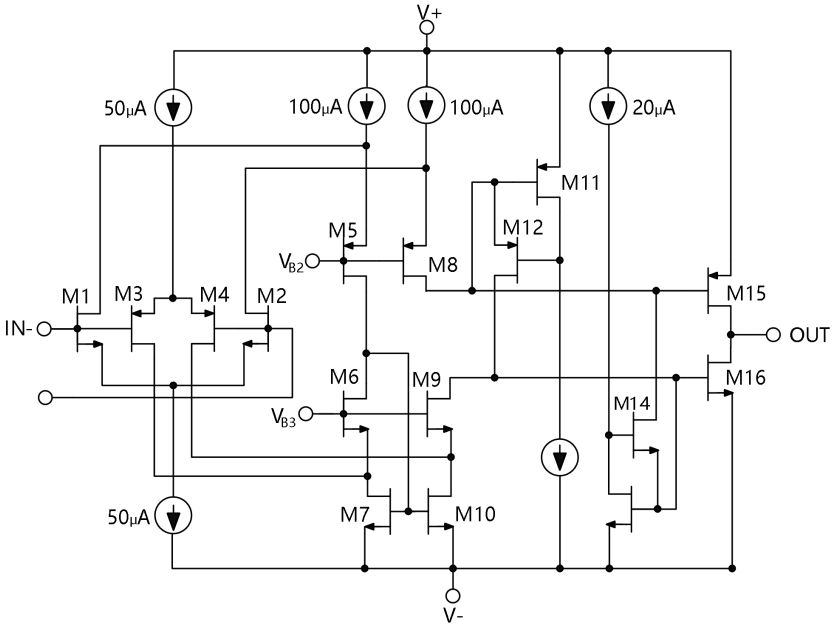
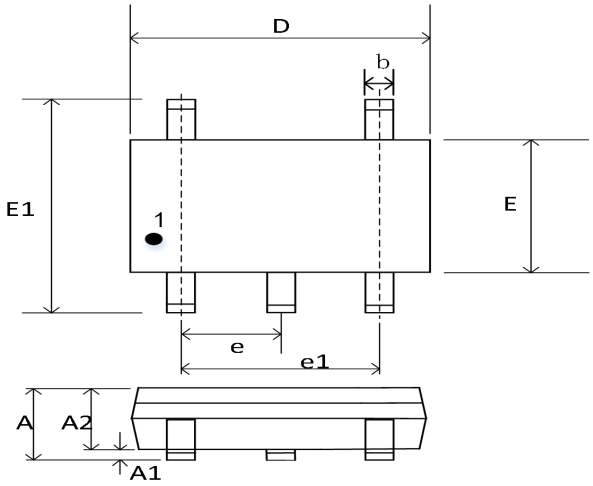


Figure 20. Simplified Equivalent Circuit

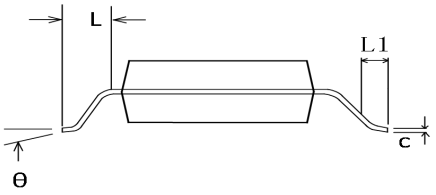
Chinese version:CD8531_CD8532_CD8534

Package Outline Dimensions

SC70-5



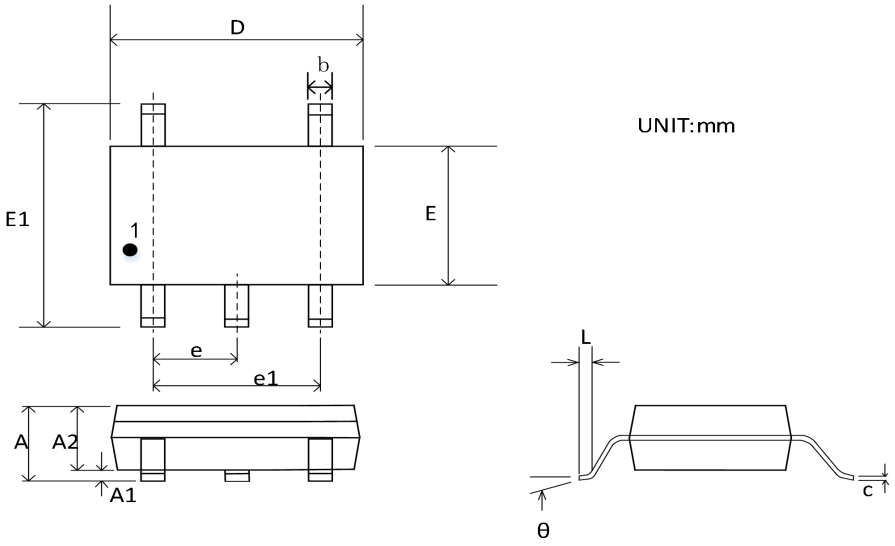
UNIT:mm



Symbol	Dimensions In Millimeters	
	Min	Max
A	0.800	1.100
A1	0.000	0.100
A2	0.700	1.000
b	0.150	0.300
c	0.080	0.220
D	1.800	2.200
E	1.150	1.350
E1	1.800	2.400
e	0.650 BSC	
e1	1.200	1.400
L	0.525 REF	
L1	0.260	0.460
θ	0°	8°

Chinese version:CD8531_CD8532_CD8534

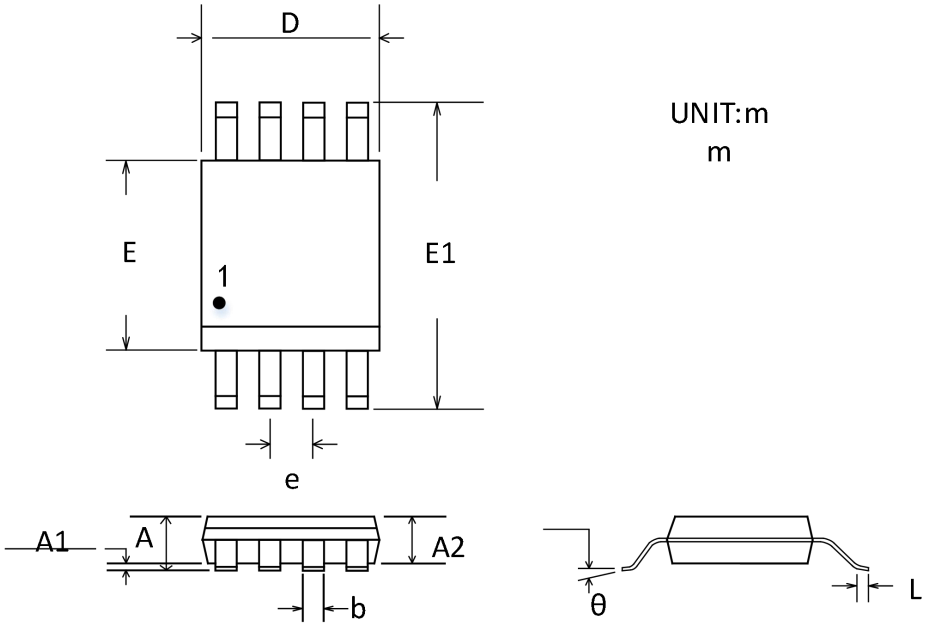
SOT23-5



Symbol	Dimensions In Millimeters	
	Min	Max
A	--	1.450
A1	--	0.150
A2	0.900	1.300
b	0.300	0.500
c	0.080	0.220
D	2.900 BSC	
E	1.600 BSC	
E1	2.80 BSC	
e	0.950 BSC	
e1	1.900 BSC	
L	0.300	0.600
θ	0°	8°

Chinese version:CD8531_CD8532_CD8534

MSOP-8

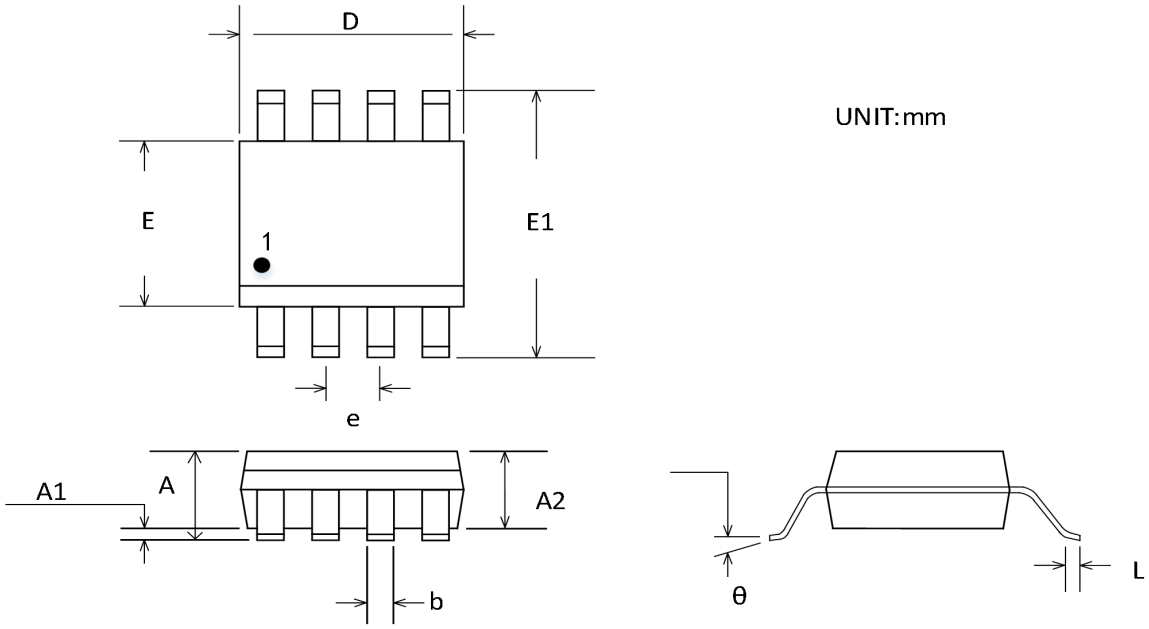


UNIT:m
m

Symbol	Dimensions In Millimeters	
	Min	Max
A	0.820	1.100
A1	0.000	0.150
A2	0.750	0.950
b	0.220	0.380
D	2.800	3.200
E	2.800	3.200
E1	4.650	5.150
e	0.650 BSC	
L	0.400	0.800
θ	0°	8°

Chinese version:CD8531_CD8532_CD8534

SOP-8

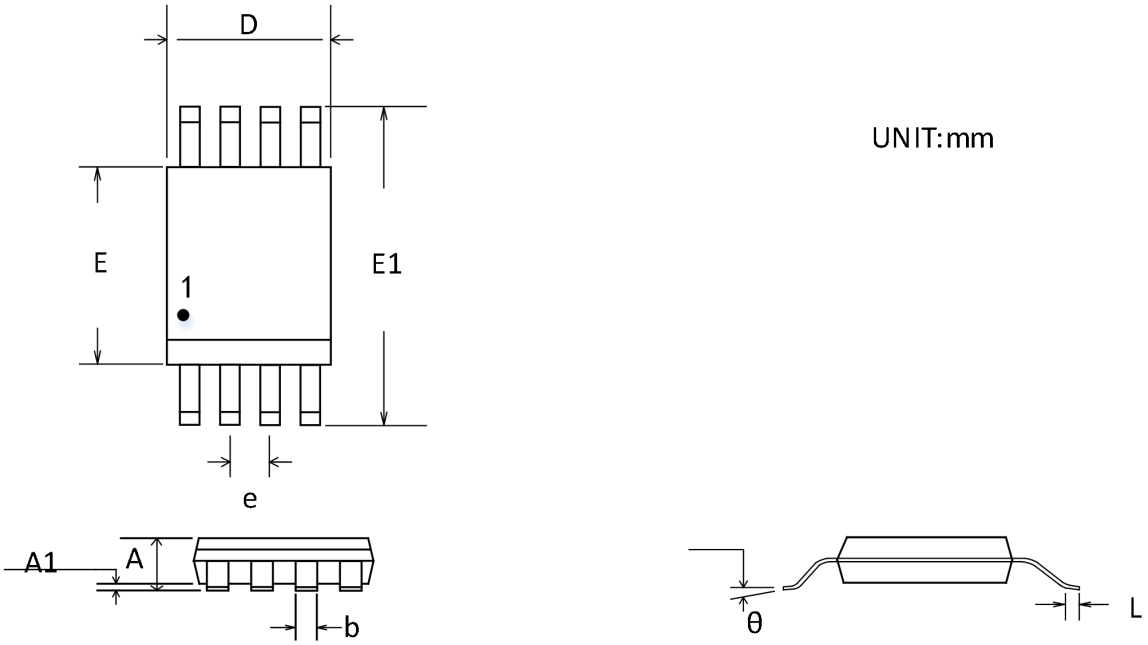


UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.310	0.510
D	4.800	5.000
E	3.800	4.000
E1	5.800	6.200
e	1.270 BSC	
L	0.400	1.270
θ	0°	8°

Chinese version:CD8531_CD8532_CD8534

TSSOP-8

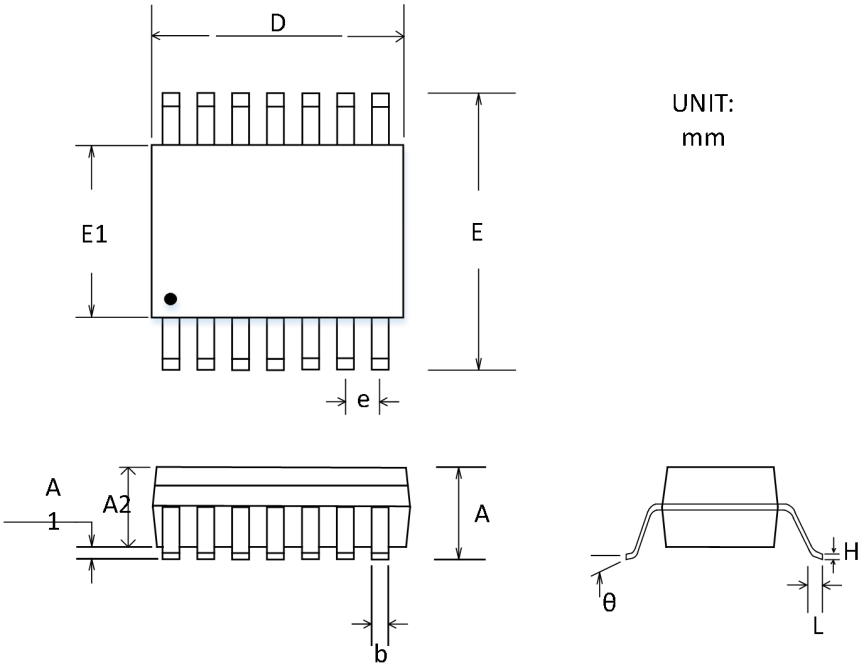


UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
D	2.90	3.10
E	4.30	4.50
E1	6.40BSC	
e	0.65 BSC	
L	0.45	0.75
θ	0°	8°

Chinese version:CD8531_CD8532_CD8534

TSSOP-14

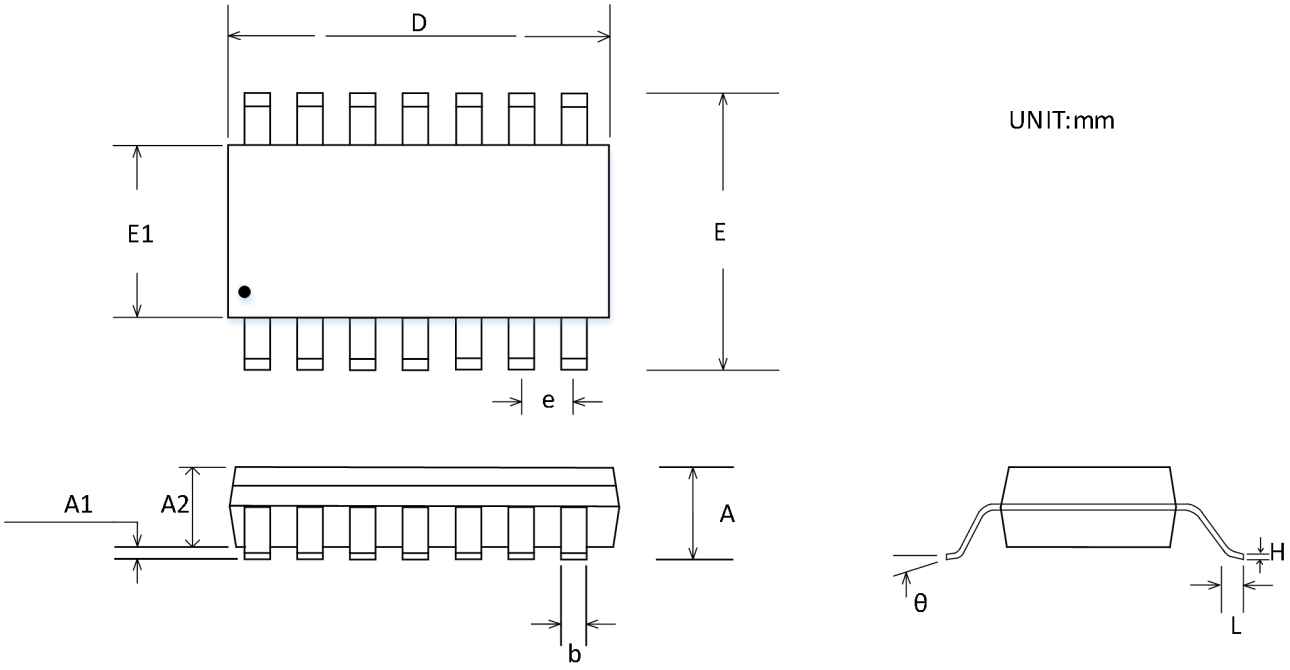


UNIT:
mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.20MAX	
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
D	4.90	5.10
E	6.40BSC	
E1	4.30	4.50
e	0.65BSC	
H	0.09	0.20
L	0.45	0.75
θ	0°	8°

Chinese version:CD8531_CD8532_CD8534

SOP-14



UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
b	0.31	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.27BSC	
H	0.17	0.25
L	0.40	1.27
θ	0°	8°

Chinese version:CD8531_CD8532_CD8534

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD8531ASC7	-40℃~125℃	SC70-5	Tape and Reel,3000
CD8531AST5	-40℃~125℃	SOT23-5	Tape and Reel,3000
CD8531AS8	-40℃~125℃	SOP-8	Tape and Reel,2500
CD8531AS8-RL	-40℃~125℃	SOP-8	Tape and Reel,3000
CD8531AS8-REEL	-40℃~125℃	SOP-8	Tape and Reel,4000
CD8532AS8	-40℃~125℃	SOP-8	Tape and Reel,2500
CD8532AS8-RL	-40℃~125℃	SOP-8	Tape and Reel,3000
CD8532AS8-REEL	-40℃~125℃	SOP-8	Tape and Reel,4000
CD8532AMS8	-40℃~125℃	MSOP-8	Tape and Reel,3000
CD8532ATS8	-40℃~125℃	TSSOP-8	Tape and Reel,2500
CD8532ATS8-RL	-40℃~125℃	TSSOP-8	Tape and Reel,3000
CD8532ATS8-REEL	-40℃~125℃	TSSOP-8	Tape and Reel,4000
CD8534AS14	-40℃~125℃	SOP-14	Tape and Reel,2500
CD8534AS14-RL	-40℃~125℃	SOP-14	Tape and Reel,3000
CD8534AS14-REEL	-40℃~125℃	SOP-14	Tape and Reel,4000
CD8534ATS14	-40℃~125℃	TSSOP-14	Tape and Reel,2500
CD8534ATS14-RL	-40℃~125℃	TSSOP-14	Tape and Reel,3000
CD8534ATS14-REEL	-40℃~125℃	TSSOP-14	Tape and Reel,4000

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Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.5.26	Initial version	Regular update	WW	LYL	

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