



CD8538_CD8539

Low Power, Precision, Auto-Zero Op Amps

Version: Rev 1.0.0 Date: 2025-5-26

Features ■■

- Low Offset Voltage: 1uV
- Input Offset Drift: 0.03 μ V/°C
- High Gain Bandwidth Product: 1.6MHz
- Rail-to-Rail Input and Output
- High Gain, CMRR, PSRR:130dB
- High Slew Rate: 0.7V/ μ s
- Low Noise: 1.3uVp-p (0.01~10Hz)
- Low Power Consumption: The typical values
- Overload Recovery Time:2us
- Low Supply Voltage: +2.7 V to +5.5 V
- No External Capacitors Required
- Extended Temperature: -40°C to +125°C

Application ■■

- Temperature Sensors
- Medical/Industrial Instrumentation
- Pressure Sensors
- Battery-Powered Instrumentation
- Active Filtering
- Weight Scale Sensor
- Strain Gage Amplifiers
- Power Converter/Inverter

Description ■■

The CD8538 and CD8539 series of CMOS operational amplifiers utilize auto-zero technology to simultaneously achieve an extremely low offset voltage (maximum 5 μ V) and near-zero drift during extended operation under varying temperatures. These amplifiers feature ultra-low noise, offset, and power consumption.

These miniature, high-precision operational amplifiers offer high impedance differential inputs, rail-to-rail input and output swing capabilities, a high gain-bandwidth product of 1.6MHz, and a slew rate of 0.7V/ μ s. They operate from single or dual power supplies ranging from a minimum of +2.7V ($\pm$ 1.35V) to a maximum of +5.5V ($\pm$ 2.5V).

The CD8538 and CD8539 (dual-supply with complete shutdown capability) series are specifically designed for industrial and automotive applications within a temperature range of -40°C to 125°C. The CD8538 single-supply amplifier is available in 5-pin SOT23, 8-pin MSOP, and 8-pin SOIC packages, while the CD8539 dual-supply amplifier comes in 8-pin SOIC and 8-pin MSOP narrow-body packages.

Contents

Features.....

- 1 -

Application.....

- 1 -

Description.....

- 1 -

Pin Configurations.....

- 3 -

Pin Description.....

- 4 -

Absolute Maximum Ratings.....

- 4 -

Electrical characteristics.....

- 5 -

Typical Characteristics.....

- 7 -

Application Information.....

- 10 -

Operating Voltage.....

- 10 -

Layout Guidelines.....

- 10 -

Package Outline Dimensions.....

- 11 -

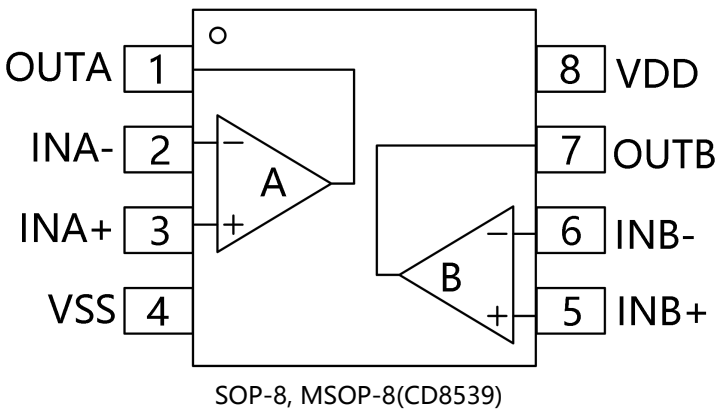
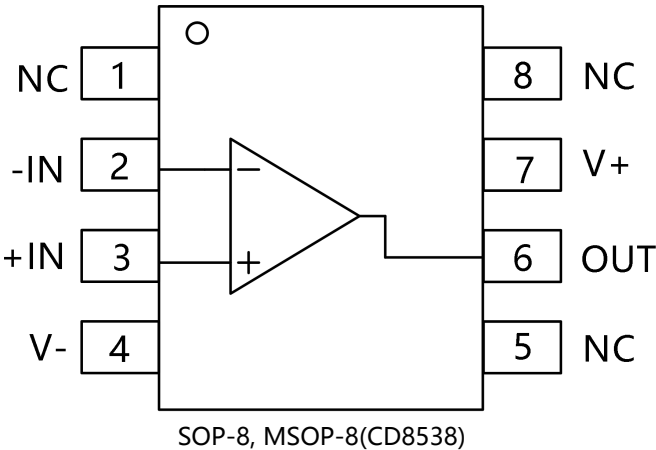
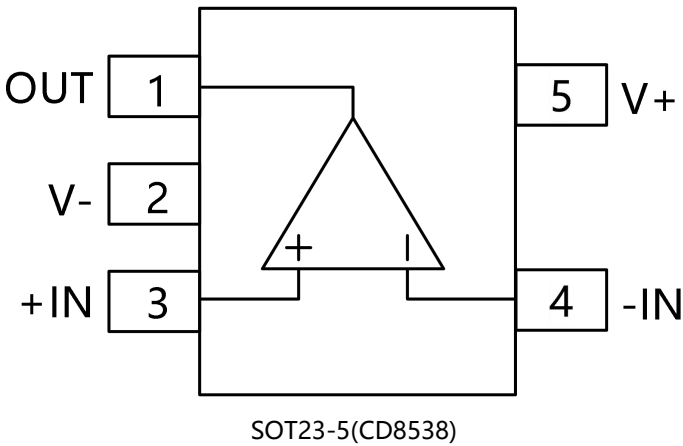
Package/Ordering Information.....

- 14 -

Revision Log.....

- 15 -

Pin Configurations



Pin Description

Pin_N	Symbol SOT23 (CD8538)	Input/Output	Function
1	OUT	Output	Output
2	V-	--	Negative power supply
3	+IN	Input	None Inverting input
4	-IN	Input	Inverting input
5	V+	--	Positive power supply
Pin_N	Symbol MSOP/SOP (CD8539)	Input/Output	Function
1	NC	--	Not Connect
2	-IN_A	Input	Inverting input
3	+IN_A	Input	None Inverting input
4	V-	--	Negative power supply
5	NC	--	Not Connect
6	OUT	Input	Output
7	V+	--	Positive power supply
8	NC	--	Not Connect
Pin_N	Symbol MSOP/SOP (CD8539)	Input/Output	Function
1	OUT_A	Output	Output A
2	-IN_A	Input	Inverting input
3	+IN_A	Input	None Inverting input A
4	V-	--	Negative power supply
5	+IN_B	Input	None Inverting input B
6	-IN_B	Input	Inverting input B
7	OUT_B	Output	Output B
8	V+	--	Positive power supply

Absolute Maximum Ratings

Parameter	Range
Supply Voltage	6V
Input Voltage	- 0.5 to (V+) + 0.5V
Differential Input Voltage	±6V
Storage Temperature Range All Packages	-65°C to +150°C
Operating Temperature Range All Packages	-40°C to +125°C
Junction Temperature Range All Packages	-65°C to +150°C
SOT23-5	200°C/W
MSOP-8	150°C/W
SOP-8	150°C/W
Lead Temperature	260°C
HBM	5kV

MM	400V
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Electrical characteristics

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

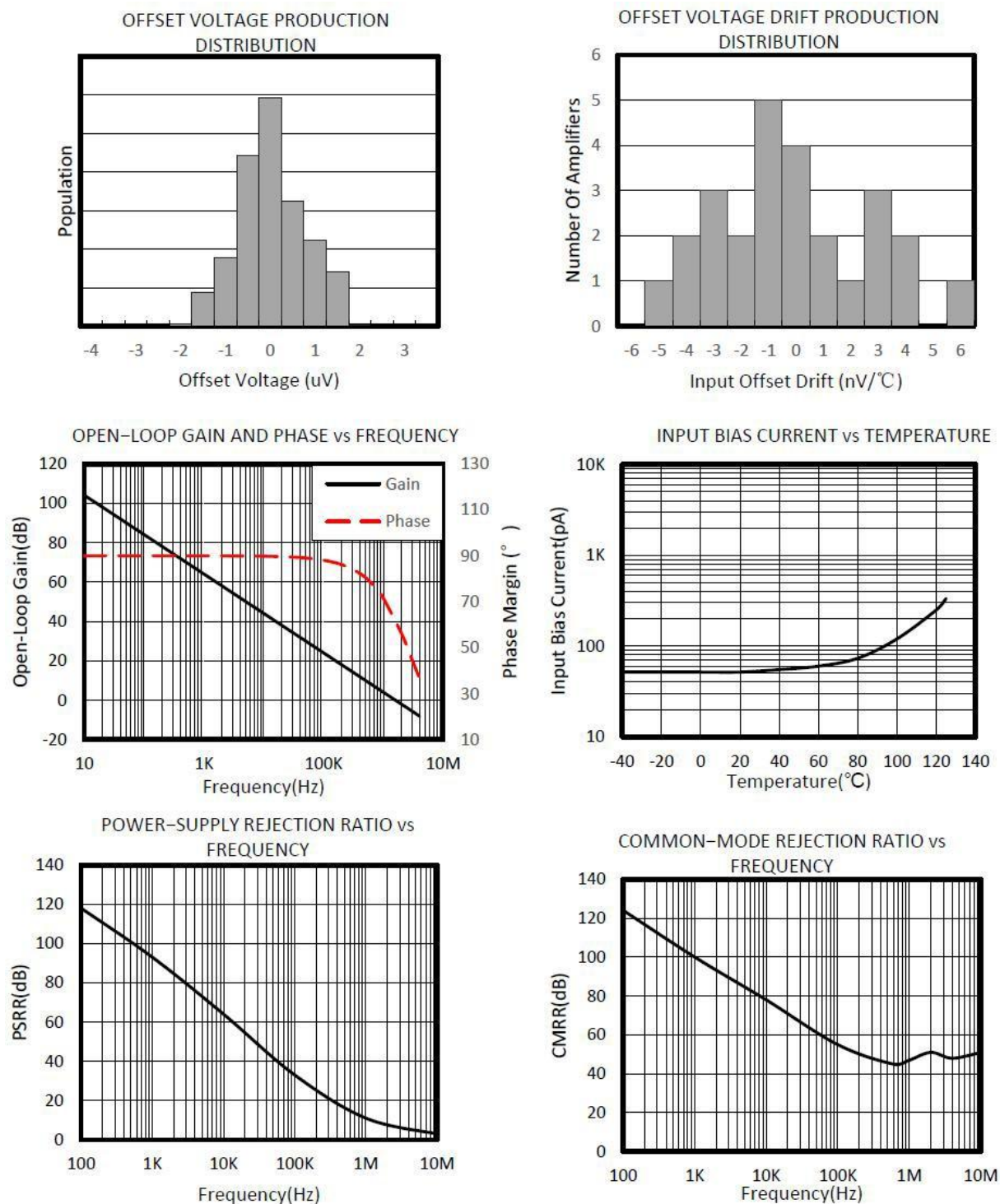
(At $T_A = +25^{\circ}\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{\text{OUT}} = V_S/2$, unless otherwise noted.)

PARAMETER	CONDIT ION	CD8538, CD8539			
		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Input Offset Voltage (V _{OS})	V _{CM} = V _S /2	--	1	5	μV
VS Temperature (dV _{OS} /dT)	--	--	0.005	0.05	μV/°C
VS Power Supply (PSRR)	V _S = +2.5V to +5.5V, V _{CM} = 0	110	130	--	dB
Channel Separation, dc	--	--	0.1	--	μV/V
INPUT BIAS CURRENT					
Input Bias Current (I _B)	V _{CM} = V _S /2	--	50	--	pA
Input Offset Current (I _{OS})	--	--	10	--	pA
NOISE PERFORMANCE					
Input Voltage Noise (e _n p-p)	f=0.01Hz to 10Hz	--	1.3	--	μVpp
Input Voltage Noise (e _n p-p)	f=0.01Hz to 1Hz	--	0.4	--	uVpp
Input Voltage Noise Density (e _n)	f=1KHz	--	60	--	nV/√Hz
Input Current Noise Density (i _n)	f=10Hz	--	8	--	fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range (V _{CM})	--	(V-)-0.1	--	(V+)+0.1	V
Common-Mode Rejection Ratio (CMRR)	(V-) – 0.1V < V _{CM} < (V+) + 0.1V	110	130	--	dB
INPUT CAPACITANCE					
Differential	--	--	1	--	pF
Common-Mode	--	--	5	--	pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain (A _{OL})	R _L =10KΩ, V _O =0.3V to 4.7V, -40°C~125°C	110	130	--	dB
DYNAMIC PERFORMANCE					
Slew Rate (SR)	G=+1	--	0.7	--	V/μs
Gain-Bandwidth Product (GBW)	--	--	1.6	--	MHz
Overload Recovery Time	--	--	2	--	us
OUTPUT CHARACTERISTICS					
Output Voltage High (V _{OH})	R _L =100 KΩ to GND	4.99	4.998	--	V
	R _L =10 KΩ to GND	4.95	4.98	--	V

Output Voltage Low (V_{OL})	$R_L=100\text{ K}\Omega$ to $V+$	--	1	10	mV
	$R_L=10\text{ K}\Omega$ to $V+$	--	10	30	mV
Short-Circuit Current (I_{SC})	--	--	40	--	mA
POWER SUUOLY					
Operating Voltage Range	--	2.5		5.5	V
Quiescent Current (I_Q)	--	--	360	520	μA
SHUTDOWN					
TOFF	--	--	2	--	μs
TON	--	--	150	--	μs
V_L (shutdown)	--	0	--	+0.8	V
V_H (amplifier is active)	--	0.75($V+$)	--	$V+$	V
Input Bias Current of Enable Pin	--	--	50	--	pA
I_{QSD}	--	--	1	5	μA

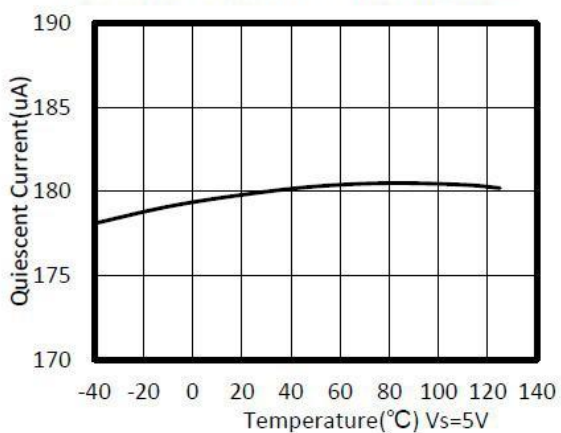
Typical Characteristics

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$, unless otherwise noted.

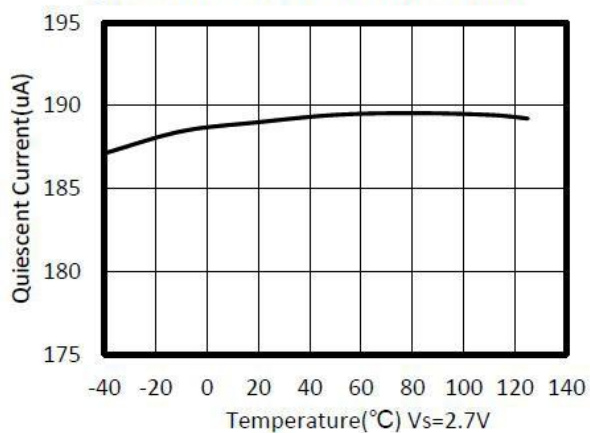


AT $T_A = +25^\circ\text{C}$ $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.

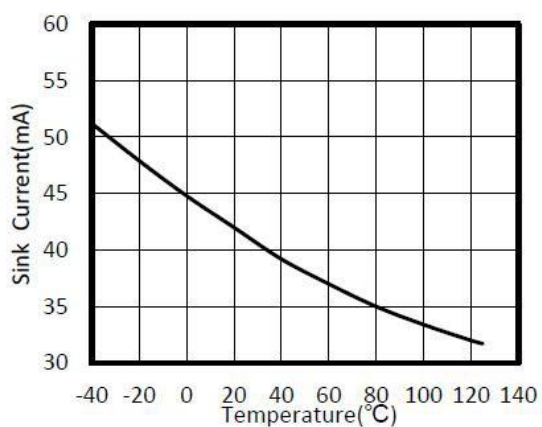
QUIESCENT CURRENT vs TEMPERATURE



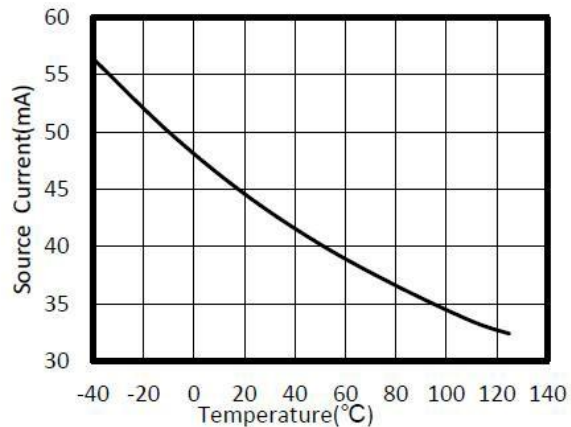
QUIESCENT CURRENT vs TEMPERATURE



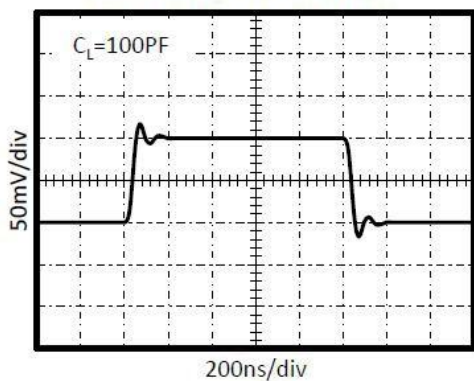
SINK CURRENT vs TEMPERATURE



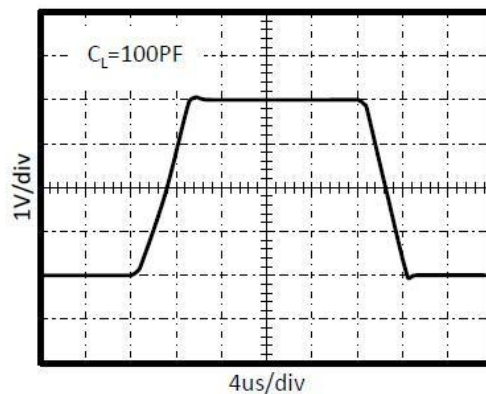
SOURCE CURRENT vs TEMPERATURE



SMALL-SIGNAL STEP RESPONSE

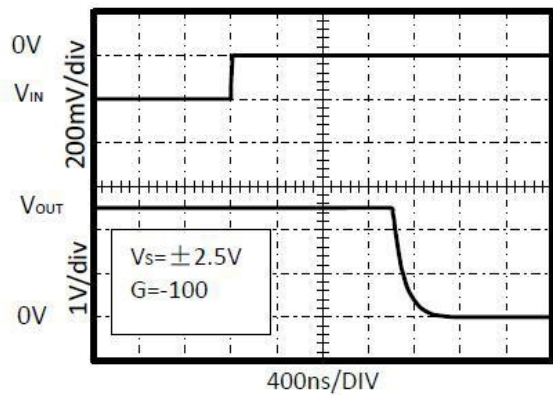


LARGE-SIGNAL STEP RESPONSE

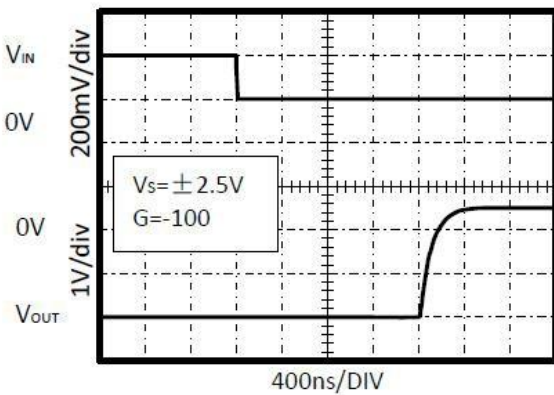


At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$, unless otherwise noted.

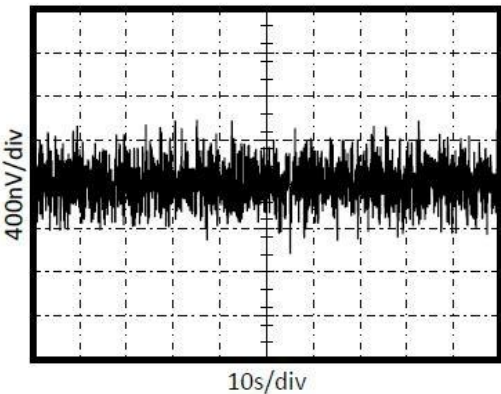
POSITIVE OVERVOLTAGE RECOVERY



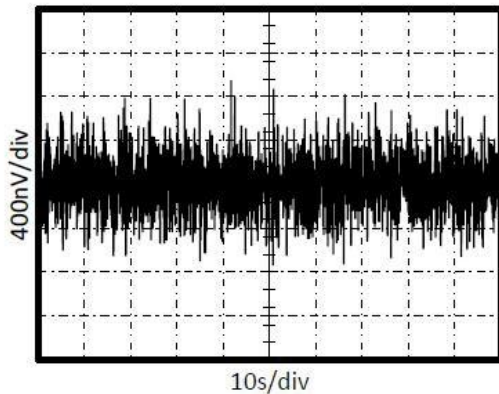
NEGATIVE OVERVOLTAGE RECOVERY



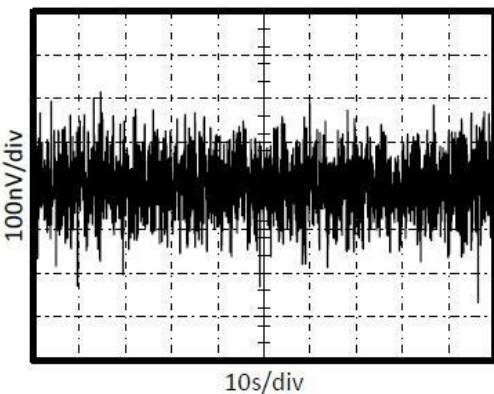
0.01Hz TO 10Hz NOISE AT $V_S=5V$



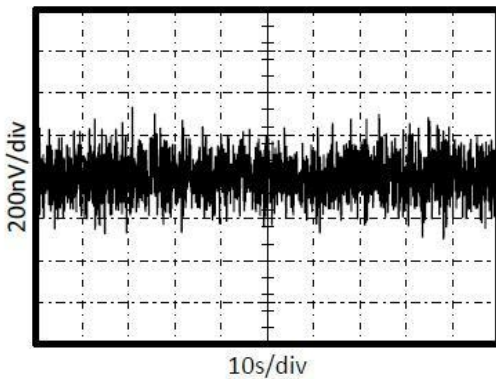
0.01Hz TO 10Hz NOISE AT $V_S=2.7V$



0.01Hz TO 1Hz NOISE AT $V_S=5V$



0.01Hz TO 1Hz NOISE AT $V_S=2.7V$



Application Information

The CD8538, CD8539 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a $0.1\mu\text{F}$ capacitor placed closely across the supply pins. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

Use low thermoelectric-coefficient connections (avoid dissimilar metals). Thermally isolate components from power supplies or other heat-sources. Shield op amp and input circuitry from air currents, such as cooling fans. Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of $0.1\mu\text{V}/^\circ\text{C}$ or higher, depending on materials used.

Operating Voltage

The CD8538, CD8539 series op amps operate over a power-supply range of $+2.5\text{V}$ to $+5.5\text{V}$ ($\pm 1.25\text{V}$ to $\pm 2.75\text{V}$). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a $0.1\mu\text{F}$ capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.

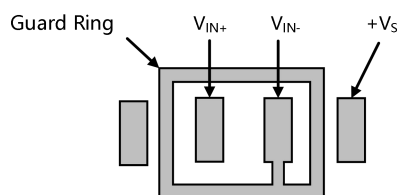
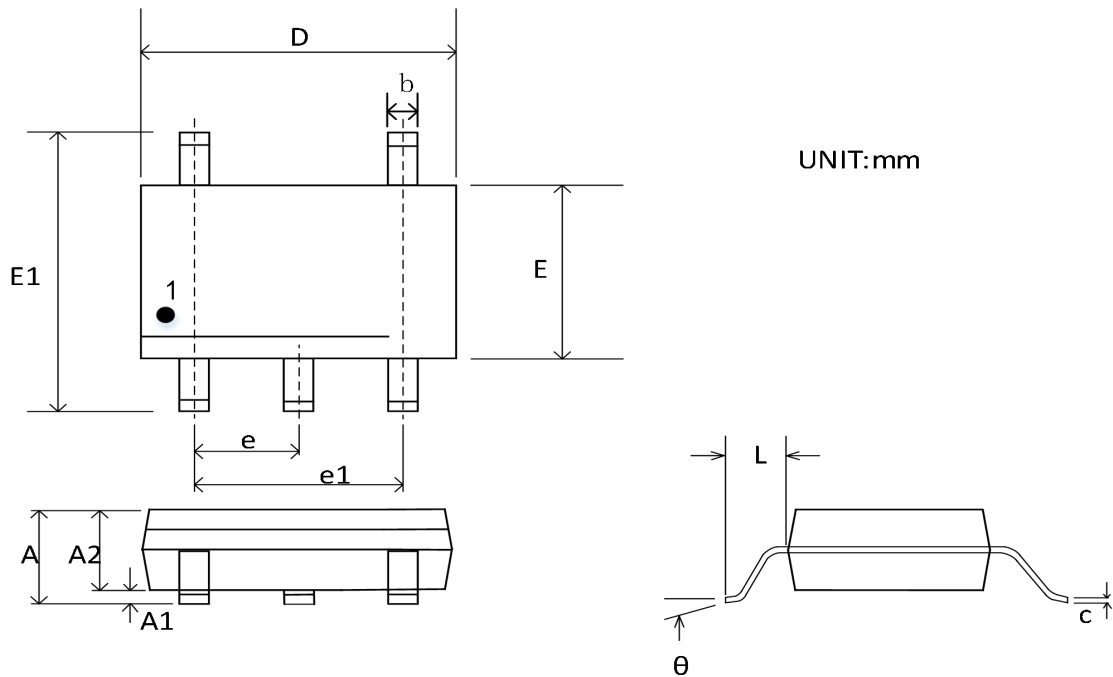


Figure 1. The Layout of Guard Ring

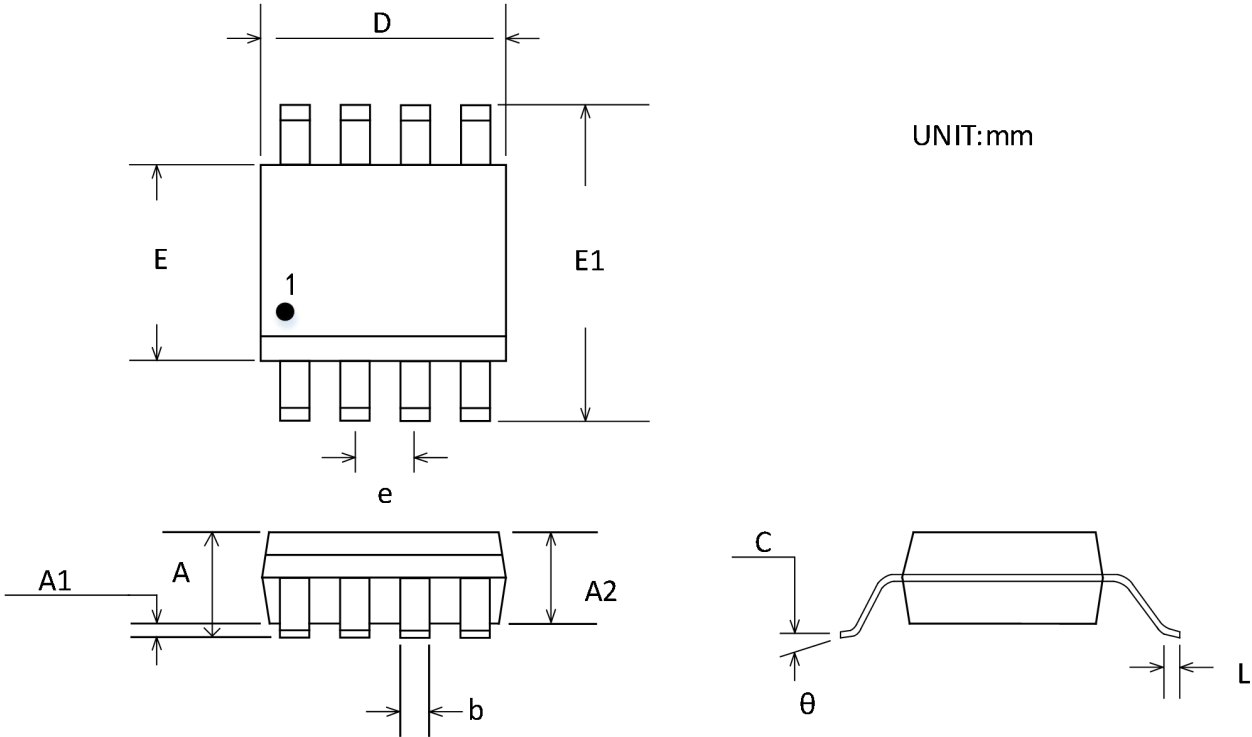
Package Outline Dimensions

SOT23-5



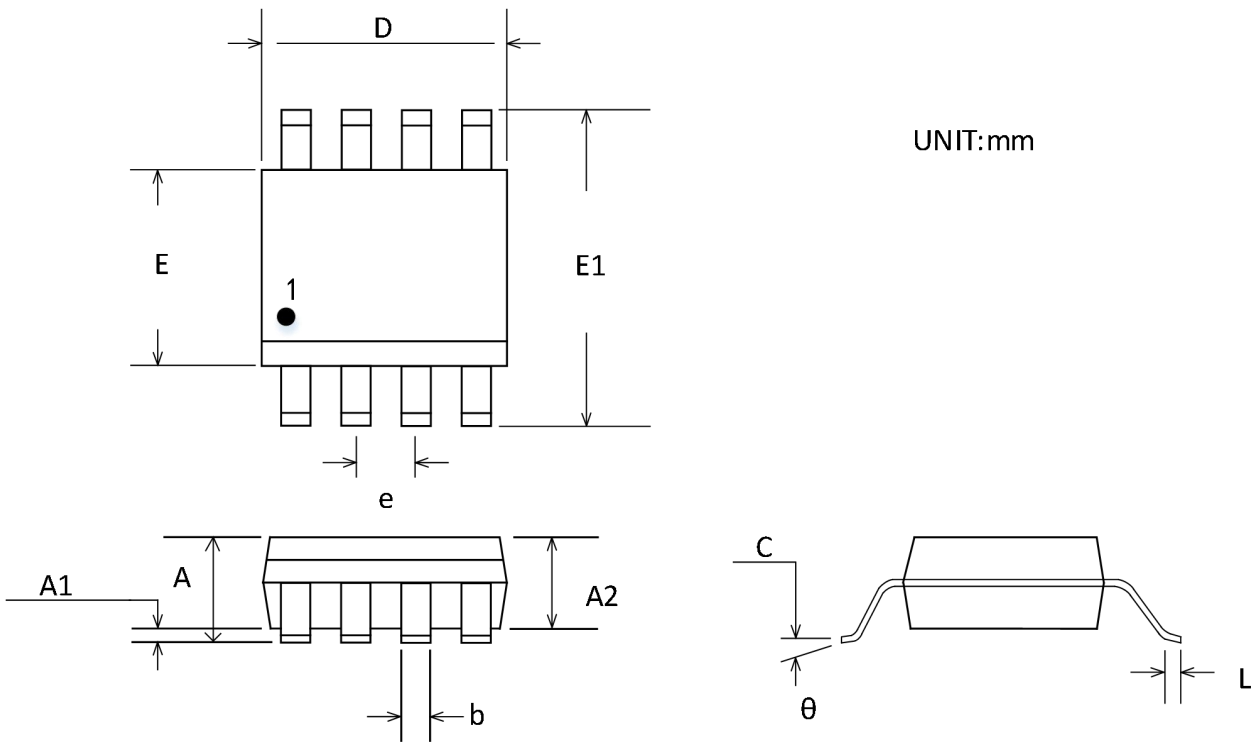
Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

MSOP-8



Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

SOP8



Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD8538AST5	-40°C~125°C	SOT23-5	Tape and Reel, 3000
CD8538AS8	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 2500
CD8538AS8-RL	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 3000
CD8538AS8-REEL	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 4000
CD8538AMS8	-40°C~125°C	MSOP-8	Tape and Reel, 3000
CD8539AS8	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 2500
CD8539AS8-RL	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 3000
CD8539AS8-REEL	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 4000
CD8539AMS8	-40°C~125°C	MSOP-8	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.5.26	Initial version	Regular update	WW	LYL	