



CD8557 CD8558 CD8559

Precision, Low Noise, CMOS, Rail-to-Rail, Input/Output Operational Amplifiers

Version: Rev 1.0.0 Date: 2025-6-3

Features ■■

- Low Offset Voltage: 20 μ V
- Input Offset Drift: 0.03 μ V/ $^{\circ}$ C
- High Gain Bandwidth Product: 4.3MHz
- Rail-to-Rail Input and Output
- High Gain, CMRR, PSRR:120dB
- High Slew Rate: 2.5V/ μ s
- Low Noise: 0.93 μ Vp-p (0.01~10Hz)
- Low Power Consumption: 650 μ A /op amp
- Overload Recovery Time:1 μ s
- Low Supply Voltage: +2.7 V to +5.5 V
- No External Capacitors Required
- Extended Temperature: -40 $^{\circ}$ C to +125 $^{\circ}$ C

Application ■■

- Temperature Sensors
- Medical/Industrial Instrumentation
- Pressure Sensors
- Battery-Powered Instrumentation
- Active Filtering
- Weight Scale Sensor
- Strain Gage Amplifiers
- Power Converter/Inverter

Description ■■

The CD8557, CD8558, CD8559 series of CMOS operational amplifiers use auto-zero techniques to simultaneously provide very low offset voltage (50 μ V max) and near-zero drift over time and temperature. This family of amplifiers has ultra low noise, offset and power.

This miniature, high-precision operational amplifiers offset high input impedance and rail-to-rail input and rail-to-rail output swing. With high gain-bandwidth product of 4.3MHz and slew rate of 2.5V/ μ s. Single or dual supplies as low as +2.7V ($\pm$ 1.35V) and up to +5.5V ($\pm$ 2.75V) may be used.

The CD8557/CD8558/CD8559 are specified for the extended industrial and automotive temperature range (-40 $^{\circ}$ C to 125 $^{\circ}$ C). The CD8557 single amplifier is available in 5-lead SOT23, 8-lead MSOP8 and 8-lead SOIC packages, The CD8558 dual amplifier is available in 8-lead SOIC and 8-lead MSOP narrow surface mount packages, The CD8559 quad amplifier is available in 14-lead SOIC and 14-lead narrow TSSOP packages.

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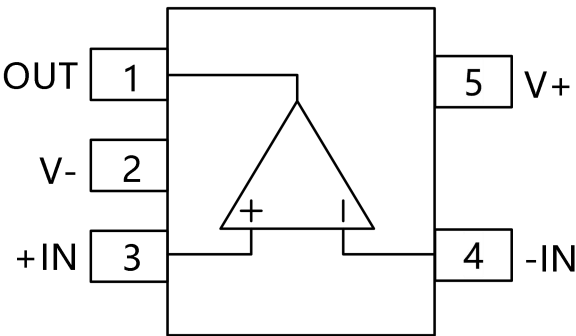
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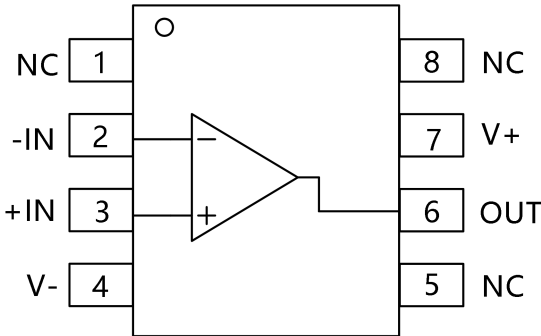
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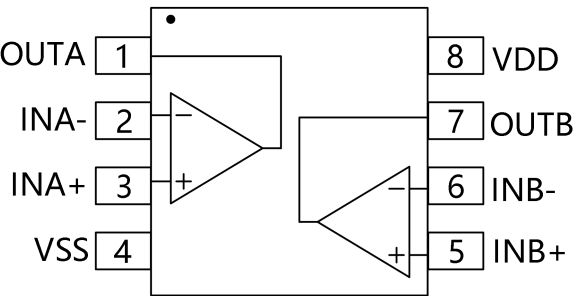
Pin Configurations



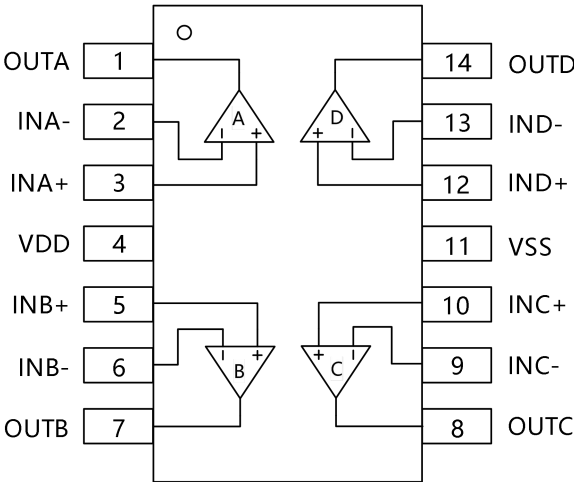
SOT23-5



SOIC-8(SOP8), MSOP-8



SOIC-8(SOP8), MSOP-8



SOIC-14(SOP14), TSSOP-14

Note : NC indicates no internal connection

Absolute Maximum Ratings

Parameter	Range
Supply Voltage (VS)	7V
Input Voltage	– 0.5 to (V+) + 0.5V
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature Range	–65°C to +150°C
Lead Temperature (Soldering,10 sec)	260°C
Package Thermal Resistance @ T_A= +25°C	
SOT23-5,SOT23-6	200°C/W

MSOP-10, SOIC-8	150°C/W
SOIC-14, TSSOP-14	100°C/W
HBM	8000V
MM	400V

Electrical characteristics

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

(At $T_A = +25^{\circ}\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.)

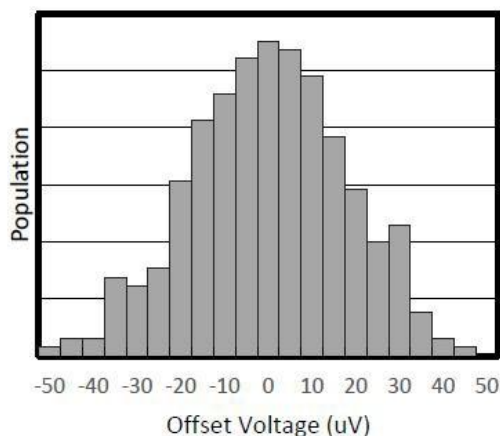
PARAMETER	CONDITION	CD8557, CD8558, CD8559			
		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Input Offset Voltage (V _{OS})	V _{CM} = V _S /2		20	50	μV
VS Temperature (dV _{OS} /dT)			0.03	0.2	μV/°C
VS Power Supply (PSRR)	V _S = +2.5V to +5.5V, V _{CM} = 0	110	120		dB
Channel Separation, dc			0.13		μV/V
INPUT BIAS CURRENT					
Input Bias Current (I _B)	V _{CM} = V _S /2		50		pA
Input Offset Current (I _{OS})			10		pA
NOISE PERFORMANCE					
Input Voltage Noise (e _n p-p)	f=0.01Hz to 10Hz		0.93		μVpp
Input Voltage Noise (e _n p-p)	f=0.01Hz to 1Hz		0.32		uVpp
Input Voltage Noise Density (e _n)	f=1KHz		45		nV/√Hz
Input Current Noise Density (i _n)	f=10Hz		2.3		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range (V _{CM})		(V-)-0.1		(V+)+0.1	V
Common-Mode Rejection Ratio (CMRR)	(V-) – 0.2V < V _{CM} < (V+)+ 0.2V	105	120		dB
INPUT CAPACITANCE					
Differential			1		pF
Common-Mode			5		pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain (A _{OL})	R _L =10KΩ,V _O =0.3V to 4.7V,-40°C ~125°C	110	120		dB
DYNAMIC PERFORMANCE					
Slew Rate (SR)	G = +1		2.5		V/μs
Gain-Bandwidth Product (GBW)			4.3		MHz

Overload Recovery Time			1		us
OUTPUT CHARACTERISTICS					
Output Voltage High (V _{OH})	R _L =100 KΩ to GND	4.99	4.99		V
	R _L =10 KΩ to GND	4.95	4.98		V
Output Voltage Low (V _{OL})	R _L =100 KΩ to V+		1	10	mV
	R _L =10 KΩ to V+		10	30	mV
Short-Circuit Current (I _{SC})			48		mA
POWER SUOOLY					
Operating Voltage Range		2.7		5.5	V
Quiescent Current (I _Q)			650	900	uA

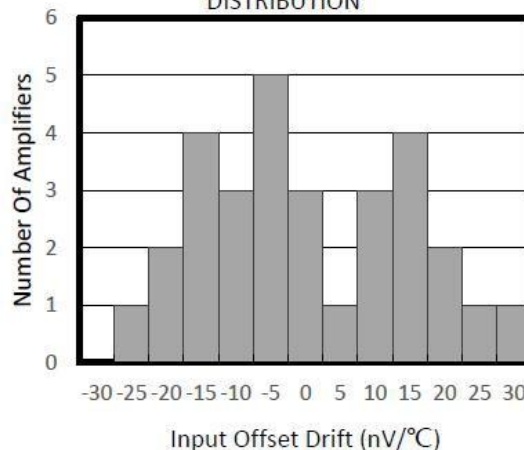
Typical Characteristics

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$, unless otherwise noted.

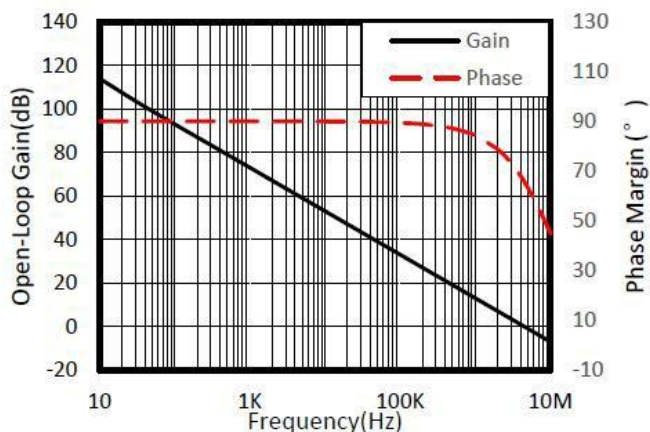
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



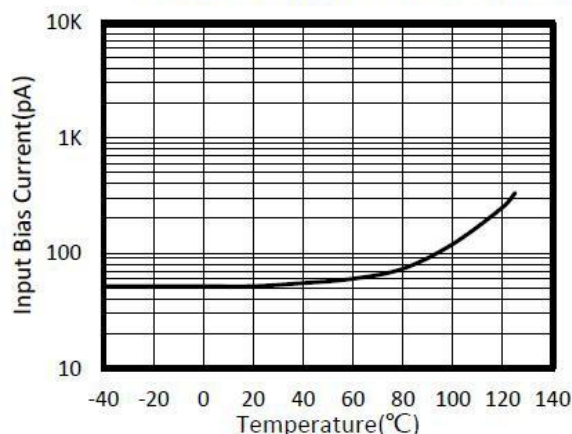
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



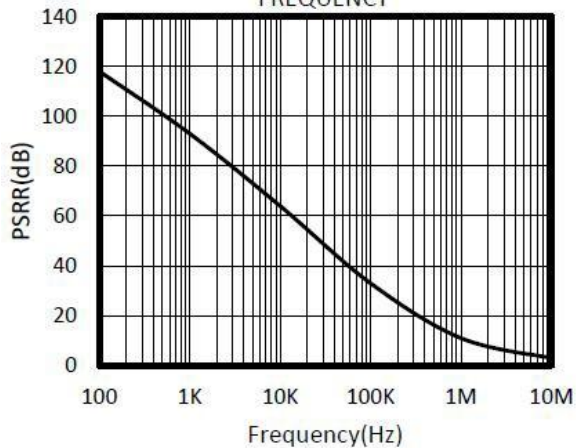
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



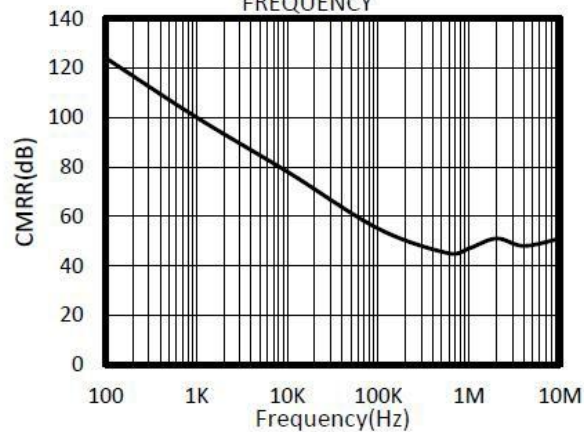
INPUT BIAS CURRENT vs TEMPERATURE

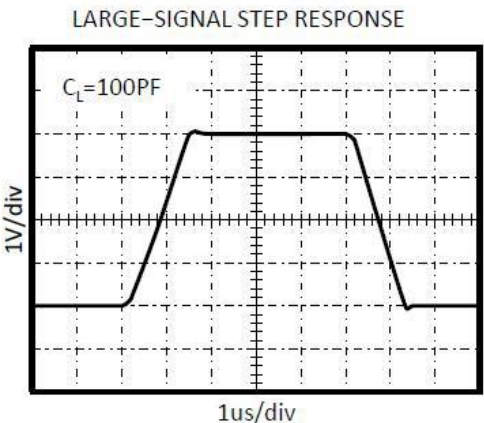
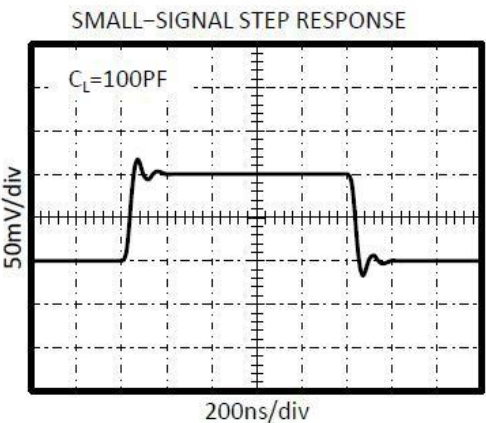
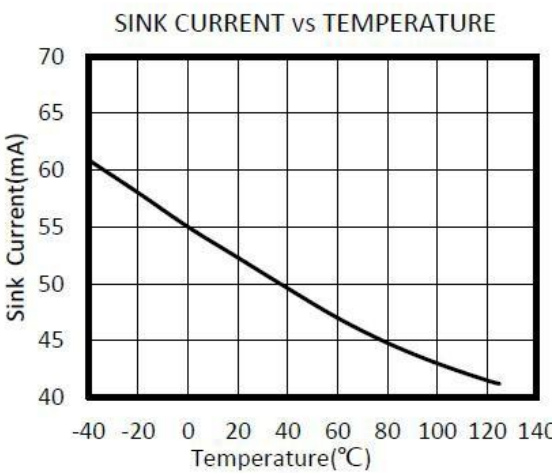
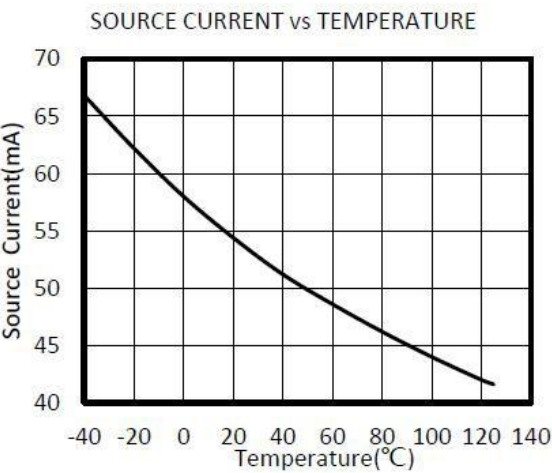
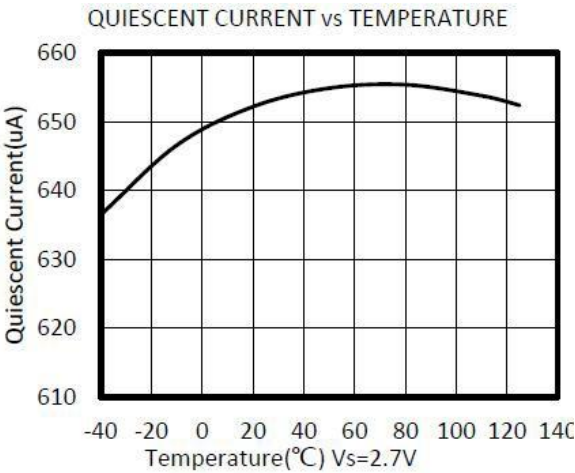
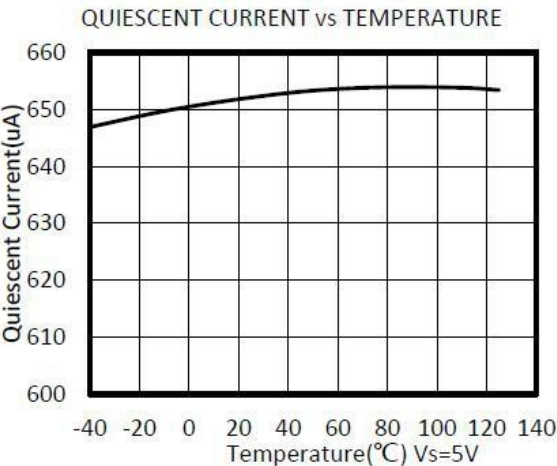


POWER-SUPPLY REJECTION RATIO vs FREQUENCY

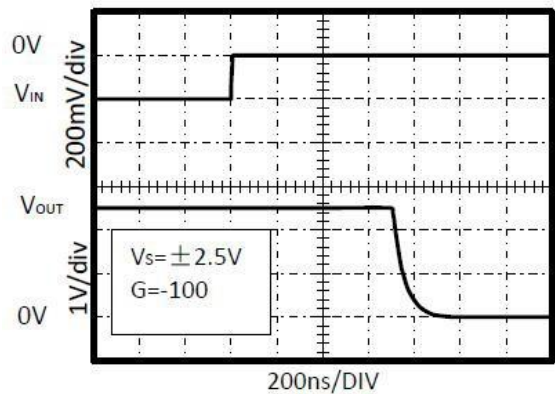


COMMON-MODE REJECTION RATIO vs FREQUENCY

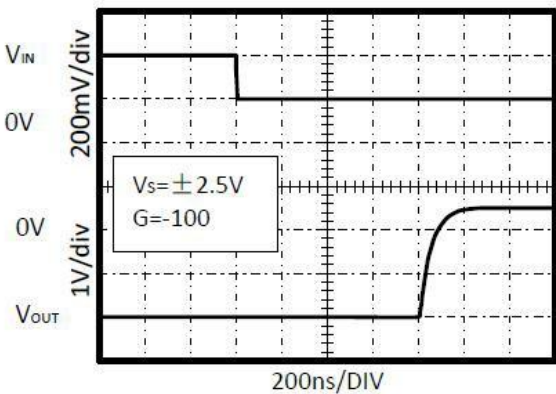




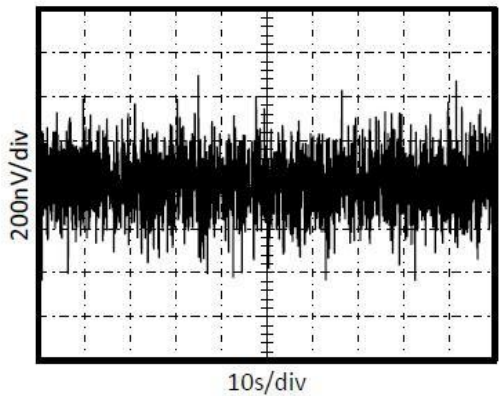
POSITIVE OVERVOLTAGE RECOVERY



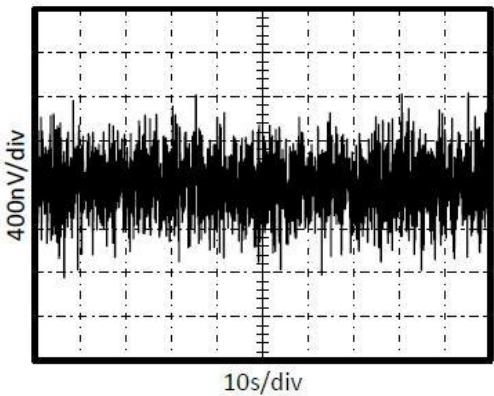
NEGATIVE OVERVOLTAGE RECOVERY



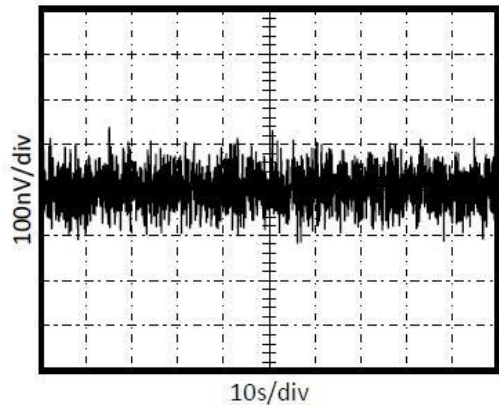
0.01Hz TO 10Hz NOISE AT $V_s=5V$



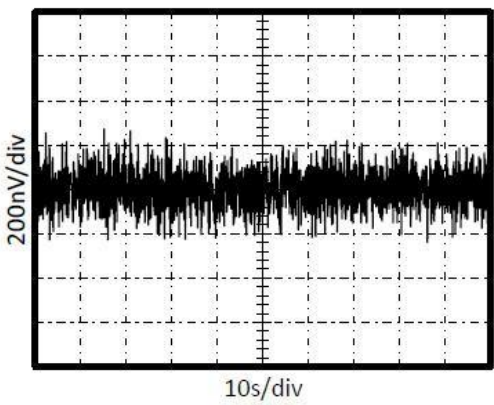
0.01Hz TO 10Hz NOISE AT $V_s=2.7V$



0.01Hz TO 1Hz NOISE AT $V_s=5V$



0.01Hz TO 1Hz NOISE AT $V_s=2.7V$



Application Information

The CD8557, CD8558, CD8559, series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a $0.1\mu\text{F}$ capacitor placed closely across the supply pins. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals. Use low thermoelectric coefficient connections (avoid dissimilar metals). Thermally isolate components from power supplies or other heat-sources. Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of $0.1\mu\text{V}/^\circ\text{C}$ or higher, depending on materials used.

Operating Voltage

The CD8557, CD8558, CD8559, series op amps operate over a power-supply range of $+2.7\text{V}$ to $+5.5\text{V}$ ($\pm 1.35\text{V}$ to $\pm 2.75\text{V}$). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a $0.1\mu\text{F}$ capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.

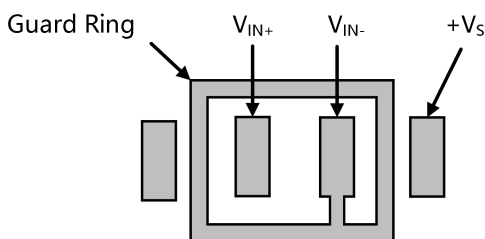
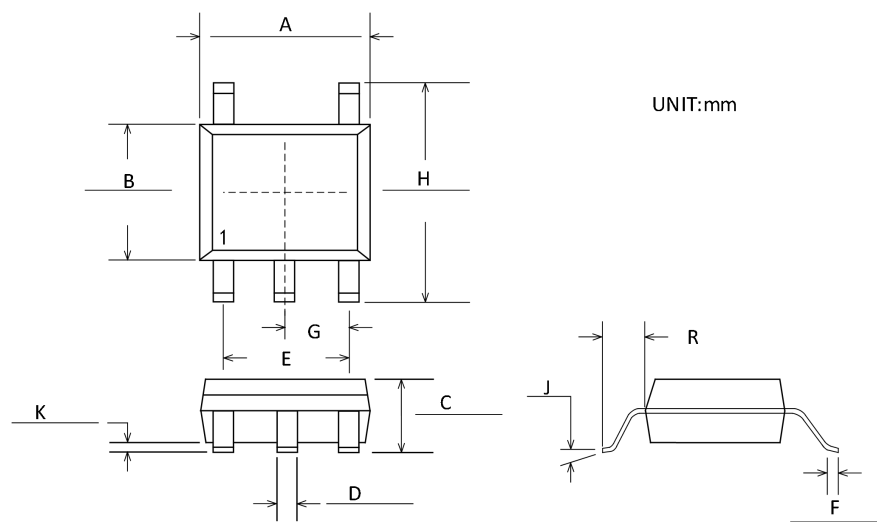


Figure 1. The Layout of Guard Ring

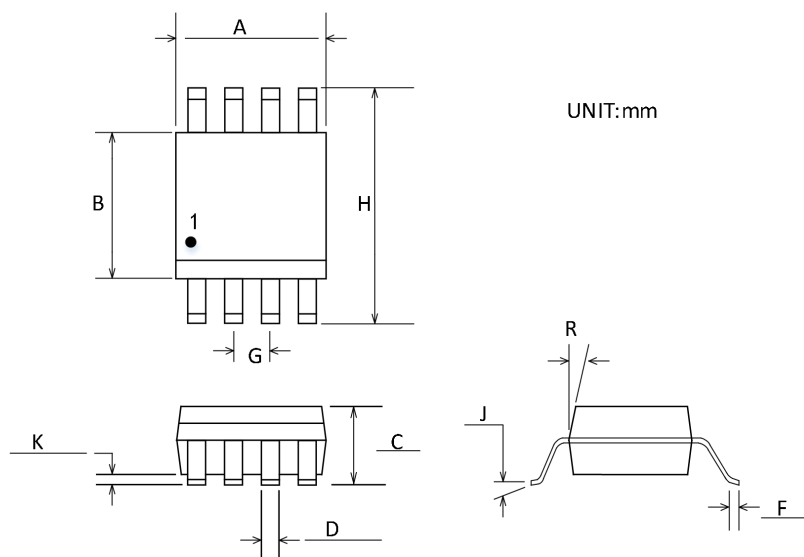
Package Outline Dimensions

SOT23-5



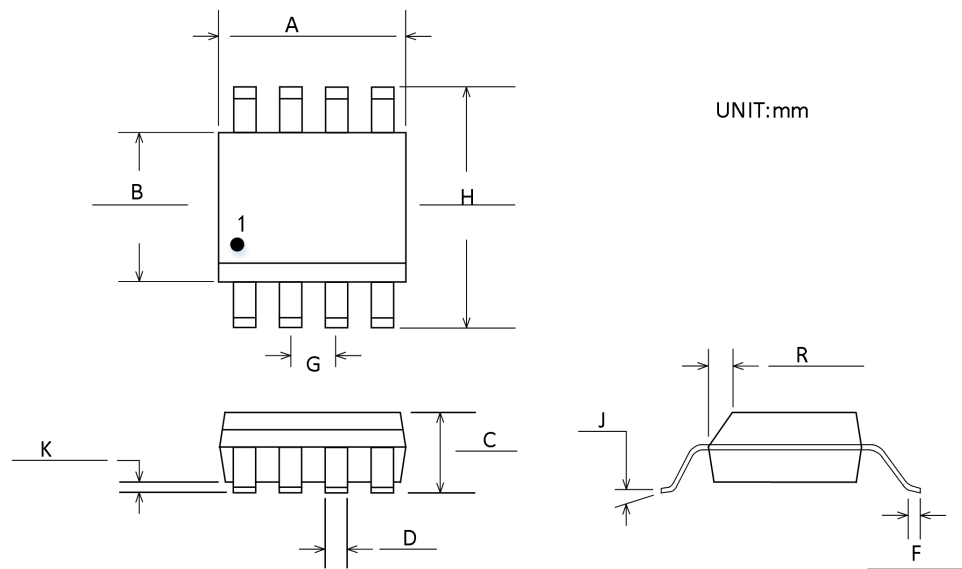
Symbol	Dimensions In Millimeters	
	Min	Max
A	2.80	3.00
B	1.50	1.70
C	0.95	1.45
D	0.35	0.50
E	1.90BSC	
F	0.35	0.55
G	0.95BSC	
H	2.60	3.00
J	0°	10°
K	0.05	0.15
R	0.60BSC	

MSOP-8



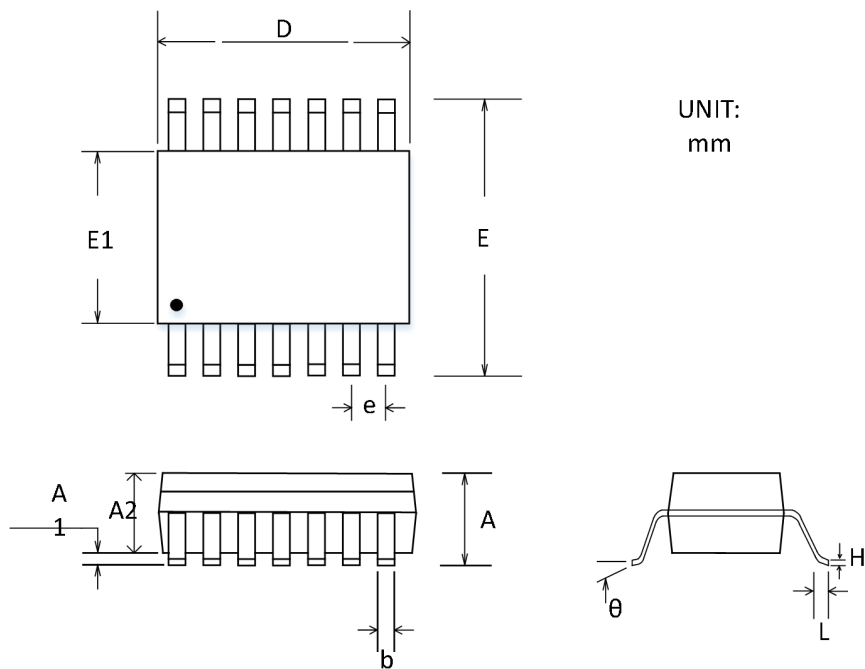
Symbol	Dimensions In Millimeters	
	Min	Max
A	2.80	3.20
B	2.80	3.20
C	1.10MAX	
D	0.25	0.40
F	0.40	0.80
G	0.65BSC	
H	4.65	5.15
J	0°	6°
K	0.05	0.15
R	15°MAX	

SOP-8



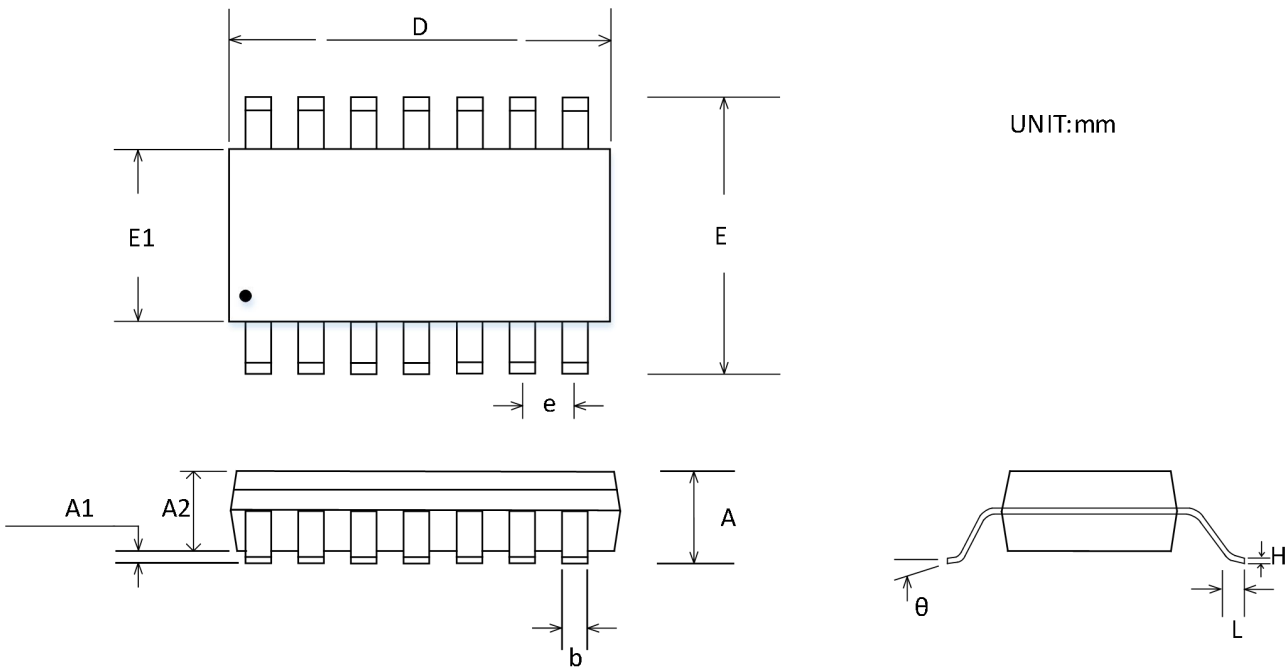
Symbol	Dimensions In Millimeters	
	Min	Max
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.31	0.51
F	0.40	1.27
G	1.27BSC	
H	5.80	6.20
J	0°	8°
K	0.10	0.25
R	0.25	0.50

TSSOP-14



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.20MAX	
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
D	4.90	5.10
E	6.40BSC	
E1	4.30	4.50
e	0.65BSC	
H	0.09	0.20
L	0.45	0.75
θ	0°	8°

SOP-14



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
b	0.31	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.27BSC	
H	0.17	0.25
L	0.40	1.27
θ	0°	8°

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD8557AST5	-40°C~125°C	SOT23-5	Tape and Reel, 3000
CD8557AS8	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 2500
CD8557AS8-RL	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 3000
CD8557AS8-REEL	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 4000
CD8557AMS8	-40°C~125°C	MSOP-8	Tape and Reel, 3000
CD8558AS8	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 2500
CD8558AS8-RL	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 3000
CD8558AS8-REEL	-40°C~125°C	SOIC-8(SOP8)	Tape and Reel, 4000
CD8558AMS8	-40°C~125°C	MSOP-8	Tape and Reel, 3000
CD8559AS14	-40°C~125°C	SOIC-14(SOP14)	Tape and Reel, 2500
CD8559AS14-RL	-40°C~125°C	SOIC-14(SOP14)	Tape and Reel, 3000
CD8559AS14-REEL	-40°C~125°C	SOIC-14(SOP14)	Tape and Reel, 4000
CD8559ATS14	-40°C~125°C	TSSOP-14	Tape and Reel, 2500
CD8559ATS14-RL	-40°C~125°C	TSSOP-14	Tape and Reel, 3000
CD8559ATS14-REEL	-40°C~125°C	TSSOP-14	Tape and Reel, 4000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.3	Initial version	Regular update	WW	LYL	