CoreadDvices
承芯微电子

CD8655_CD8656

Low Noise, Precision CMOS Amplifier

Version: Rev 1.0.0 Date: 2025-5-26

Features

- Low noise: 2.7nV/√Hz at f = 10 kHz
- Low offset voltage: 250 µV max over VCM
- Offset voltage drift: 0.4 µV/°C typ and 2.3µV/°
- Bandwidth: 28 MHz
- Rail-to-rail input/output
- Unity gain stable
- 2.7 V to 5.5 V operation
- −40°C to +125°C operation

Application

- ADC and DAC buffers
- Audio
- Industrial controls
- Precision filters
- Digital scales
- Automotive collision avoidance
- PLL filters

Description

The CD8655/CD8656 are the industry's lowest noise, precision CMOS amplifiers. They can achieve high dc accuracy.

The CD8655/CD8656 provide low noise (2.7 at 10 kHz), low THD + N (0.0007%), and high precision performance (250 µV max over VCM) to low voltage applications. The ability to swing rail-to-rail at the input and output enables designers to buffer analog-to-digital converters (ADCs) and other wide dynamic range devices in single- supply systems.

The high precision performance of the CD8655/CD8656 improves the resolution and dynamic range in low voltage applications. Audio applications, such as microphone pre-amps and audio mixing consoles, benefit from the low noise, low distortion, and high output current capability of the CD8655/CD8656 to reduce system level noise performance and maintain audio fidelity. The high precision and rail-to-rail input and output of the CD8655/ CD8656 benefit data acquisition, process controls, and PLL filter applications.

The CD8655/CD8656 are fully specified over the −40°C to+125°C temperature range. The CD8655/CD8656 are available in Pb- free, 8-lead MSOP and SOIC packages. The CD8655/CD8656 are both available for automotive applications.

Chinese version:CD8655_CD8656

Contents

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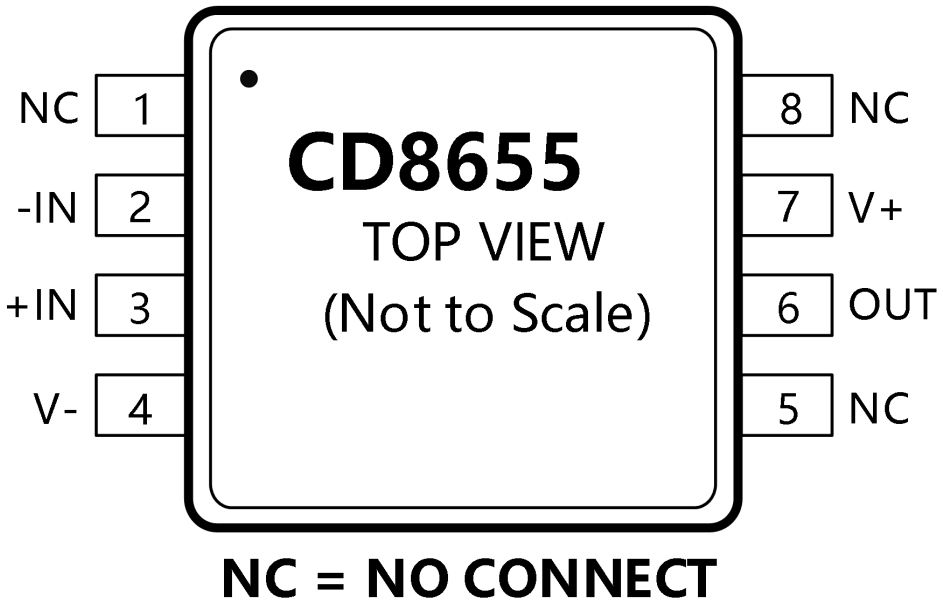
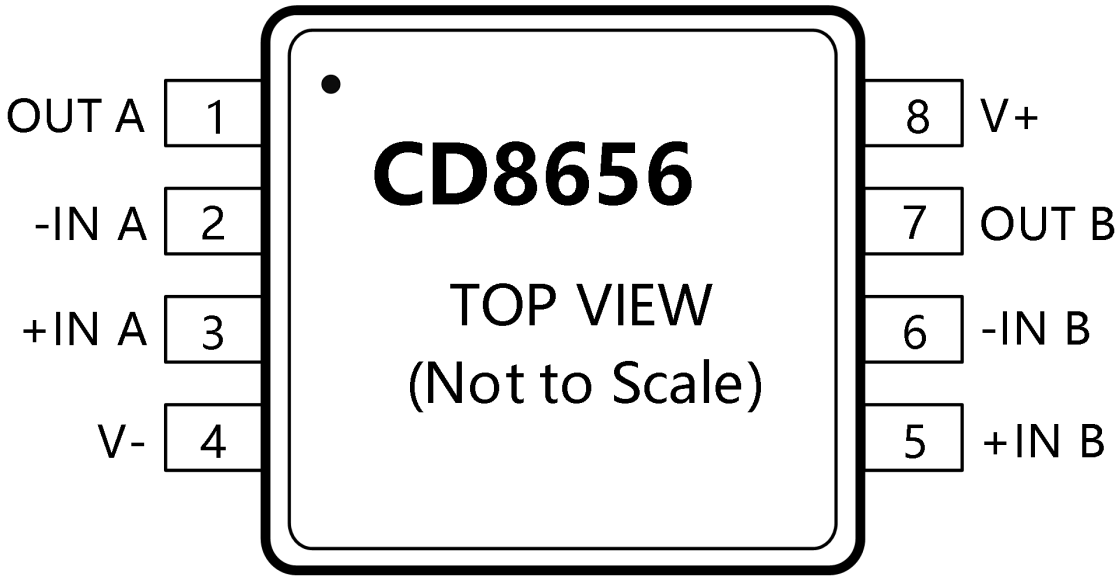
Pin Configurations



8-Lead MSOP (RM-8)
8-Lead SOIC (R-8)
Figure 1. CD8655



8-Lead MSOP (RM-8)
8-Lead SOIC (R-8)
Figure 2. CD8656

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	6V
Input Voltage	VSS−0.3V to VDD+0.3V
Differential Input Voltage	±6 V
Output Short-Circuit Duration to GND	Indefinite
Electrostatic Discharge (HBM)	3.0kV
Storage Temperature Range R, RM Packages	−65℃ to +150℃
Junction Temperature Range R, RM Packages	−65℃ to +150℃
Lead Temperature (Soldering,10 sec)	260℃
8-Lead MSOP (RM)	θ_{JA}: 210℃/W θ_{JC}: 45℃/W
8-Lead SOIC (R)	θ_{JA}: 158℃/W θ_{JC}: 43℃/W

Electrical characteristics

V_S=2.7V, V_{CM}=V_S/2, T_A=25℃, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM}=0V to 2.7V	--	44	250	μV
		−40℃≤T_A≤+125℃	--	--	550	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta_T$	−40℃≤T_A≤+125℃	--	0.4	2.0	μV/℃
Input Bias Current	I_B	--	--	1	10	pA
		−40℃≤T_A≤+125℃	--	--	500	pA
Input Offset Current	I_{OS}	--	--	--	10	pA
		−40℃≤T_A≤+125℃	--	--	500	pA
Input Voltage Range	--	--	0	--	2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=0V to 2.7V	80	98	--	dB
Large Signal Voltage Gain	A_{VO}	V_O=0.2V to 2.5V, R_L=10kΩ, V_{CM}=0V	98	--	--	dB
		−40℃≤T_A≤+125℃	90	--	--	dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L=1mA;−40℃≤T_A≤+125℃	2.67	2.688	--	V

Output Voltage Low	V_{OL}	I_L=1mA;−40℃≤T_A≤+125℃	--	10	30	mV
Output Current	I_{OUT}	V_{OUT}=±0.5V	--	±75	--	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S=2.7V to 5.0V	88	105		dB
Supply Current/Amplifier	I_{SY}	V_O=0V	--	3.7	4.5	mA
		−40℃≤T_A≤+125℃	--	--	5.3	mA
INPUT CAPACITANCE	C_{IN}					
Differential	--	--	--	9.3	--	pF
Common-Mode	--	--	--	16.7	--	pF
NOISE PERFORMANCE						
Input Voltage Noise Density	en	f=1kHz	--	4	--	$\mathbf{nV}/\sqrt{\boldsymbol{Hz}}$
		f=10kHz	--	2.7	--	$\mathbf{nV}/\sqrt{\boldsymbol{Hz}}$
Total Harmonic Distortion+Noise	THD+N	G=1, R_L=1kΩ, f=1kHz,	--	0.0007	--	%
		V_{IN}=2V p-p	--	--	--	
FREQUENCY RESPONSE						
Gain Bandwidth Product	GBP		--	27	--	MHz
Slew Rate	SR	R_L=10kΩ	--	8.5	--	V/μs
Settling Time	ts	To 0.1%, V_{IN}=0V to 2V step, G=+1	--	370	--	ns
Phase Margin	--	C_L=0pF	--	54	--	degrees

Typical Characteristics

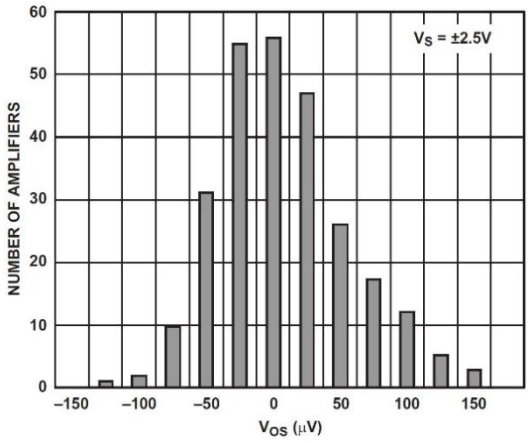


Figure 3. Input Offset Voltage Distribution

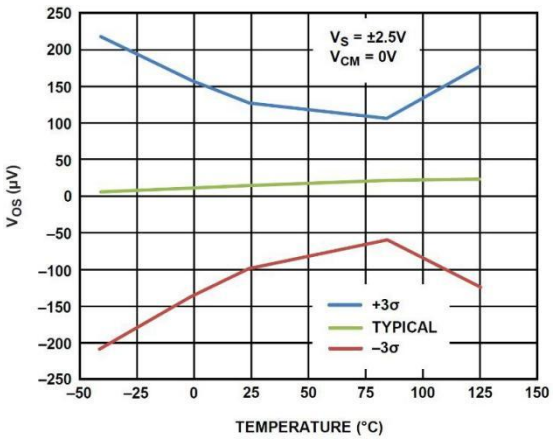


Figure 4. Input Offset Voltage vs.Temperature

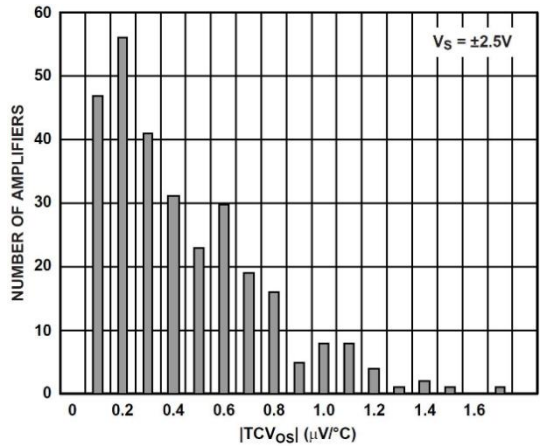


Figure 5. | TCV_{OS} | Distribution

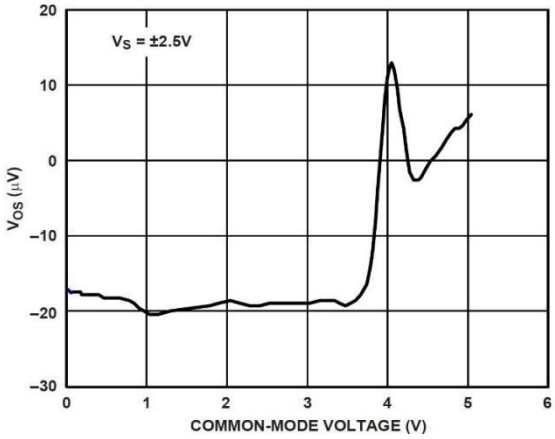


Figure 6. Input Offset Voltage vs. Common-Mode Voltage

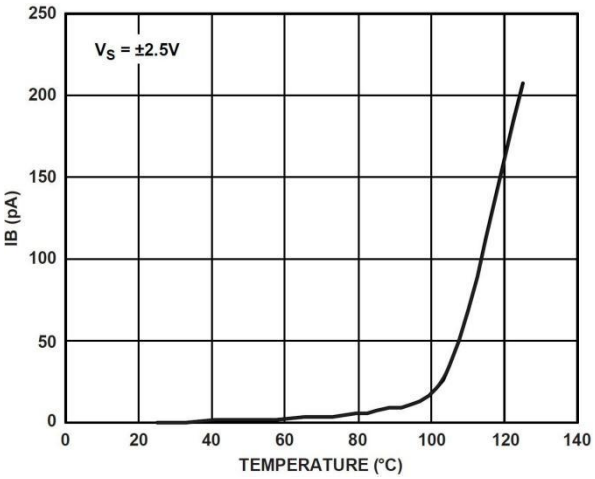


Figure 7. Input Bias Current vs. Temperature

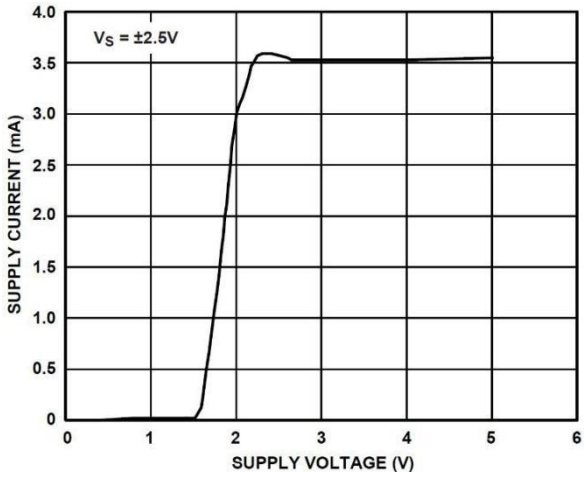


Figure 8. Supply Current vs. Supply Voltage

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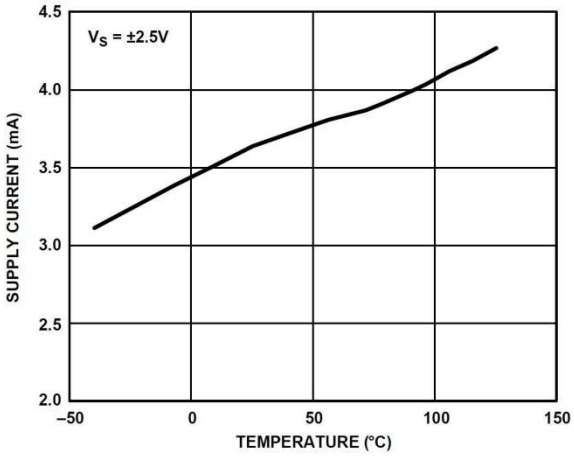
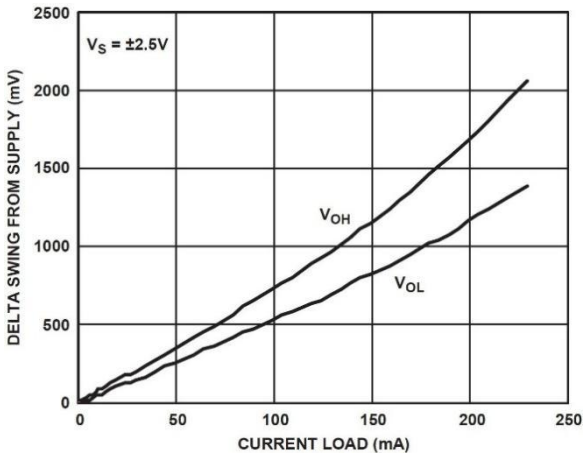


Figure 9. Supply Current vs. Temperature Figure



10. CD8655 Output Voltage to Supply Rail vs. Current Load

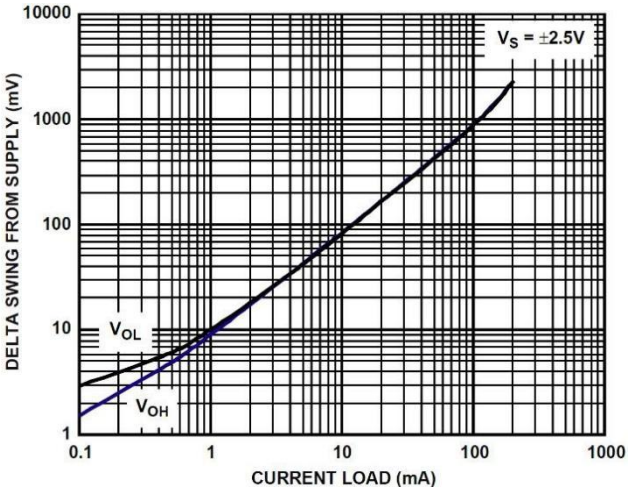
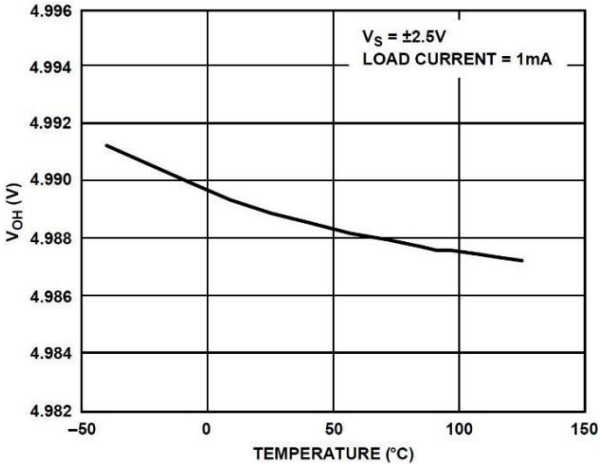


Figure 11. CD8656 Output Swing vs. Current Load Figure



12. Output Voltage Swing High vs. Temperature

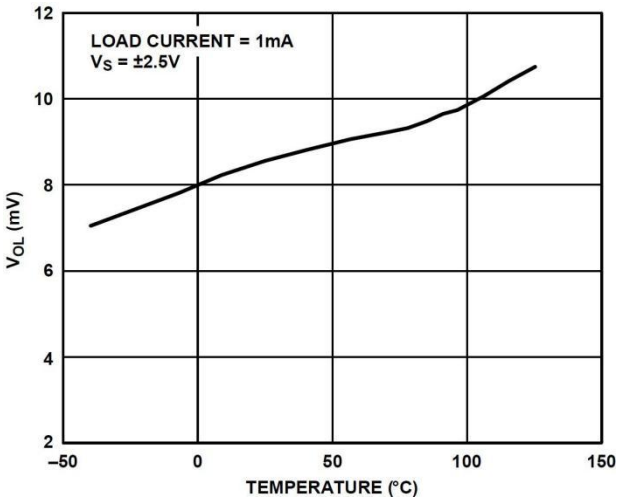
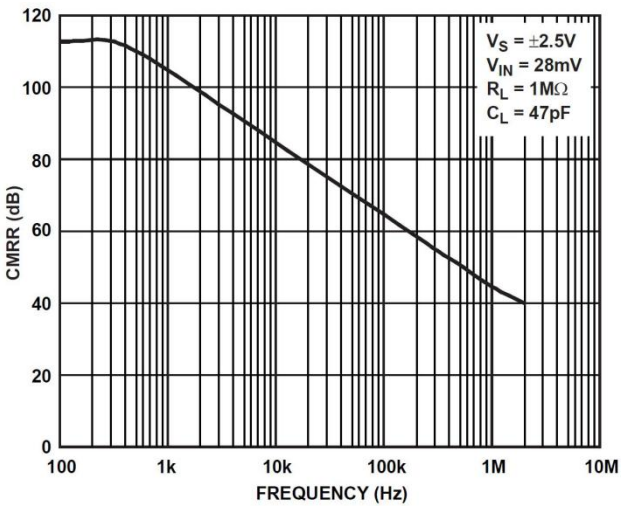


Figure 13. Output Voltage Swing Low vs. Temperature Figure



14. CMRR vs. Frequency

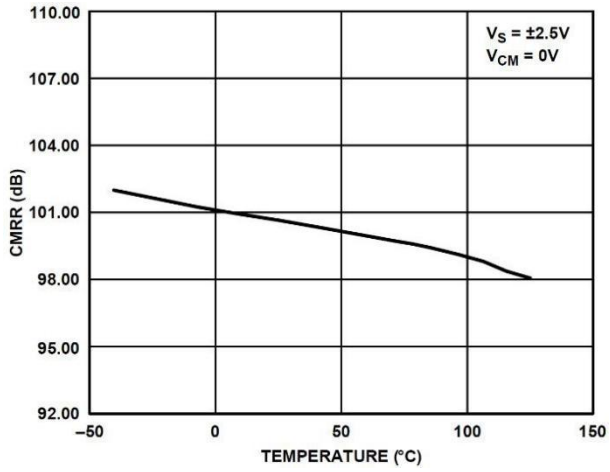


Figure 15. Large Signal CMRR vs. Temperature

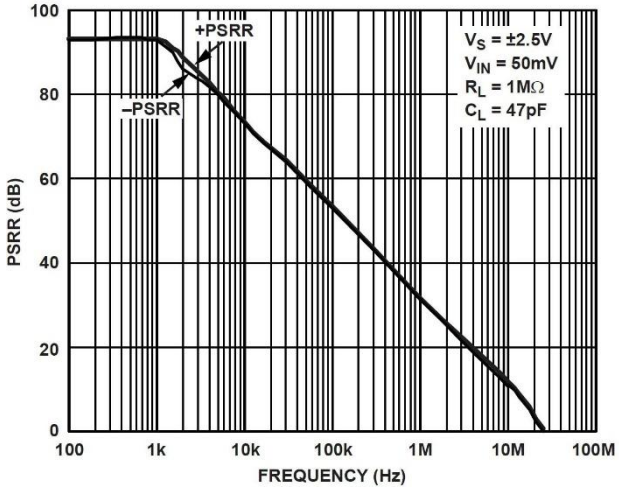


Figure 16. Small Signal PSSR vs. Frequency

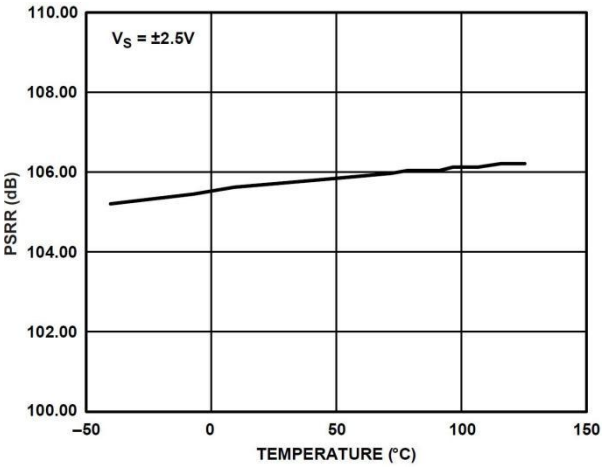


Figure 17. Large Signal PSSR vs. Temperature

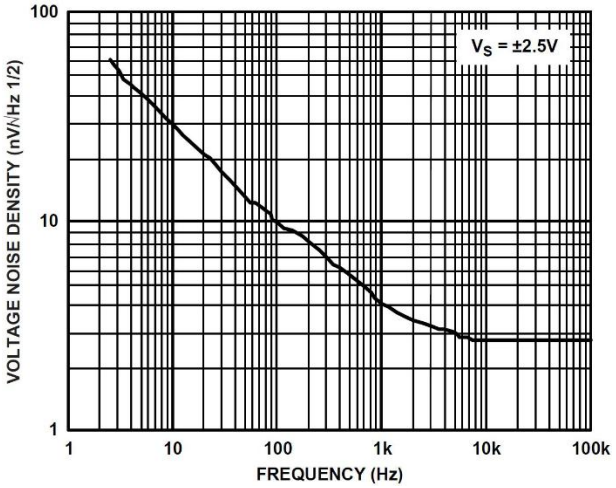


Figure 18. Voltage Noise Density vs. Frequency

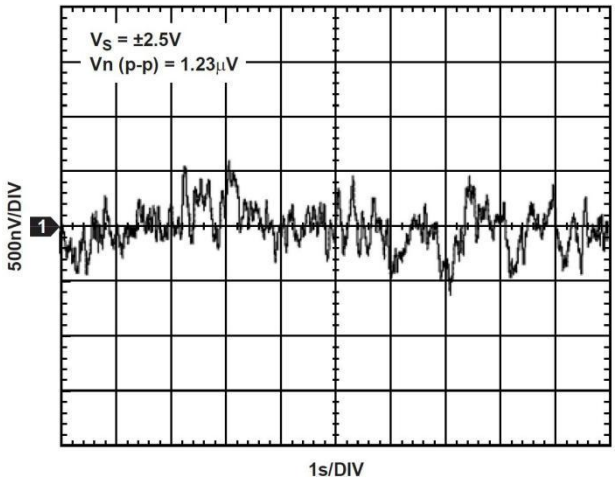
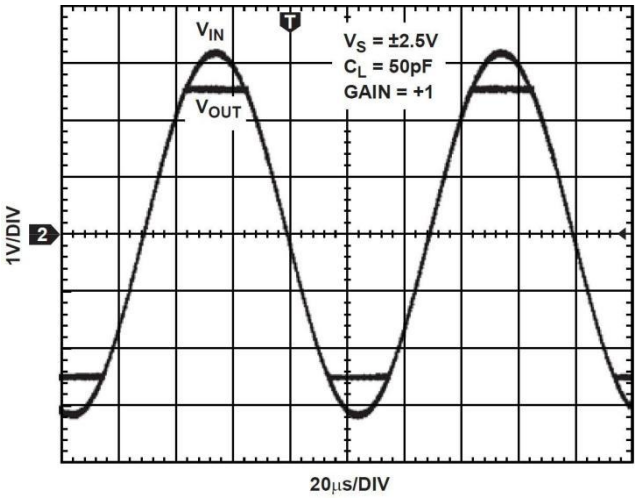


Figure 19. Low Frequency Noise (0.1 Hz to 10 Hz) Figure



20. No Phase Reversal

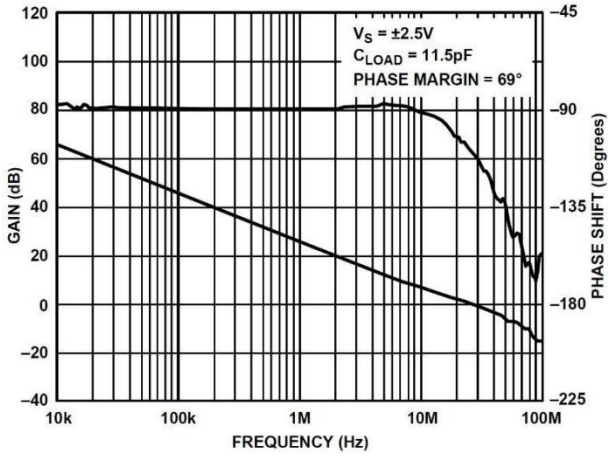


Figure 21. Open-Loop Gain and Phase vs. Frequency

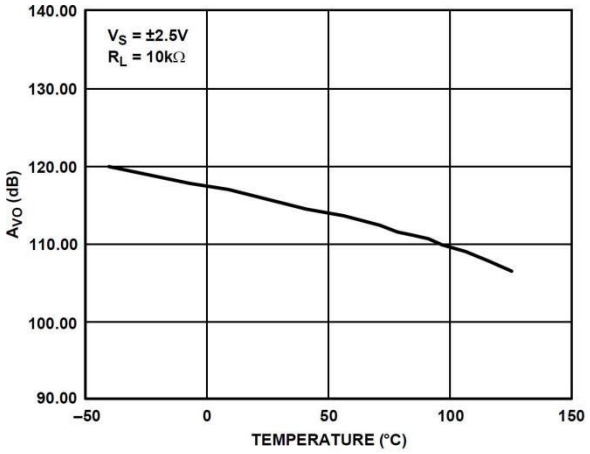


Figure 22. Large Signal Open-Loop Gain vs. Temperature

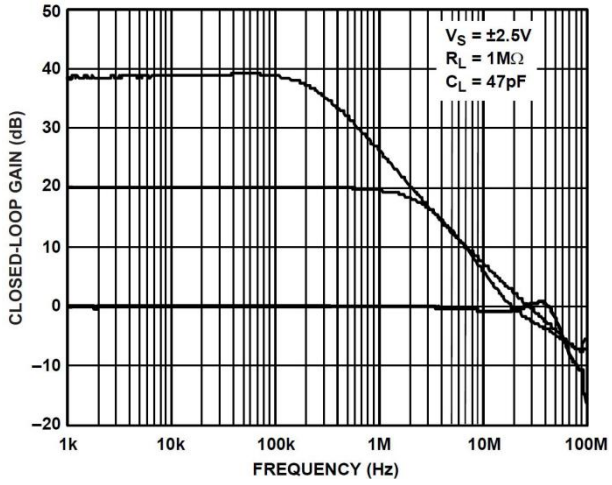
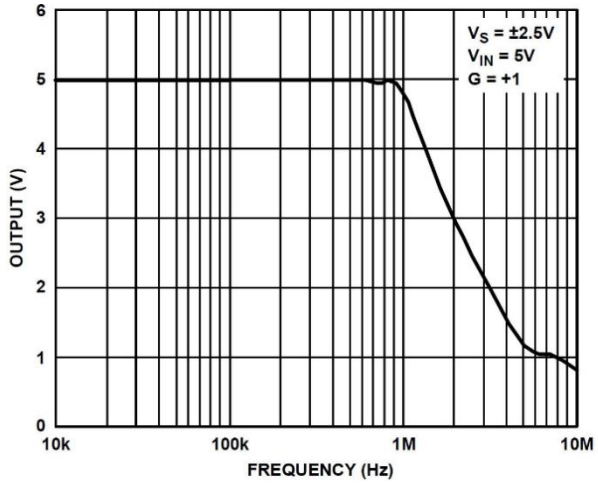


Figure 23. Closed-Loop Gain vs. Frequency Figure



24. Maximum Output Swing vs. Frequency

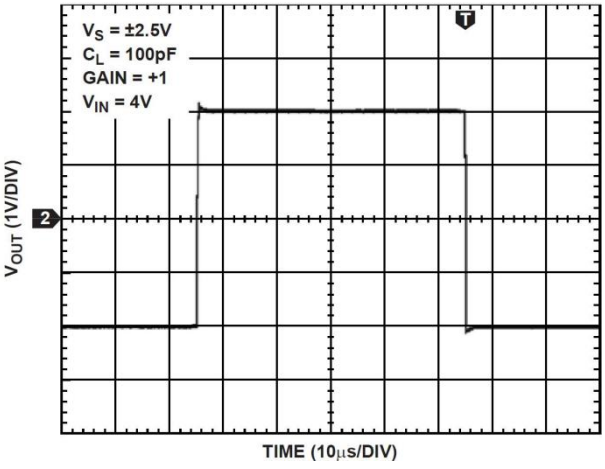
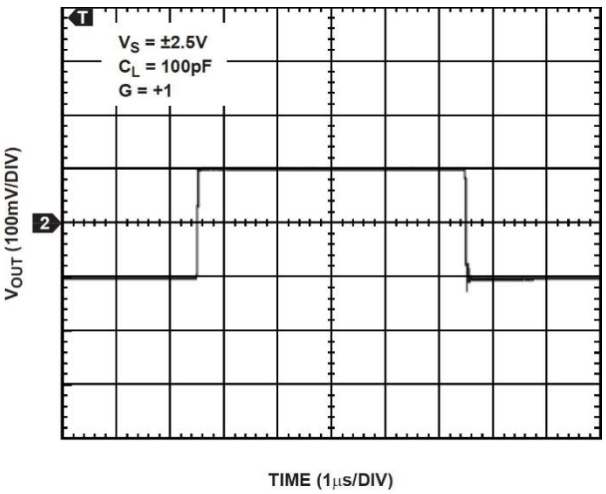


Figure 25. Large Signal Response Figure



26. Small Signal Response

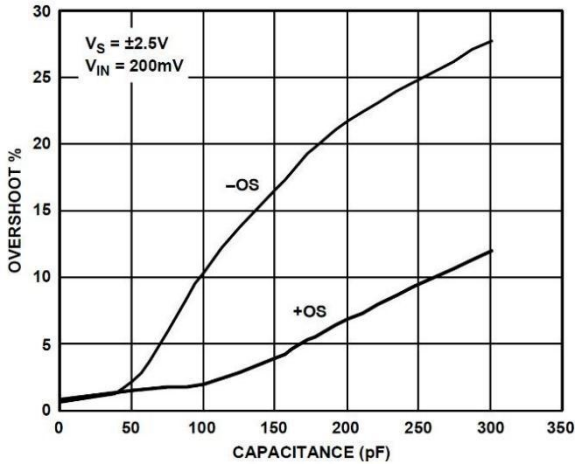
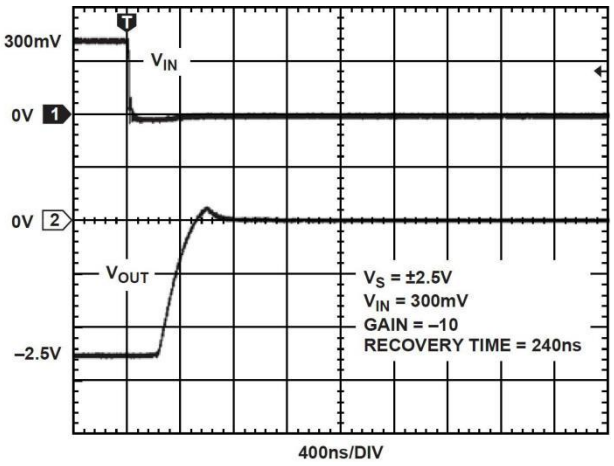


Figure 27. Small Signal Overshoot vs. Load Capacitance Figure



28. Negative Overload Recovery Time

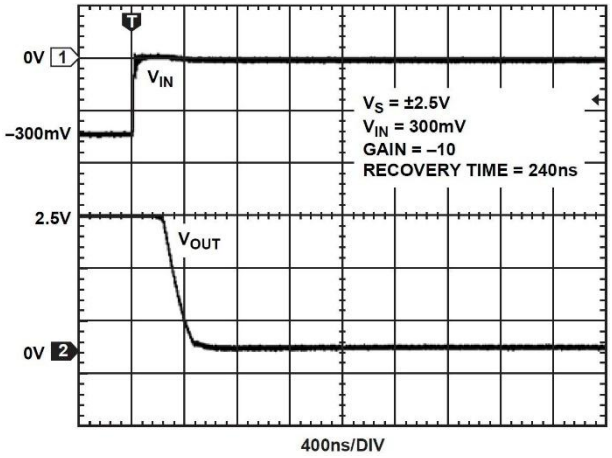


Figure 29. Positive Overload Recovery Time

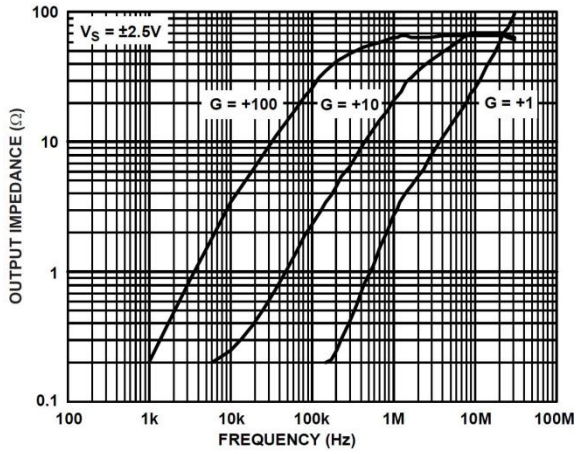


Figure 30. Output Impedance vs. Frequency

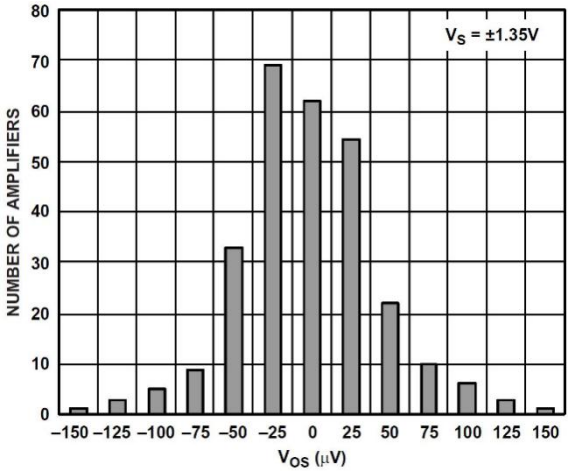


Figure 31. Input Offset Voltage Distribution

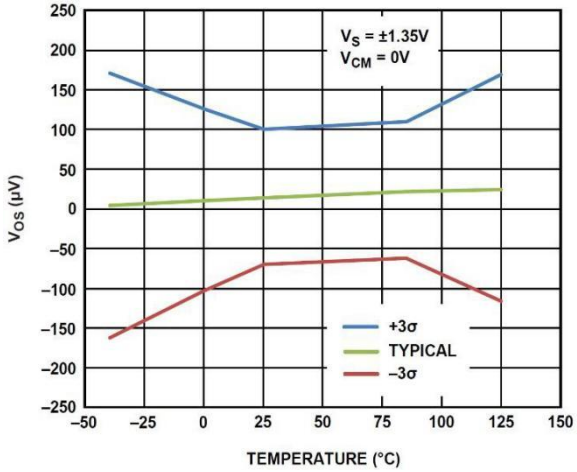


Figure 32. Input Offset Voltage vs. Temperature

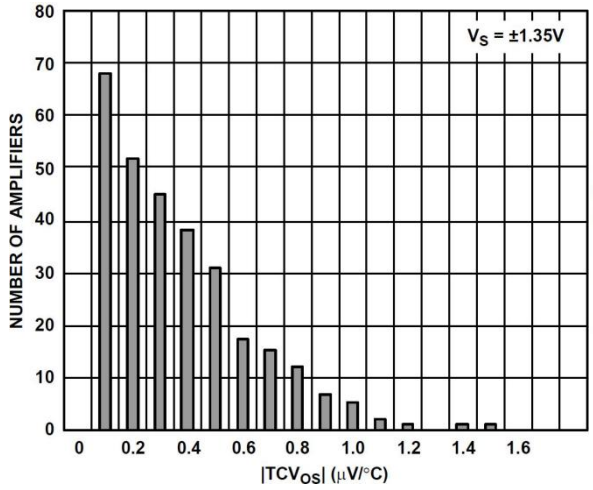


Figure 33. |TCVOS| Distribution

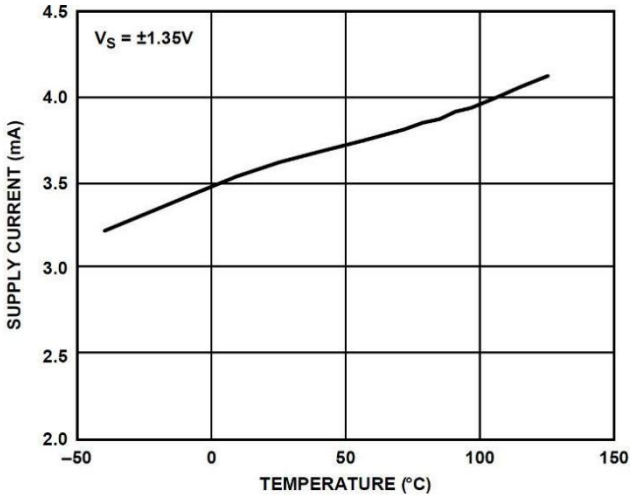


Figure 34. Supply Current vs. Temperature

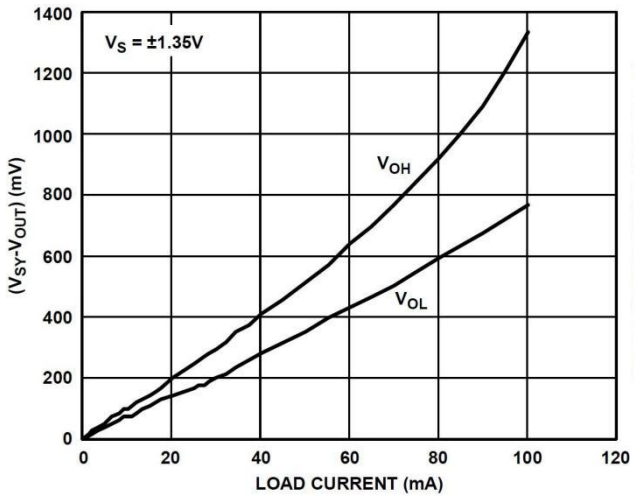
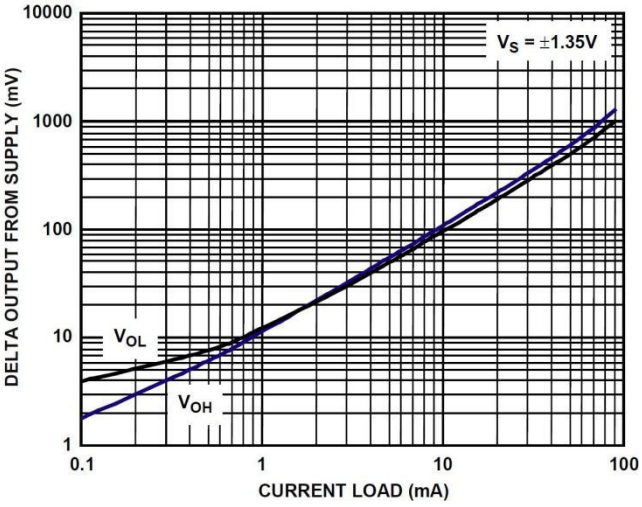


Figure 35. CD8655 Output Voltage to Supply Rail vs. Load Current Figure



36. CD8656 Output Swing vs. Current Load

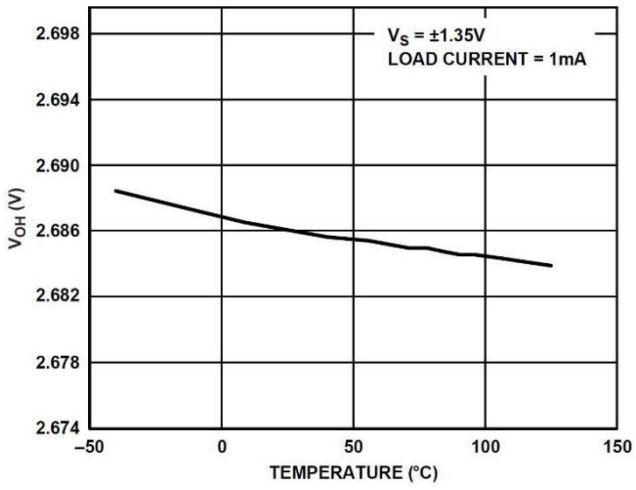


Figure 37. Output Voltage Swing High vs. Temperature

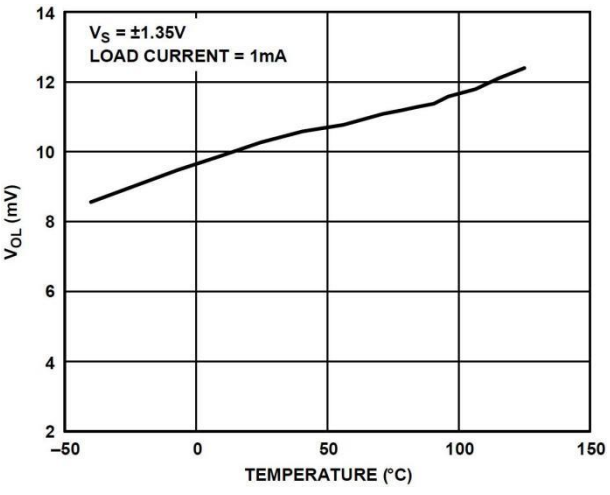


Figure 38. Output Voltage Swing Low vs. Temperature

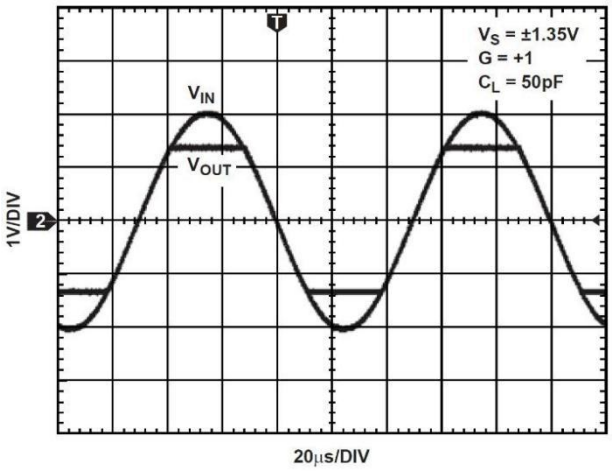


Figure 39. No Phase Reversal

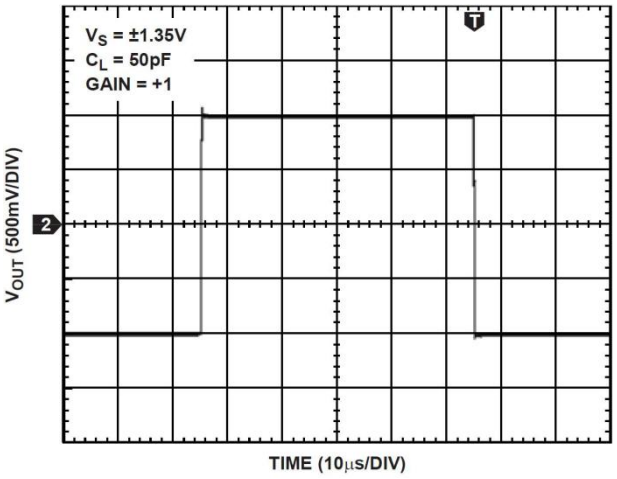


Figure 40. Large Signal Response

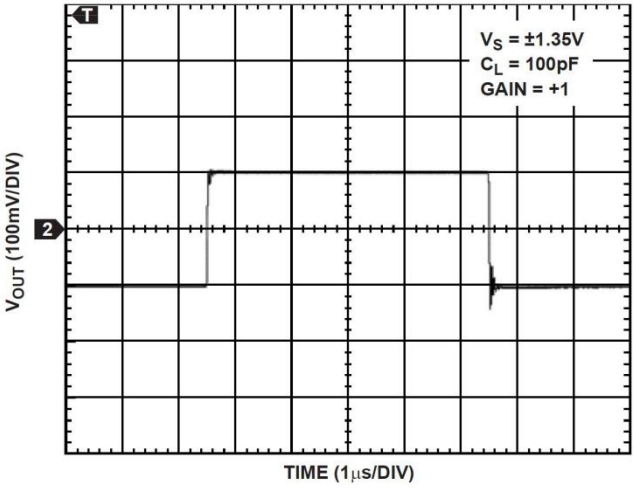


Figure 41. Small Signal Response

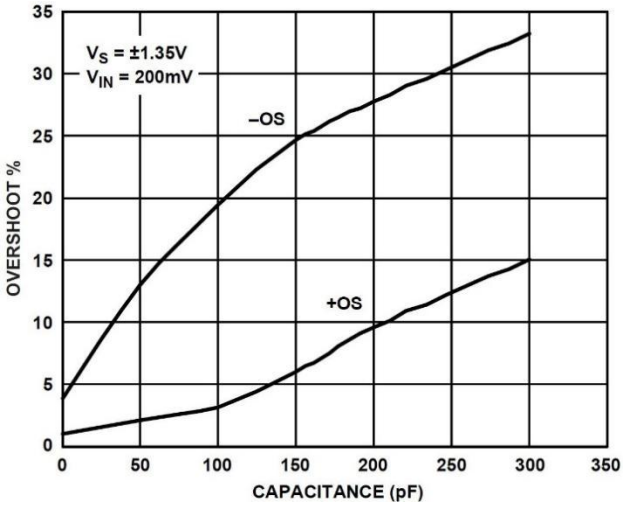


Figure 42. Small Signal Overshoot vs. Load Capacitance

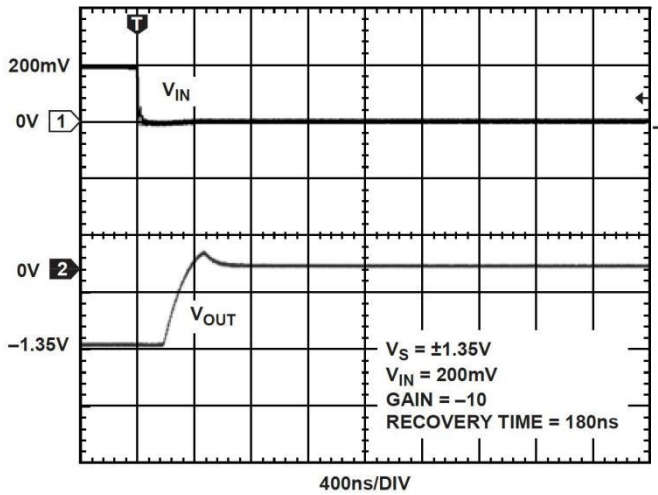


Figure 43. Negative Overload Recovery Time

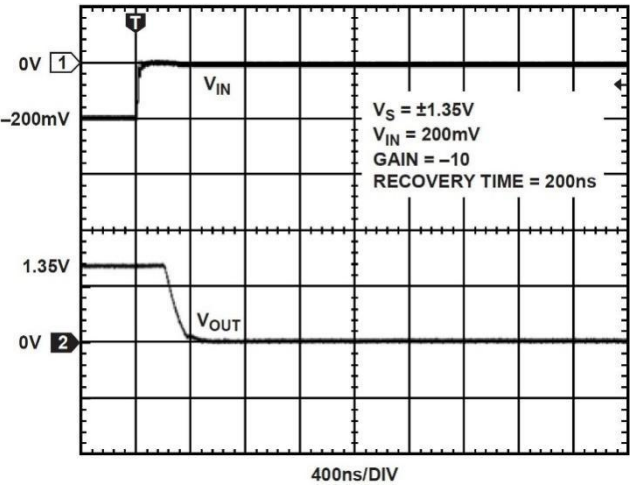


Figure 44. Positive Overload Recovery Time

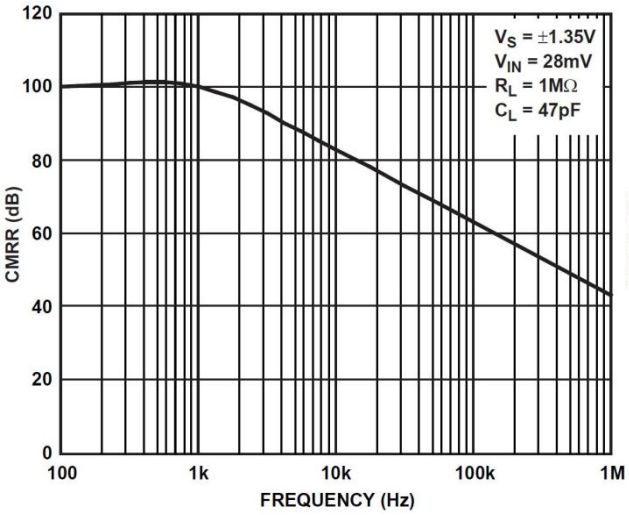


Figure 45. CMRR vs. Frequency

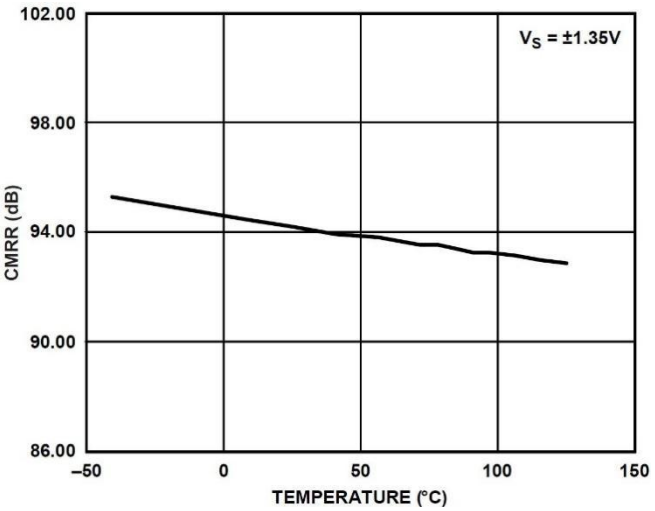


Figure 46. Large Signal CMRR vs. Temperature

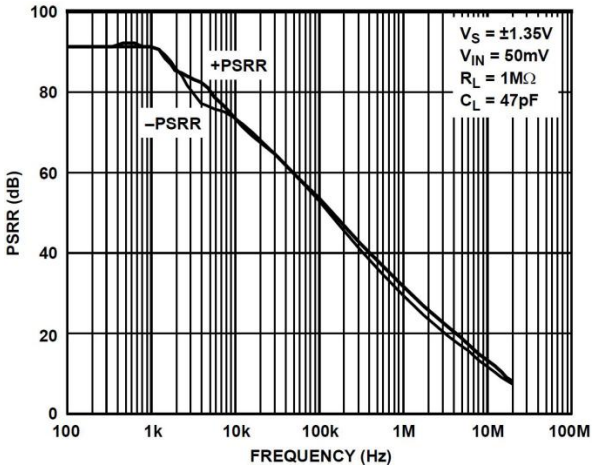


Figure 47. Small Signal PSSR vs. Frequency

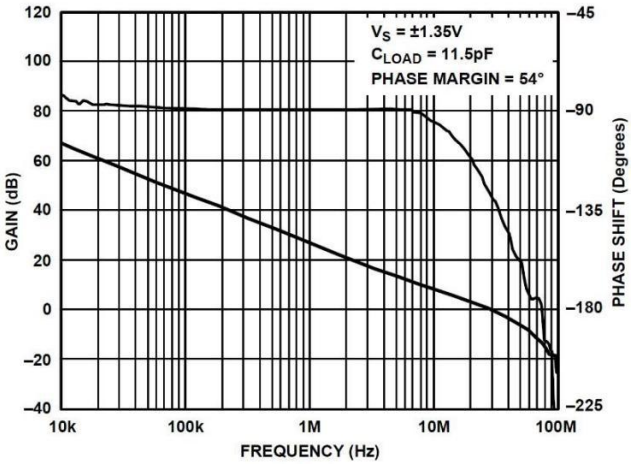


Figure 48. Open-Loop Gain and Phase vs. Frequency

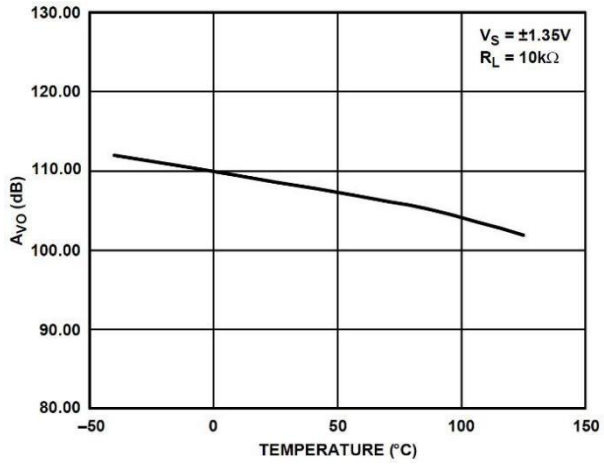


Figure 49. Large Signal Open-Loop Gain vs. Temperature

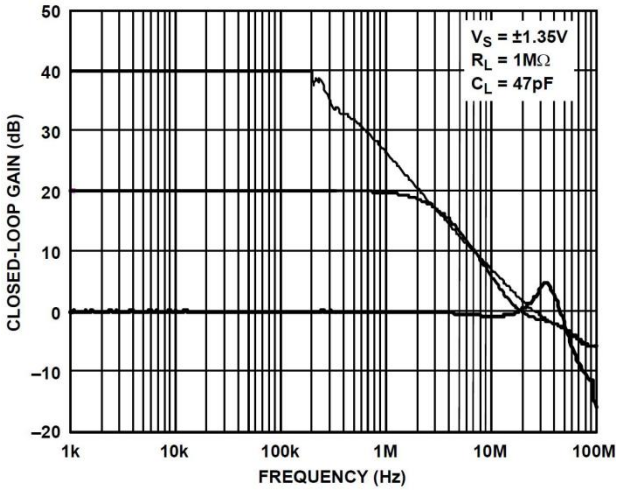


Figure 50. Closed-Loop Gain vs. Frequency

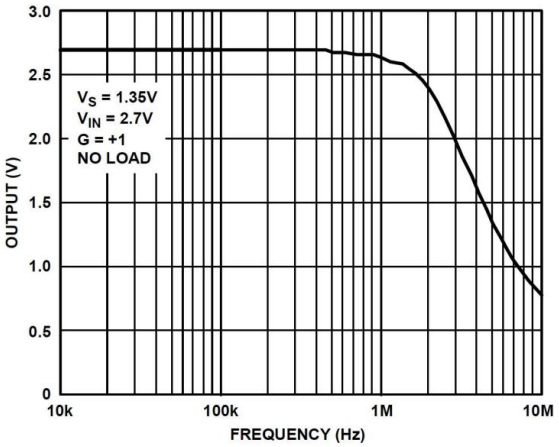


Figure 51. Maximum Output Swing vs. Frequency

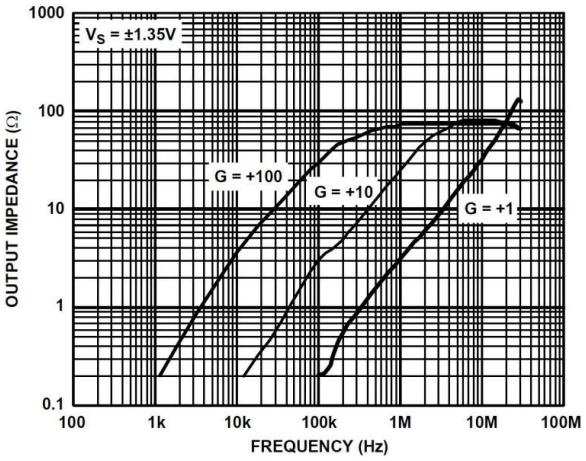


Figure 52. Output Impedance vs. Frequency

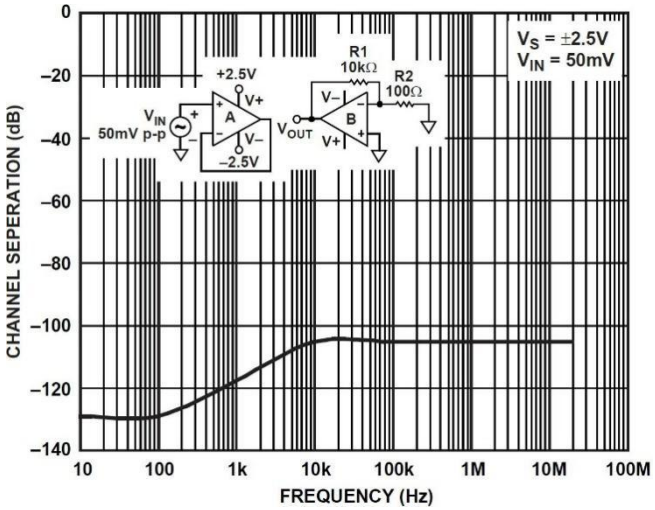


Figure 53. Channel Separation vs. Frequency

Theory Of Operation

The CD8655/CD8656 amplifiers are voltage feedback, rail-to-rail input and output precision CMOS amplifiers, which operate from 2.7V to 5.0V of power supply voltage. These amplifiers use the digital trimming technology to achieve a higher degree of precision than is available from most CMOS amplifiers. Digital trimming technology, used in a number of amplifiers, is a method of trimming the offset voltage of the amplifier after it is packaged. The advantage of post-package trimming is that it corrects any offset voltages caused by the mechanical stresses of assembly.

The CD8655/CD8656 are available in standard op amp pin outs, making digital trimming completely transparent to the user. The input stage of the amplifiers is a true rail-to-rail architecture, allowing the input common-mode voltage range of the amplifiers to extend to both positive and negative supply rails. The open-loop gain of the CD8655/CD8656 with a load of 10k Ω is typically 110dB.

The CD8655/CD8656 can be used in any precision op amp application. The amplifier does not exhibit phase reversal for common-mode voltages within the power supply. The CD8655/ CD8656 are great choices for high resolution data acquisition systems with voltage noise of 2.7nV/√Hz and THD + Noise of −103 dB for a 2V p-p signal at 10kHz. Their low noise, sub-pA input bias current, precision offset, and high speed make them superb preamps for fast filter applications. The speed and output drive capability of the CD8655/CD8656 also make them useful in video applications.

Application Information

INPUT OVERVOLTAGE PROTECTION

The internal protective circuitry of the CD8655/CD8656 allows voltages exceeding the supply to be applied at the input. It is recommended, however, not to apply voltages that exceed the supplies by more than 0.3V at either input of the amplifier. If a higher input voltage is applied, series resistors should be used to limit the current flowing into the inputs. The input current should be limited to less than 5mA.

The extremely low input bias current allows the use of larger resistors, which allows the user to apply higher voltages at the inputs. The use of these resistors adds thermal noise, which contributes to the overall output voltage noise of the amplifier. For example, a 10kΩ resistor has less than 12.6nV/√Hz of thermal noise and less than 10nV of error voltage at room temperature.

INPUT CAPACITANCE

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance

between the inputs and ground. For circuits with resistive feedback network, the total capacitance, whether it is the source capacitance, stray capacitance on the input pin, or the input capacitance of the amplifier, causes a break point in the noise gain of the circuit. As a result, a capacitor must be added in parallel with the gain resistor to obtain stability. The noise gain is a function of frequency and peaks at the higher frequencies, assuming the feedback capaci-tor is selected to make the second-order system critically damped. A few picofarads of capacitance at the input reduce the input impedance at high frequencies, which increases the amplifier’ s gain, causing peaking in the frequency response or oscillations. With the CD8655/CD8656, additional input damping is required for stability with capacitive loads greater than 200pF with direct input to output feedback. See the Driving Capacitive Loads section.

DRIVING CAPACITIVE LOADS

Although the CD8655/CD8656 can drive capacitive loads up to 500pF without oscillating, a large amount of ringing is present when operating the part with input frequencies above 100 kHz. This is especially true when the amplifiers are configured in positive unity gain (worst case). When such large capacitive loads are required, the use of external compensation is highly recommended. This reduces the overshoot and minimizes ringing, which, in turn, improves the stability of the CD8655/ CD8656 when driving large capacitive loads.

One simple technique for compensation is a snubber that consists of a simple RC network.

With this circuit in place, output swing is maintained, and the amplifier is stable at all gains. Figure 55 shows the implementation of a snubber, which reduces overshoot by more than 30% and eliminates ringing. Using a snubber does not recover the loss of bandwidth incurred from a heavy capacitive load.

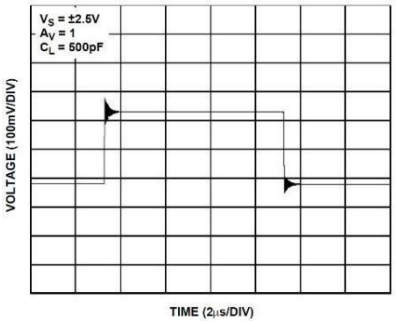


Figure 54. Driving Heavy Capacitive Loads Without Compensation

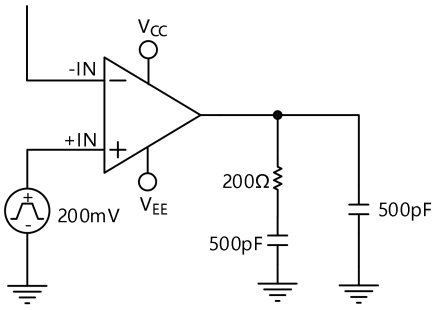


Figure 55. Snubber Network

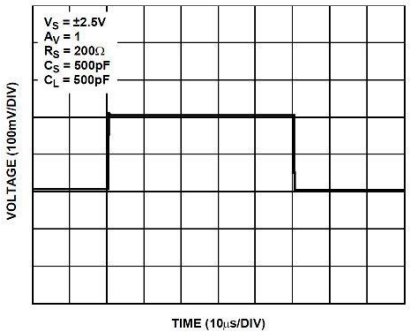


Figure 56. Driving Heavy Capacitive Loads Using a Snubber Network

THD Readings vs. Common-Mode Voltage

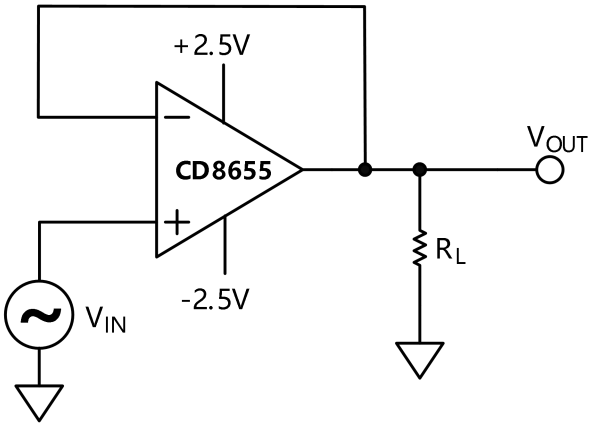


Figure 57. THD + N Test Circuit

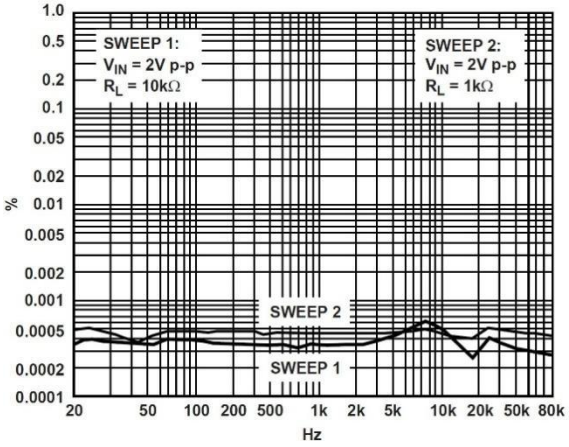


Figure 58. THD + Noise vs. Frequency

Layout Guidelines

POWER SUPPLY BYPASSING

Power supply pins can act as inputs for noise, so care must be taken to apply a noise-free, stable dc voltage. The purpose of bypass capacitors is to create low impedances from the supply to ground at all frequencies, thereby shunting or filtering most of the noise. Bypassing schemes are designed to minimize the supply impedance at all frequencies with a parallel combination of capacitors with values of 0.1 µF and 4.7 µF. Chip capacitors of 0.1 µF (X7R or NPO) are critical and should be as close as possible to the amplifier package. The 4.7 µF tantalum capacitor is less critical for high frequency bypassing, and, in most cases, only one is needed per board at the supply inputs.

GROUNDING

A ground plane layer is important for densely packed PC boards to minimize parasitic inductances. This minimizes voltage drops with changes in current. However, an under-standing of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances, and, therefore, the high frequency impedance of the path. Large changes in currents in an inductive ground return create unwanted voltage noise.

The length of the high frequency bypass capacitor leads is critical, and, therefore, surface-mount capacitors are recommended. A parasitic inductance in the bypass ground trace works against the low impedance created by the bypass capacitor. Because load currents flow from the supplies, the ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For larger value capacitors intended to be effective at lower frequencies, the current return path distance is less critical.

LEAKAGE CURRENTS

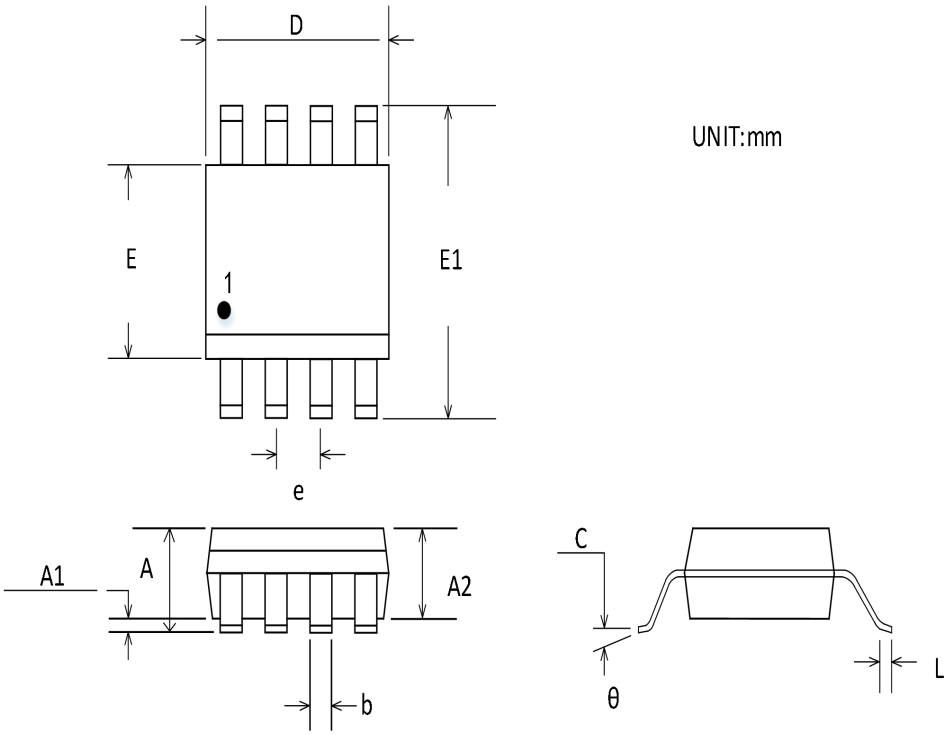
Poor PC board layout, contaminants, and the board insulator material can create leakage currents that are much larger than the input bias current of the CD8655/CD8656. Any voltage differential between the inputs and nearby traces creates leakage currents through the PC board insulator, for example, 1 V/100 GΩ = 10pA. Similarly, any contaminants on the board can create significant leakage (skin oils are a common problem).

To significantly reduce leakage, put a guard ring (shield) around the inputs and input leads that are driven to the same voltage potential as the inputs. This ensures there is no voltage potential between the inputs and the surrounding area to create any leakage currents. To be effective, the guard ring must be driven by a relatively low impedance source and should completely surround the input leads on all sides, above and below, by using a multilayer board.

The charge absorption of the insulator material itself can also cause leakage currents. Minimizing the amount of material between the input leads and the guard ring helps to reduce the absorption. Also, using low absorption materials, such as Teflon® or ceramic, may be necessary in some instances.

Package Outline Dimensions

MSOP-8

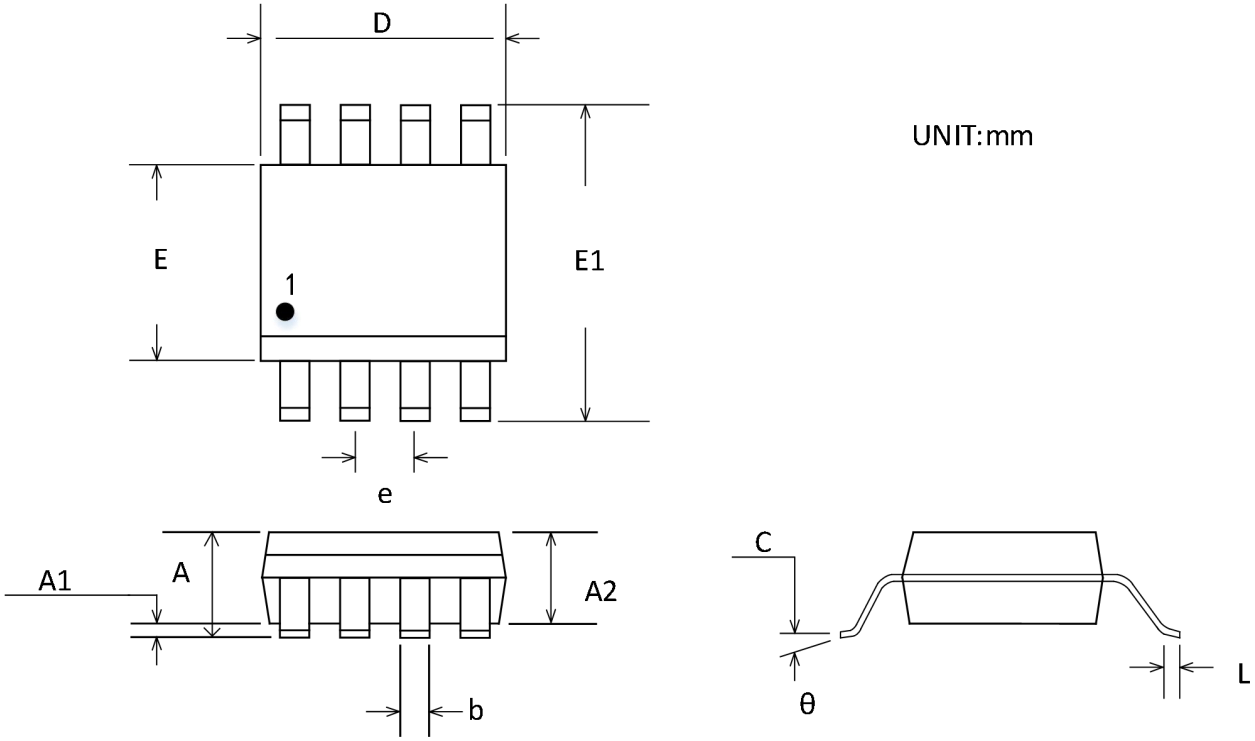


UNIT:mm

Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Chinese version:CD8655_CD8656

SOP8



UNIT:mm

Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Chinese version:CD8655_CD8656

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD8655AS8	-40℃~125℃	SOP-8	Tape and Reel, 2500
CD8655AS8-RL	-40℃~125℃	SOP-8	Tape and Reel, 3000
CD8655AS8-REEL	-40℃~125℃	SOP-8	Tape and Reel, 4000
CD8655AMS8	-40℃~125℃	MSOP-8	Tape and Reel, 3000
CD8656AS8	-40℃~125℃	SOP-8	Tape and Reel, 2500
CD8656AS8-RL	-40℃~125℃	SOP-8	Tape and Reel, 3000
CD8656AS8-REEL	-40℃~125℃	SOP-8	Tape and Reel, 4000
CD8656AMS8	-40℃~125℃	MSOP-8	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.5.26	Initial version	Regular update	WW	LYL	