CoreadDvices
承芯微电子

CD96AD56

Quad, 16-Bit, 125 MSPS, JESD204B 1.8 V Analog-to-Digital Converter

Version: Rev 1.0.0 Date: 2025-5-20

Features

- SNR：79dBFS (9.7MHz, V_{REF}=1.4V)
- SNR：77dBFS (9.7MHz, V_{REF}=1.0V)
- SFDR：85dBc to Nyqulst(V_{REF}=1.4V)
- SFDR：91dBc to Nyqulst(V_{REF}=1.0V)
- JESD204B Subclass 1 coded serial digital outputs
- Flexible analog input range: 2.0 V p-p to 2.8 V p-p
- 1.8 V supply operation
- Low power: 195 mW per channel at 125 MSPS (two lanes)
- DNL = ±0.6 LSB (V_{REF} = 1.4 V)
- INL = ±5.0 LSB (V_{REF} = 1.4 V)
- 650 MHz analog input bandwidth, full power
- Serial port control
- Full chip and individual channel power-down modes
- Built-in and custom digital test pattern generation
- Multichip sync and clock divider
- Standby mode

Application

- High speed imaging
- Quadrature radio receivers
- Diversity radio receivers
- Portable test equipment

Description

The CD96AD56 is available in a Pb-free, 72-lead, QFN specified over the −40°C to +85°C industrial temperature range.

The CD96AD56-125 is a quad, 16-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip sample and hold circuit designed for low cost, low power, small size, and ease of use. The device operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/ CMOS-/LVDS-compatible sample rate clock for full performance operation. An external reference or driver components are not required for many applications.

Individual channel power-down is supported and typically consumes less than 14 mW when all channels are disabled. The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable output clock, data alignment, and digital test pattern generation. The available digital test patterns include built-in deterministic and pseudo-random patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

Contents

Functional Block Diagram

This product adopts 56-pin package. It is specified over the −40°C to +85°C

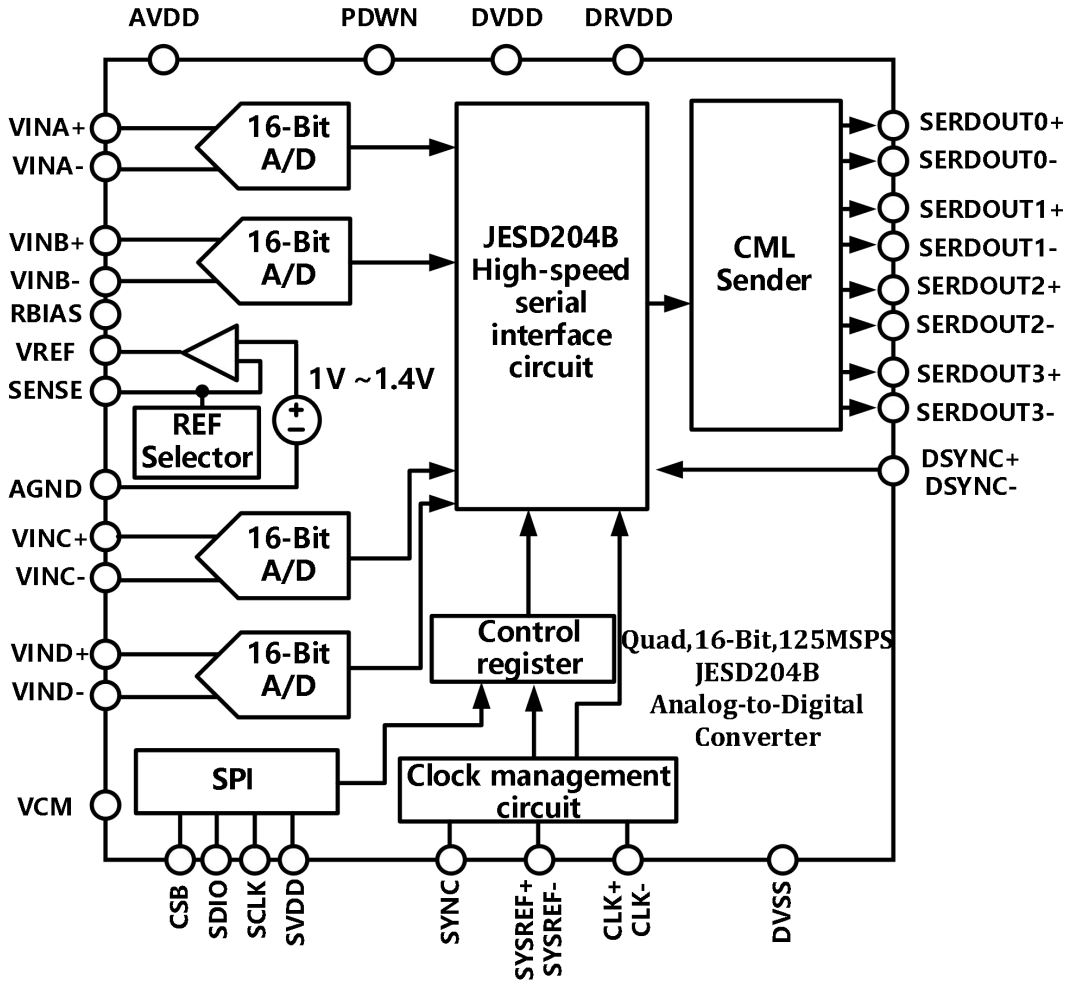

Figure1. Functional Block Diagram

Product Highlights

1. It has a small footprint. Four ADCs are contained in a small, 8 mm × 8 mm package.
2. An on-chip phase-locked loop (PLL) allows users to provide a single ADC sampling clock; the PLL multiplies the ADC sampling clock to produce the corresponding JESD204B data rate clock.

3. The configurable JESD204B output block supports up to 6.4 Gbps per lane.
4. JESD204B output block supports one, two, and four lane configurations.
5. Low power of 200 mW per channel at 125 MSPS, two lanes.
6. The SPI control offers a wide range of flexible features to meet specific system requirements.

Electrical characteristics

- **DC Specifications(V_{REF}=1.4 V)**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p full-scale differential input, 1.4 V reference, A_{IN}= −1.0 dBFS, unless otherwise noted.

Table1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	25℃	--	16	--	Bits
ACCURACY					
No Missing Codes	25℃	--	Guaranteed	--	
Offset Error	25℃	--	0.2	--	%FSR
Offset Matching	25℃	--	0.05	--	%FSR
Gain Error	25℃	--	1.2	--	%FSR
Gain Matching	25℃	--	0.95	--	%FSR
Differential Nonlinearity(DNL)	25℃	--	±0.5	--	LSB
Integral Nonlinearity(INL)	25℃	--	±5.0	--	LSB
TEMPERATURE DRIFT					
Gain Error	Full	--	5.2	--	ppm/℃
Offset Error	Full	--	-2.5	--	ppm/℃
INTERNAL VOLTAGE REFERENCE					
Output Voltage	25℃	--	1.4	--	V
Load Regulation at 1.0 mA	25℃	--	4	--	mV
Input Resistance	25℃	--	7.5	--	kΩ
INPUT REFERRED NOISE					
V_{REF}=1.4V	25℃	--	2.1	--	LSB rms

ANALOG INPUTS					
Differential Input Voltage	25℃	--	2.8	--	V_{p-p}
Common-Mode Voltage	25℃	--	0.9	--	V
Common-Mode Range	25℃	0.7	--	1.1	V
Differential Input Resistance	25℃	--	2.6	--	kΩ
Differential Input Capacitance	25℃	--	7	--	pF
POWER SUPPLY					
AVDD	25℃	--	1.8	--	V
DVDD、DRVDD	25℃	--	1.8	--	V
IAVDD (125MSPS、2 Lanes)	25℃	--	288	--	mA
IDVDD (125MSPS、2 Lanes)	25℃	--	67	--	mA
IDRVDD (125MSPS、2 Lanes)	25℃	--	83	--	mA
TOTAL POWER CONSUMPTION					
DC Input (125MSPS、2 Lanes)	25℃	--	706	--	mW
Sine Wave Input(125MSPS、2 Lanes)	25℃	--	788	--	mW
Power-Down Mode	25℃	--	14	--	mW
Standby Mode	25℃	--	547	--	mW

- **DC Specifications(V_{REF}=1.0 V)**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input, 1.0 V reference, A_{IN} = −1.0 dBFS, unless otherwise noted.

Table2.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	25℃	--	16	--	Bits
ACCURACY					
No Missing Codes	25℃	--	Guaranteed	--	
Offset Error	25℃	--	0.2	--	%FSR
Offset Matching	25℃	--	0.13	--	%FSR
Gain Error	25℃	--	1.0	--	%FSR
Gain Matching	25℃	--	0.4	--	%FSR
Differential Nonlinearity(DNL)	25℃	--	±0.5	--	LSB
Integral Nonlinearity(INL)	25℃	--	±4.0	--	LSB
TEMPERATURE DRIFT					
Gain Error	Full	--	3.1	--	ppm/℃

Offset Error	Full	--	-3	--	ppm/℃
INTERNAL VOLTAGE REFERENCE					
Output Voltage	25℃	--	1.0	--	V
Load Regulation at 1.0 mA	25℃	--	2	--	mV
Input Resistance	25℃	--	7.5	--	kΩ
INPUT REFERRED NOISE					
V_{REF}=1.4V	25℃	--	2.7	--	LSB rms
ANALOG INPUTS					
Differential Input Voltage	25℃	--	2.0	--	V_{p-p}
Common-Mode Voltage	25℃	--	0.9	--	V
Common-Mode Range	25℃	0.5		1.3	V
Differential Input Resistance	25℃	--	2.6	--	kΩ
Differential Input Capacitance	25℃	--	7	--	pF
POWER SUPPLY					
AVDD	25℃	--	1.8	--	V
DVDD、DRVDD	25℃	--	1.8	--	V
IAVDD (125MSPS、2 Lanes)	25℃	--	276	--	mA
IDVDD (125MSPS、2 Lanes)	25℃	--	69	--	mA
IDRVDD (125MSPS、2 Lanes)	25℃	--	83	--	mA
TOTAL POWER CONSUMPTION					
DC Input (125MSPS、2 Lanes)	25℃	--	688	--	mW
Sine Wave Input(125MSPS、2 Lanes)	25℃	--	771	--	mW
Power-Down Mode	25℃	--	14	--	mW
Standby Mode	25℃	--	520	--	mW

- **AC Specifications(VREF=1.4 V)**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p full-scale differential input, 1.4 V reference, A_{IN} = −1.0 dBFS, 125 MSPS, unless otherwise noted.

Table3.

Parameter	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE(SNR)					
f_{IN} = 9.7MHz	25℃	--	79.0	--	dBFS
f_{IN} = 16MHz	25℃	--	78.2	--	dBFS
f_{IN} = 64MHz	25℃	--	76.3	--	dBFS

f_{IN} = 128MHz	25℃	--	71.5	--	dBFS
f_{IN} = 201MHz	25℃	--	69.7	--	dBFS
f_{IN} = 301MHz	25℃	--	66.2	--	dBFS
SIGNAL-TO-NOISE-AND-DISTORTION(SINAD)RATIO					
f_{IN} = 9.7MHz	25℃	--	78.3	--	dBFS
f_{IN} = 16MHz	25℃	--	77.7	--	dBFS
f_{IN} = 64MHz	25℃	--	75.2	--	dBFS
f_{IN} = 128MHz	25℃	--	70.9	--	dBFS
f_{IN} = 201MHz	25℃	--	68.7	--	dBFS
f_{IN} = 301MHz	25℃	--	65.9	--	dBFS
EFFECTIVE NUMBER OF BITS(ENOB)					
f_{IN} = 9.7MHz	25℃	--	12.7	--	Bits
f_{IN} = 16MHz	25℃	--	12.6	--	Bits
f_{IN} = 64MHz	25℃	--	12.2	--	Bits
f_{IN} = 128MHz	25℃	--	11.5	--	Bits
f_{IN} = 201MHz	25℃	--	11.1	--	Bits
f_{IN} = 301MHz	25℃	--	10.7	--	Bits
SPURIOUS-FREE DYNAMIC RANGE(SFDR)					
f_{IN} = 9.7MHz	25℃	--	93.2	--	dBc
f_{IN} = 16MHz	25℃	--	90.1	--	dBc
f_{IN} = 64MHz	25℃	--	82.8	--	dBc
f_{IN} = 128MHz	25℃	--	82.3	--	dBc
f_{IN} = 201MHz	25℃	--	76.1	--	dBc
f_{IN} = 301MHz	25℃	--	82.3	--	dBc
WORST HARMONIC(SECOND OR THIRD)					
f_{IN} = 9.7MHz	25℃	--	93.2	--	dBc
f_{IN} = 16MHz	25℃	--	90.1	--	dBc
f_{IN} = 64MHz	25℃	--	82.8	--	dBc
f_{IN} = 128MHz	25℃	--	82.3	--	dBc
f_{IN} = 201MHz	25℃	--	76.1	--	dBc
f_{IN} = 301MHz	25℃	--	82.3	--	dBc
WPRST OTHER SPUR OR HARMONIC(EXCLUDING SECOND OR THIRD)					
f_{IN} = 9.7MHz	25℃	--	-96	--	dBc
f_{IN} = 16MHz	25℃	--	-92	--	dBc
f_{IN} = 64MHz	25℃	--	-90	--	dBc
f_{IN} = 128MHz	25℃	--	-89	--	dBc

f_{IN} = 201MHz	25℃	--	-93	--	dBc
f_{IN} = 301MHz	25℃	--	-90	--	dBc
TWO-TONE INTERMODULATION DISTORTION(IMD)-INPUT AMPLITUDE=-7.0dBFS					
f_{IN1}=70.5MHz,fIN1=72.5MHz	25℃	--	-84	--	dBc
CROSSTALK					
CROSSTALK[2]	25℃	--	-93	--	dB
CROSSTALK(OVERRANGE CONDITION)[3]	25℃	--	-89	--	dB
ANALOG INPUT BANDWIDTH,FULL POWER	25℃	--	650	--	MHz

1. When f_{IN}≥401MHz is tested, the test shall be conducted under the condition of A_{IN}=-5.0dBFS.

2. Crosstalk is measured at 70 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.

3. Over range condition is defined as the input being 3 dB above full scale.

- **AC Specifications(VREF=1.0 V)**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 V p-p full-scale differential input, 1.0 V reference, A_{IN}=−1.0 dBFS, 125 MSPS, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE(SNR)					
f_{IN} = 9.7MHz	25℃	--	77.4	--	dBFS
f_{IN} = 16MHz	25℃	--	77.1	--	dBFS
f_{IN} = 64MHz	25℃	--	75.3	--	dBFS
f_{IN} = 128MHz	25℃	--	71.9	--	dBFS
f_{IN} = 201MHz	25℃	--	69.2	--	dBFS
f_{IN} = 301MHz	25℃	--	65.8	--	dBFS
SIGNAL-TO-NOISE-AND-DISTORTION(SINAD)RATIO					
f_{IN} = 9.7MHz	25℃	--	77.3	--	dBFS
f_{IN} = 16MHz	25℃	--	76.9	--	dBFS
f_{IN} = 64MHz	25℃	--	75.1	--	dBFS

f_{IN} = 128MHz	25℃	--	71.6	--	dBFS
f_{IN} = 201MHz	25℃	--	68.5	--	dBFS
f_{IN} = 301MHz	25℃	--	65.6	--	dBFS
EFFECTIVE NUMBER OF BITS(ENOB)					
f_{IN} = 9.7MHz	25℃	--	12.5	--	Bits
f_{IN} = 16MHz	25℃	--	12.4	--	Bits
f_{IN} = 64MHz	25℃	--	12.2	--	Bits
f_{IN} = 128MHz	25℃	--	11.6	--	Bits
f_{IN} = 201MHz	25℃	--	11.1	--	Bits
f_{IN} = 301MHz	25℃	--	10.6	--	Bits
SPURIOUS-FREE DYNAMIC RANGE(SFDR)					
f_{IN} = 9.7MHz	25℃	--	97.6	--	dBc
f_{IN} = 16MHz	25℃	--	94.9	--	dBc
f_{IN} = 64MHz	25℃	--	92.5	--	dBc
f_{IN} = 128MHz	25℃	--	86.0	--	dBc
f_{IN} = 201MHz	25℃	--	77.5	--	dBc
f_{IN} = 301MHz	25℃	--	80.3	--	dBc
WORST HARMONIC(SECOND OR THIRD)					
f_{IN} = 9.7MHz	25℃	--	-97.6	--	dBc
f_{IN} = 16MHz	25℃	--	-94.9	--	dBc
f_{IN} = 64MHz	25℃	--	-92.5	--	dBc
f_{IN} = 128MHz	25℃	--	-86.0	--	dBc
f_{IN} = 201MHz	25℃	--	-77.5	--	dBc
f_{IN} = 301MHz	25℃	--	-80.3	--	dBc
WPRST OTHER SPUR OR HARMONIC(EXCLUDING SECOND OR THIRD)					
f_{IN} = 9.7MHz	25℃	--	-95	--	dBc
f_{IN} = 16MHz	25℃	--	-95	--	dBc
f_{IN} = 64MHz	25℃	--	-94	--	dBc
f_{IN} = 128MHz	25℃	--	-89	--	dBc
f_{IN} = 201MHz	25℃	--	-91	--	dBc
f_{IN} = 301MHz	25℃	--	-89	--	dBc
TWO-TONE INTERMODULATION DISTORTION(IMD)-INPUT AMPLITUDE=-7.0dBFS					
f_{IN1}=70.5MHz,fIN1=72.5MHz	25℃	--	-89	--	dBc
CROSSTALK					
CROSSTALK[2]	25℃	--	-94	--	dB
CROSSTALK(OVERRANGE CONDITION)[3]	25℃	--	-89	--	dB

ANALOG INPUT BANDWIDTH,FULL POWER	25℃	--	650	--	MHz

1. When f_{IN}≥401MHz is tested, the test shall be conducted under the condition of A_{IN}=-5.0dBFS.

2. Crosstalk is measured at 70 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.

3. Over range condition is defined as the input being 3 dB above full scale.

- **Digital Specifications**

AVDD = 1.8 V, DRVDD = 1.8 V, SVDD = 1.8 V, 2.8 V p-p differential input, 1.4 V reference, A_{IN}=−1.0 dBFS, unless otherwise noted.

Table 5.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUT(CLK+、CLK-)					
Logic Compliance	--	--	CMOS/LVDS/LVPECL	--	--
Differential Input Voltage Range	Full	0.2	--	3.6	Vp-p
Input Voltage Range	Full	AGND−0.2	--	AVDD+0.2	V
Input Common-Mode Voltage	Full	--	0.9	--	V
Input Resistance(Differential)	25℃	--	15	--	kΩ
Input Capacitance	25℃	--	4	--	pF
DSYNC INPUT(DSYNC+/ DSYNC-)					
Logic Compliance	Full	--	LVDS	--	--
Internal Common-Mode Bias	Full	--	0.9	--	V
Differential Input Voltage Range	Full	0.3	--	3.6	Vp-p
Input Voltage Range	Full	DGND	--	DVDD	V
Input Common-Mode Voltage Range	Full	0.9	--	1.4	V
High Level Input Current	Full	−5	--	+5	μA
Low Level Input Current	Full	−5	--	+5	μA

Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
DSYSREF INPUT(DSYSREF+/ DSYSREF-)					
Logic Compliance		--	LVDS	--	
Internal Common-Mode Bias	Full	--	0.9	--	V
Differential Input Voltage Range	Full	0.3	--	3.6	Vp-p
Input Voltage Range	Full	DGND	--	DVDD	V
Input Common-Mode Voltage Range	Full	0.9	--	1.4	V
High Level Input Current	Full	−5	--	+5	μA
Low Level Input Current	Full	−5	--	+5	μA
Input Capacitance	Full	--	4	--	pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT(PDWN、SYNC、SCLK)					
Logic 1 Voltage Range	Full	1.2	--	AVDD+0.2	V
Logic 0 Voltage Range	Full	0	--	0.8	V
Input Resistance	25℃	--	30	--	kΩ
Input Capacitance	25℃	--	2	--	pF
LOGIC INPUT(CSB)					
Logic 1 Voltage Range	25℃	1.2	--	AVDD+0.2	V
Logic 0 Voltage Range	25℃	0	--	0.8	V
Input Resistance	25℃	--	26	--	kΩ
Input Capacitance	25℃	--	2	--	pF
LOGIC INPUT(SDIO)					
Logic 1 Voltage Range	25℃	1.2	--	AVDD+0.2	V
Logic 0 Voltage Range	25℃	0	--	0.8	V
Input Resistance	25℃	--	26	--	kΩ
Input Capacitance	25℃	--	5	--	pF
DIGITAL OUTPUTS (SERDOUTx+、SERDOUTx-)					
Logic Compliance	Full	--	CML400	--	--
Differential Output Voltage(VOD)	Full	400	600	750	mV
Output Offset Voltage(VOS)	Full	0.75	DRVDD/2	1.05	V

- **Switching Specifications**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 V p-p differential input, 1.4 V reference, A_{IN}=−1.0 dBFS, unless otherwise noted.

Table6.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK					
Input Clock Rate	Full	40	--	1000	MHz
Conversion Rate	--	40	--	125	MSPS
Clock Pulse Width High(tEH)	--	--	4	--	ns
Clock Pulse Width Low(tEL)	--	--	4	1.4	ns
SYNC Setup Time to Clock	--	--	--	-0.4	ns
SYNC Hold Time to Clock	--	--	370	600	ns
DSYSREF Setup Time to Clock(t_{REFS})4	--	--	-92	0	ps
DSYSREF Hold Time to Clock(t_{REFH})4	--	--	--	--	ps
DATA OUTPUT PARAMETERS					
Data Output Period or Unit Interval(UI)	Full	--	L/(20 × M × fS)	--	秒
Data Output Duty Cycle	25°C	--	50	--	%
Data Valid Time	25°C	--	0.81	--	UI
PLL Lock Time(t_{LOCK})	25°C	--	25	--	µs
Wake-Up Time		--		--	
Standby	25°C	--	250	--	ns
ADC(Power-Down)	25°C	--	375	--	µs
Output(Power-Down)	25°C	--	50	--	µs
DSYNC Falling Edge to First K.28 Characters	Full	4	--	--	Multiframes
CGS Phase K.28 Characters Duration	Full	1	--	--	Multiframes
Pipelie Delay	--	--	--	--	
JESD204B M4、L1 Mode(Latency)	Full	--	23	--	Cycle 7
JESD204B M4、L2 Mode(Latency)	Full	--	29	--	Cycle 7
JESD204B M4、L4 Mode(Latency)	Full	--	44	--	Cycle 7
Data Rate per Lane	Full	--	--	6.4	Gbps
Deterministic Jitter(D_J)		--	--	--	
At 6.4 Gbps	Full	--	8	--	Ps

Random Jitter(R_J)		--		--	
At 6.4 Gbps	Full	--	1.25	--	ps rms
Output Rise Time/Fall Time	Full	--	50	--	ps
Differential Termination Resistance	25°C	--	100	--	Ω
APERTURE					
Aperture Delay(t_A)	25°C	--	1	--	--
Aperture Uncertainty(Jitter，t_J)	25°C	--	135	--	--
Out of Range Recovery Time	25°C	--	1	--	--

● Timing Specifications

Table 7.

Parameter	Description	Limit	Unit
SPI TIMING REQUIREMENTS See Figure 70			
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns(min)
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns(min)
t_{CLK}	Period of the SCLK	40	ns(min)
t_S	Setup time between CSB and SCLK	2	ns(min)
t_H	Hold time between CSB and SCLK	2	ns(min)
t_{HIGH}	SCLK pulse width high	10	ns(min)
t_{LOW}	SCLK pulse width low	10	ns(min)
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	ns(min)
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	ns(min)

Timing Diagrams

Refer to the Memory Map Register Table section for SPI register settings.

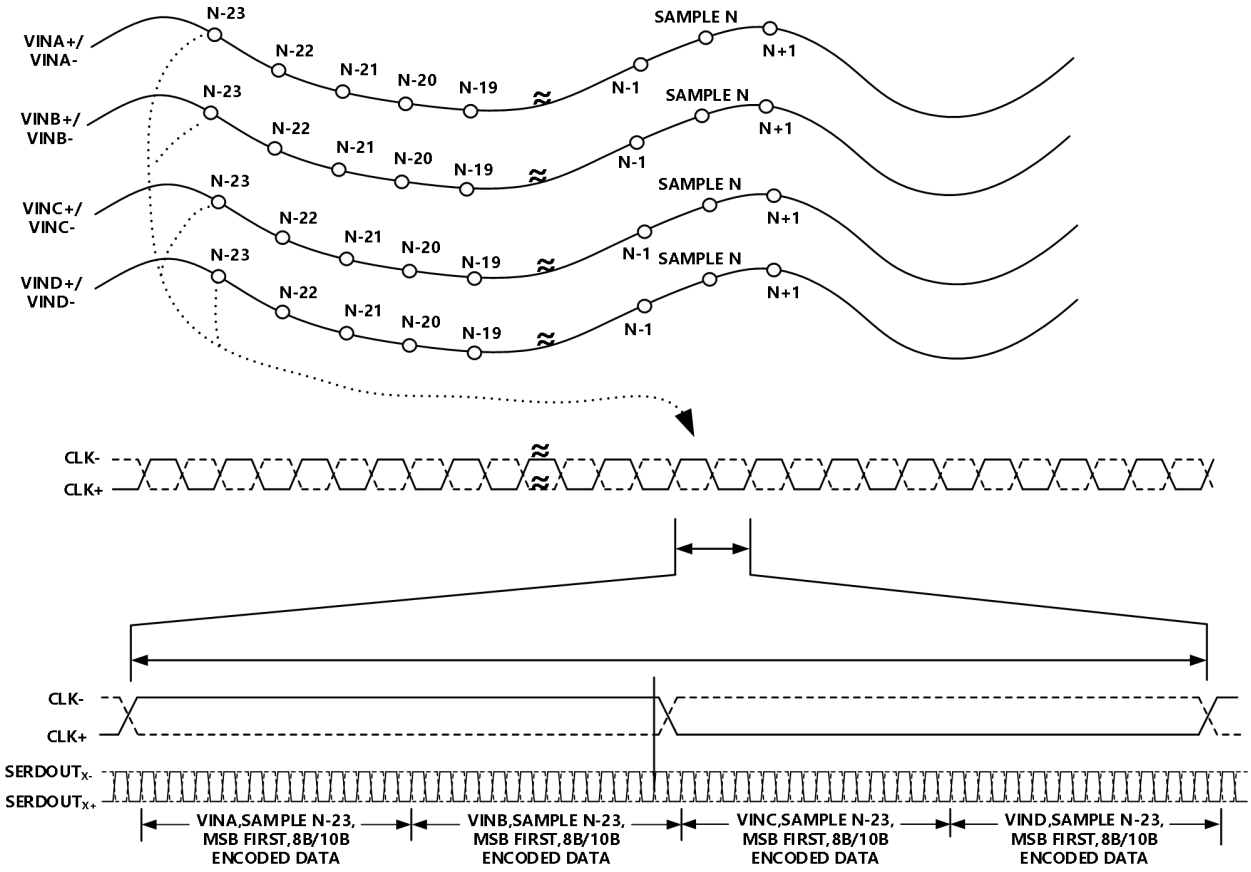

Figure 2. Data Output Timing, M=4, L=1

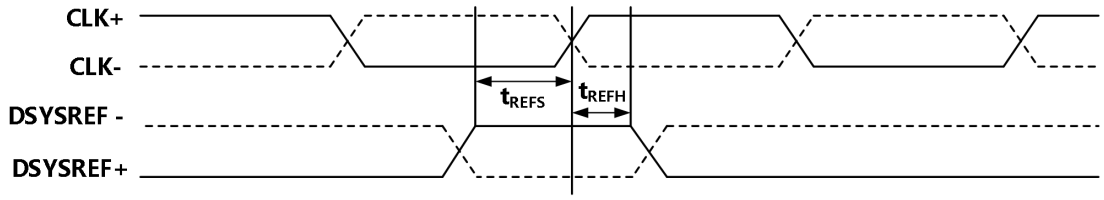

Figure 3. SYSREF±Setup and Hold Timing (Clock Divider = 1)

Absolute Maximum Ratings

Parameter	Range
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
DVDD to DVSS	−0.3 V to +2.0 V
SVDD to AGND	−0.3 V to +2.0 V
Digital Outputs to AGND	−0.3 V to +2.0 V
CLK+、CLK− to AGND	−0.3 V to +2.0 V
VINx+、VINx− to AGND	−0.3 V to +2.0 V
DSYSREF+、DSYSREF− to AGND DSYNC−、DSYNC+ to AGND	−0.3 V to +2.0 V
SCLK、SDIO、CSB、PDWN to AGND SYNC to AGND	−0.3 V to +3.9 V
RBIAS to AGND	−0.3 V to +2.0 V
VCM、VREF、SENSE to AGND	
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE: θ_{JA} is for a 4-layer printed circuit board (PCB) with solid ground plane (simulated). The exposed pad is soldered to the PCB ground.

Package Type	Air Flow Velocity(m/s)	θ_{JA} (° C/W)	θ_{JB} (° C/W)1	θ_{JC} Top (° C/W)1	θ_{JC} Bottom(° C/W)1
56-Lead LFCSP、8mm×8 mm	0	22.4	7.7	7.42	2.29
	1	19.0	N/A	N/A	N/A
	2.5	17.6	N/A	N/A	N/A

Pin Configuration

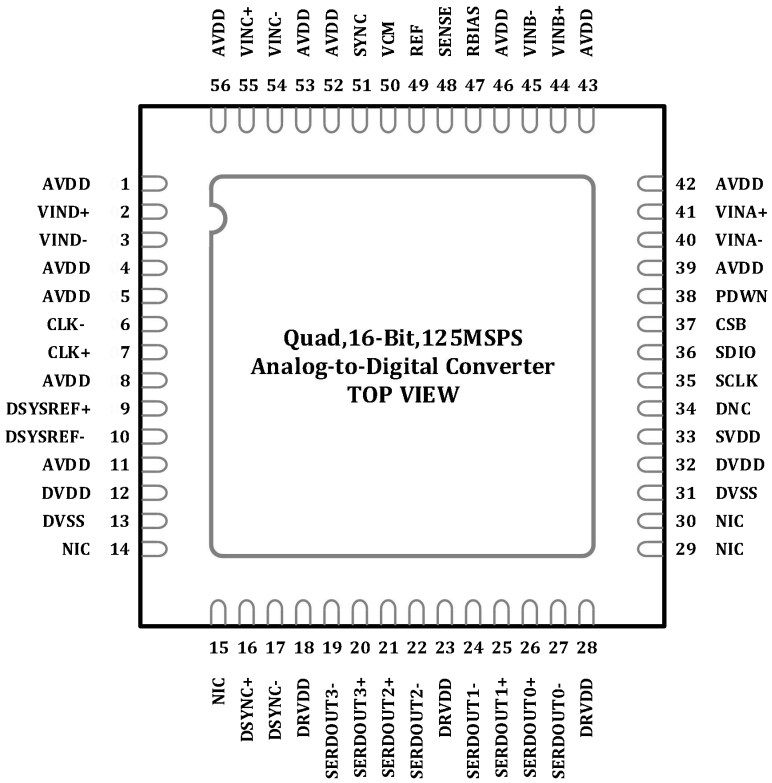

Figure 4. Pin Configuration, Top View

The INL and DNL test curves are shown in Figure 3.The FFT with input analog input frequency of 100MHz and sampling rate of 250MSPS is shown in Figure 4. The FFT with input analog input frequency of 170MHz and sampling rate of 250MSPS is shown in Figure 5. The FFT with input analog input frequency of 230MHz and sampling rate of 250MSPS is shown in Figure 6. The FFT with input analog input frequency of 300MHz and sampling rate of 250MSPS is shown in Figure 7. The bandwidth test is shown in Figure 8.

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND,Exposed Pad	--
1,4,5,8,11,39,42,43,46,52,53,56	AVDD	1.8 V Analog Supply Pins.

2	VIND+	ADC D Analog Input True.
3	VIND-	ADC D Analog Input Complement.
6,7	CLK-,CLK+	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
9	DSYSREF+	Active High JESD204B LVDS SYSREF Input True.
10	DSYSREF-	Active High JESD204B LVDS SYSREF Input Complement.
12,32	DVDD	Digital Supply.
13,31	DVSS	Digital Ground.
14,15,29,30	NIC	Not Internally Connected. Can be connected to ground if desired.
16	DSYNC+	Active Low JESD204B LVDS SYNC Input True.
17	DSYNC-	Active Low JESD204B LVDS SYNC Input Complement.
18,23,28	DRVDD	Digital Output Driver Supply.
19	SEROUT3-	Lane 3 Digital Output Complement.
20	SEROUT3+	Lane 3 Digital Output True.
21	SEROUT2+	Lane 2 Digital Output True.
22	SEROUT2-	Lane 2 Digital Output Complement.
24	SEROUT1-	Lane 1 Digital Output Complement.
25	SEROUT1+	Lane 1 Digital Output True.
26	SEROUT0+	Lane 0 Digital Output True.
27	SEROUT0-	Lane 0 Digital Output Complement.
33	SVDD	SPI Supply Pin.
34	DNC	Do Not Connect. Do not connect to this pin.
35	SCLK	SPI Clock Input.
36	SDIO	SPI Data Input and Output, Bidirectional.
37	CSB	SPI Chip Select Bar.Active low enable;30kΩ internal pull-up resistor.
38	PDWN	Digital Input.This pin has a 30kΩ internal pill-down resistor.PDWN high=power-down device and PDWN low=run device(normal operation)
40	VINA-	ADC A Analog Input Complement.
41	VINA+	ADC A Analog Input True.
44	VINB+	ADC B Analog Input True.
45	VINB-	ADC B Analog Input Complement.

47	RBIAS	Sets Analog Current Bias.This pin connects a 10kΩ(1% tolerance)resistor to ground.
48	SENSE	Reference Mode Selection.
49	VREF	Voltage Reference Input and Output.
50	VCM	Analog Input Common-Mode Voltage.
51	SYNC	Digital Input. Synchronous input to clock divider.
54	VINC-	ADC C Analog Input Complement.
55	VINC+	ADC C Analog Input True.

Typical Performance Characteristics

- **V_{REF} = 1.4 V**

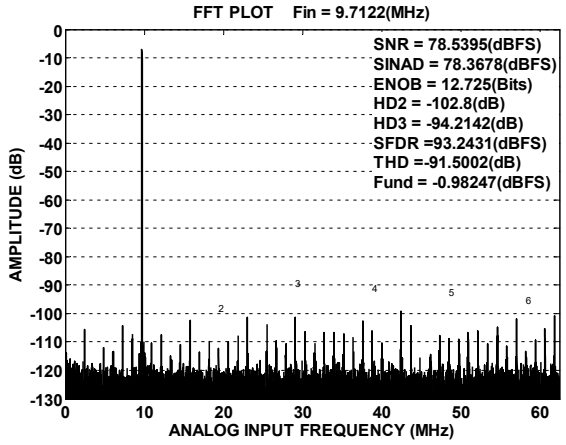

Figure 5. Single-Tone 32k FFT with f_{IN} = 9.7 MHz,f_S = 125 MSPS

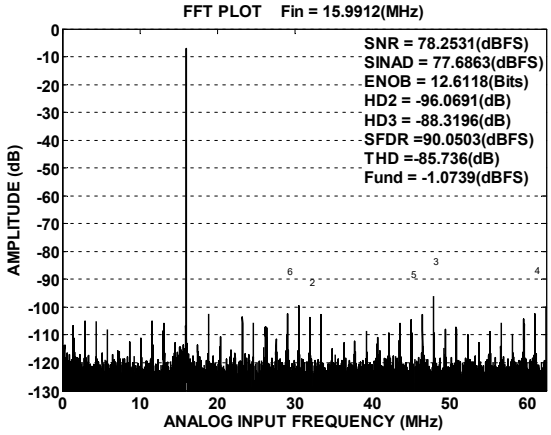

Figure 6. Single-Tone 32k FFT with fIN = 16.3 MHz, f_S = 125 MSPS

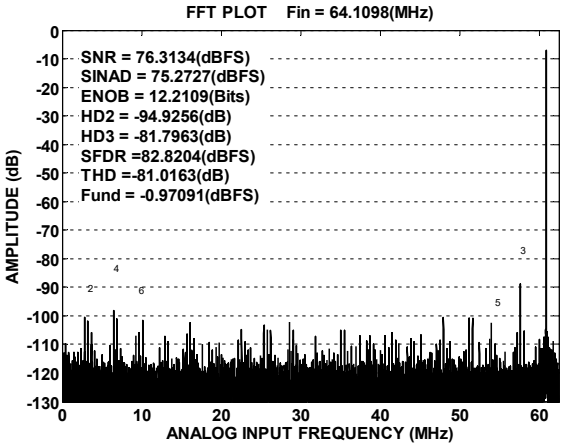

Figure7.Single-Tone 32K(f_{IN}=64MHz, f_S=125MSPS)

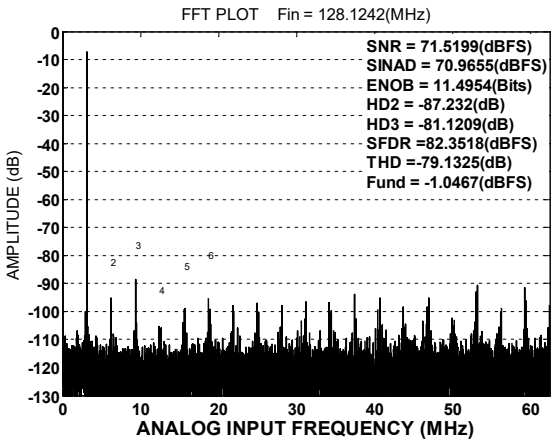

Figure8.Single-Tone 32K(f_{IN}=128MHz, f_S=125MSPS)

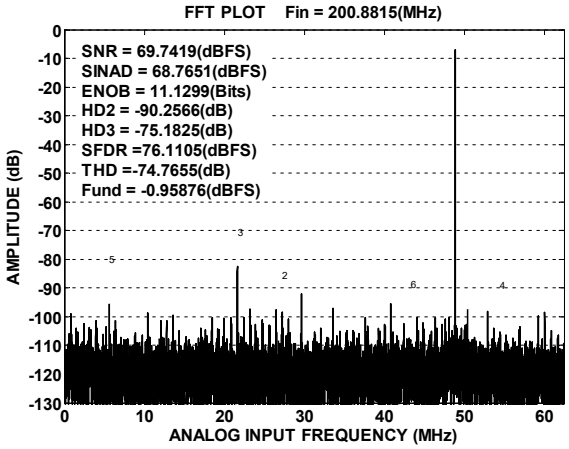

Figure9.Single-Tone 32K(f_{IN}=201MHz，f_S=125MSPS)

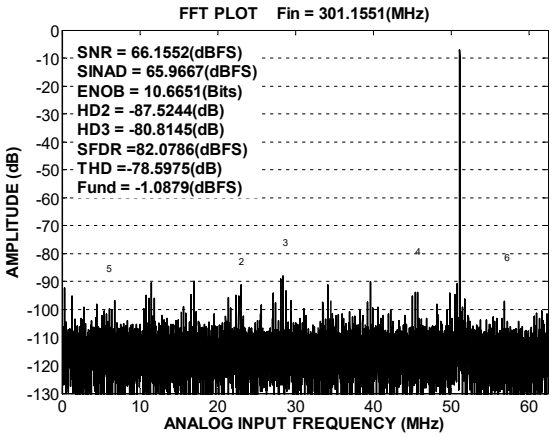

Figure10.Single-Tone32K(f_{IN}=301MHz，f_S=125MSPS)

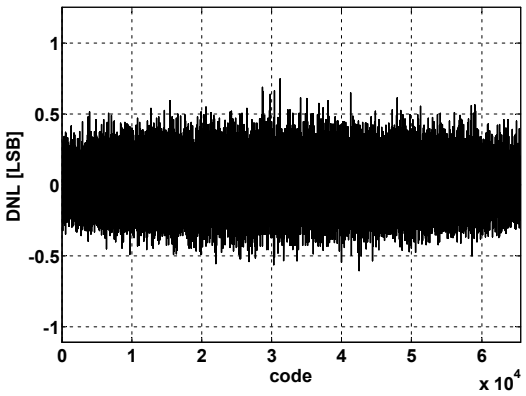

Figure11.Differential Nonlinearity (DNL)(f_{IN}=9.7MHz，f_S=125MSPS)

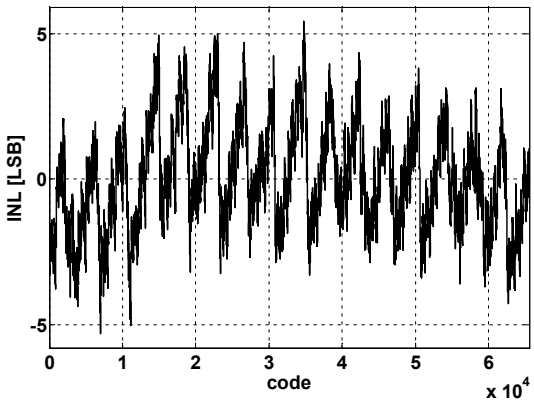

Figure12.Integral Nonlinearity (INL)(f_{IN}=9.7MHz，f_S=125MSPS)

- **V_{REF} = 1.0 V**

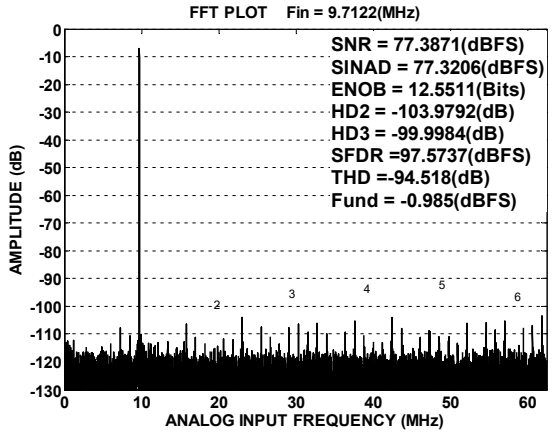

Figure13.Single-Tone 32K(f_{IN}=9.7MHz，f_S=125MSPS)

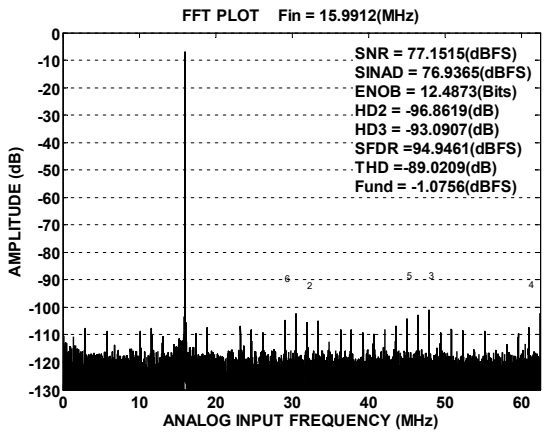

Figure14.Single-Tone 32K(f_{IN}=16MHz，f_S=125MSPS)

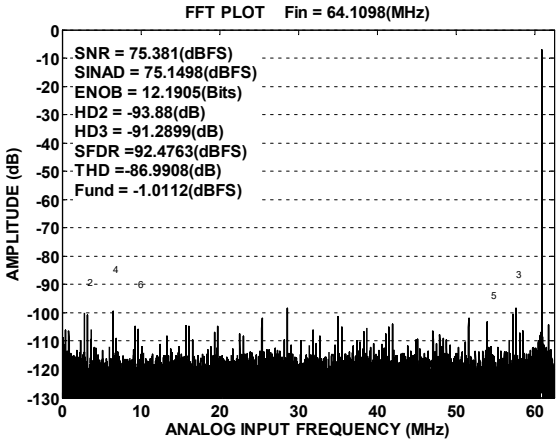

Figure15.Single-Tone 32K(f_{IN}=64MHz，f_S=125MSPS)

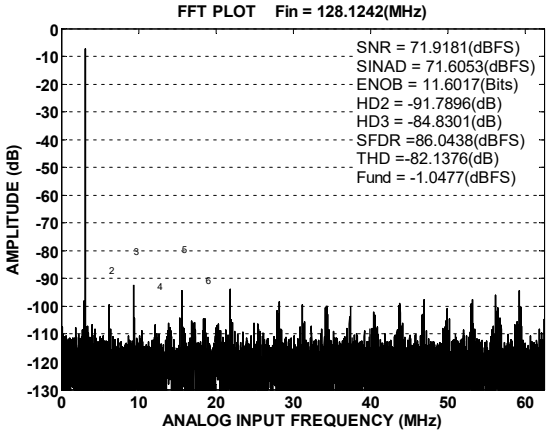

Figure16.Single-Tone 32K(f_{IN}=128MHz，f_S=125MSPS)

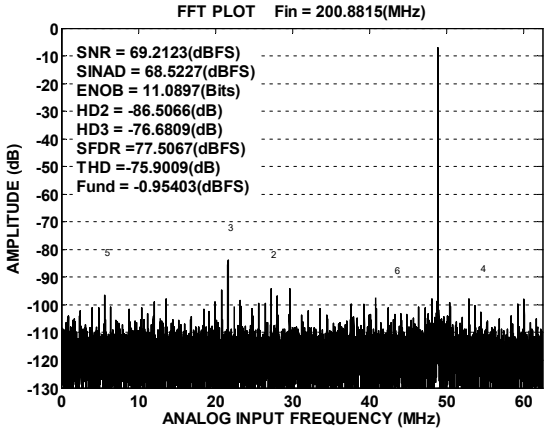

Figure17.Single-Tone 32K(f_{IN}=201MHz，f_S=125MSPS)

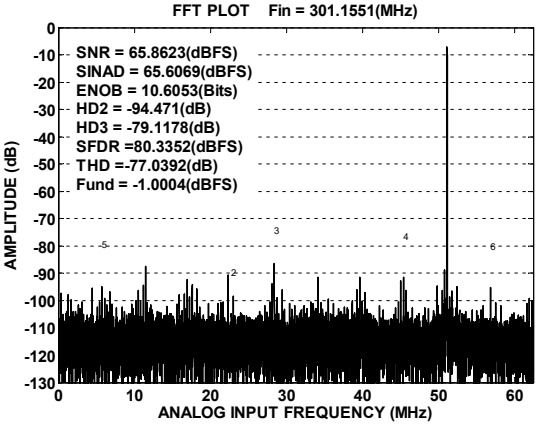

Figure18.Single-Tone 32K(f_{IN}=301MHz，f_S=125MSPS)

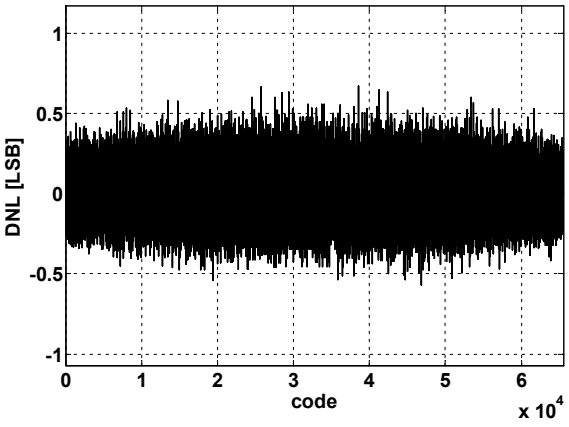

Figure19.Differential Nonlinearity (DNL)(f_{IN}=10MHz，f_S=125MSPS)

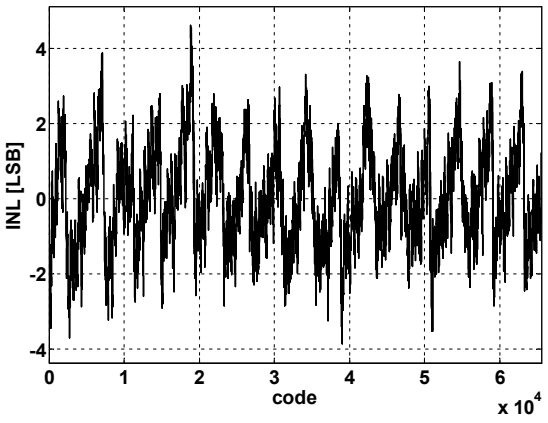

Figure20.Integral Nonlinearity (INL)(f_{IN}=10MHz，f_S=125MSPS)

Equivalent Circuits

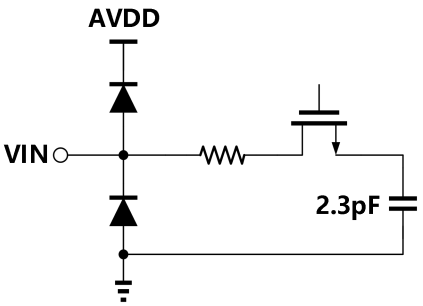

Figure 21. Equivalent Analog Input Circuit

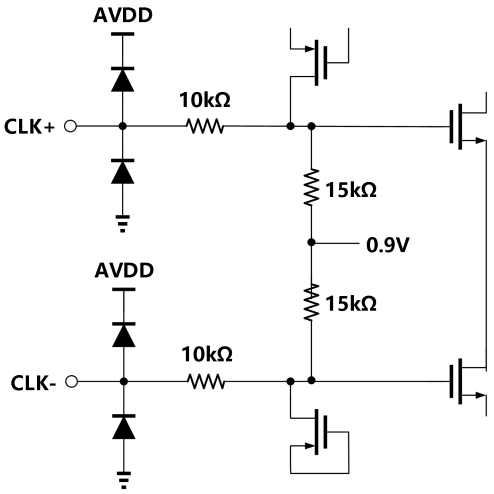

Figure 22. Equivalent CLOCK Input Circuit

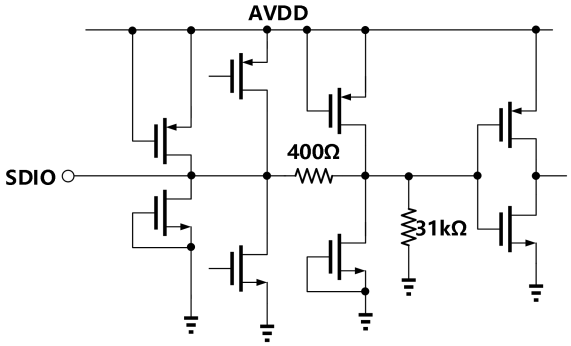

Figure 23. Equivalent SDIO Input Circuit

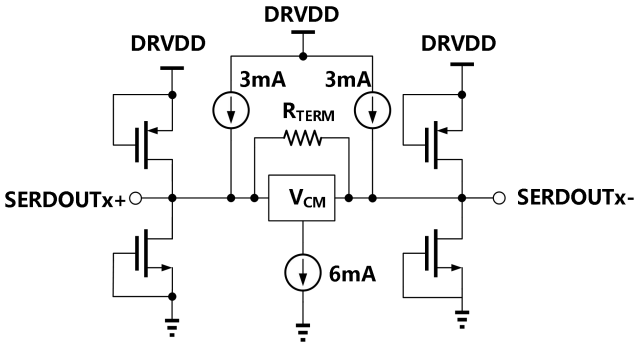

Figure 24. Equivalent SERDOUT± Circuit

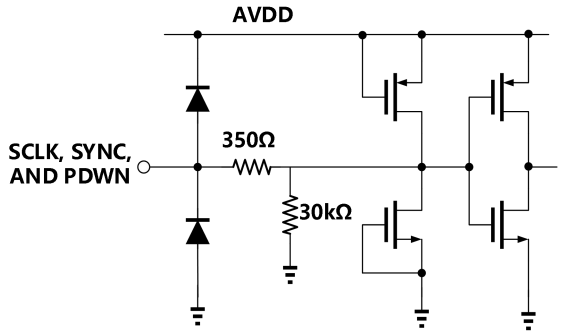

Figure25.Equivalent SCLK，SYNC，PDWN Circuit

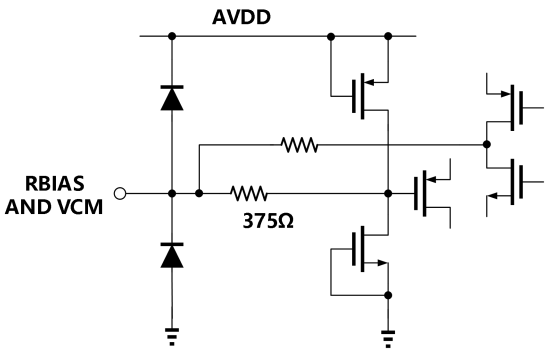

Figure26.Equivalent RBIAS,VCM Circuit

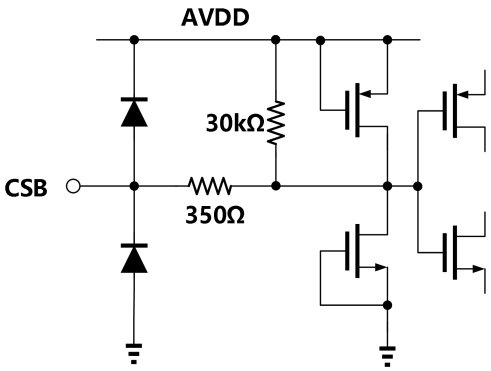

Figure27.Equivalent CSB Input Circuit

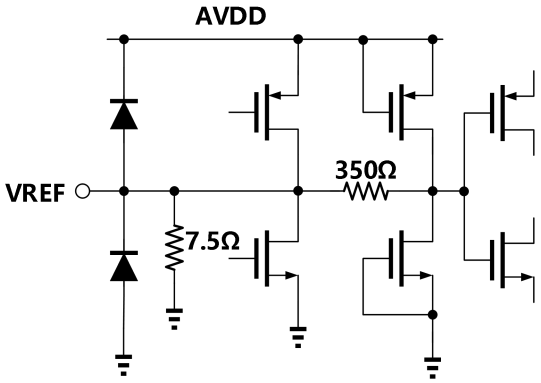

Figure28.Equivalent VREF Input Circuit

Memory MAP Register Table

Table 16. Memory Map Registers (SPI Registers/Bits Not Labeled Local Are Global)

Addr (Hex)	Register Names	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Notes/ Comments
Chip Configuration Registers											
0x00	SPI port configuration	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	
0x01	Chip ID	8-bit chip ID[7:0]; CD96AD56-125=0xC0(Quad、16位、125MSPS、JESD204B)								0xC0	Read Only
0x02	Device index	Open	Speed grade ID[6:4]; 110=125MSPS			Open	Open	Open	Open	0x60	Read Only
Channel Index and Transfer Registers											
0x05	Device index	Open	Open	Open	Open	Data Channel 3	Data Channel 2	Data Channel 1	Data Channel 0	0x0F	
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Initiate Register 0X100override(self clearing)	0x00	
ADC Functions											
0x08	Power modes	Open	Open	PDWN pin function:	JTX standby mode:0	Reserved		Power mode: 00=normal operation, 01=full		0x00	

				0=full power-down,1=standby	=ignore standby,1=do not ignore standby			power-down, 10=standby 11=digital reset			
0x09	Clock	Open	0	Open	Open	Open	Open	Open	Duty cycle stabilizer: 0=off, 1=on	0x00	
0x0A	PLL_STATUS	PLL locked Status bit: 0=PLL is not locked, 1=PLL is locked	Open	Open	Open	Open	Open	Open	JTX link status: 0=not ready, 1=ready		Read Only
0x0B	Clock divider	Open	Open	Open	Open	Open	Clock divider ratio[2:0]: 000=divide by 1, 001=divide by 2, 010=divide by 3, 011=divide by 4, 100=divide by 5, 101=divide by 6, 110=divide by 7, 111=divide by 8,			0x00	
0x0C	Enhancement control	Open	Open	Open	Open	Open	Chop mode: 0=off 1=on	Open	Open	0x00	
0x0D	Test mode(local except for pseudo-random number(PN)sequence resets)	User input test mode: 00=single 01=alternate 10=single once 11=alternate once, (affects user input test mode		Reset PN long generator	Reset PN short generator	Output test mode[3:0](local): 0000=off(default), 0001=midscale short, 0010=positive full scale(FS), 0011=negative FS, 0100=alternating checkerboard, 0101=PN23 sequence, 0110=PN9 sequence, 0111=one/zero word toggle,				When set,the test data is placed on the output pins in place of normal	

		only,Bits[3:0]=1000)			1000=user input, 1001=1/0 bit toggle, 1010=1X sync 1011=one bit high 1100=mixed bit frequency				data.		
0x10	Offset adjust(local)	8-bit device offset adjustment[7:0](local); offset adjusts in LSB from +127 to −128(twos complement format)							0x00		Device offset trim
0x14	Output mode	JTX CS mode: 000={overrange||underrange,valid flag} 001={overrange||underrange} 010={overrange||underrange,blank} 011={blank.valid flag} 100={blank,blank} Others={overrange||underrange,valid flag}			ADC output disable: 0=enabled, 1=disabled(local)	Open	Open	Output format: 00=offset binary, 01=twos complement	0x01		Bits[7:5] are not applicable when using the default 16-bit resolution
0x15	Output adjust	Open	Open	Open	Open	Open	Typical CML differential output drive level: 000=473mVp-p, 001=524mVp-p, 010=574mVp-p, 011=621mVp-p(default), 100=667mVp-p, 101=716mVp-p, 110=763mVp-p, 111=811mVp-p			0x03	
0x16	Clock phase control	Open	Input clock phase adjust[2:0] (value is number of input clock cycles of phase delay)			Open	Open	Open	Open	0x00	
0x18	Input span select	Internal VREF adjustment[1:0]: 00=1.0V, 01=1.2V, 10=1.3V, 11=1.4V		Open	Open	Open	Differential span adjustment: 000=50% of normal, 001=57% of normal, 010=67% of normal, 011=80% of normal, 100=normal			0x04	
0x19	User Test Pattern 1 LSB	User Test Pattern 1[7:0]								0x00	
0x1A	User Test Pattern 1	User Test Pattern 115:8]								0x00	

	MSB										
0x1B	User Test Pattern 2 LSB	User Test Pattern 2[7:0]								0x00	
0x1C	User Test Pattern 2 MSB	User Test Pattern 2[15:8]								0x00	
0x21	FLEX_SERIAL_CONTROL	Open	Open	Open	Open	PLL low rate mode: 0=lane rate≥2 Gbps 1=lane rate<2 Gbps	Open	Open	Open	0x00	
0x22	FLEX_SERIAL_CH_STAT	Open	Open	Open	Open	Open	Open	Open	Channel power-down (local)	0x00	
0x3A	SYSREF_CTRL	Open	Open	Open	0=normal mode, 1=realigngthe lanes on every active DSYNC±	0=realign the lanes only when DSYSREF± causes a resync of the counters,1=realign the lanes on every DSYSREF±	Open	Open	Open	0x00	
0x3B	REALIGN_PATTERN_CTRL	This pattern is written into the FIFO when a lane is being aligned: 00 = lane outputs constant zero, 55 = lane outputs toggling pattern								0x55	
0x5E	JESD204B Quick configuration	0x41 = four converters, one lane; 0x42 = four converters, two lanes; 0x44 = 0x22 = two converters, two lanes; 0x21 = two converters, one lane; 0x11 =								0x00	Self clearing always reads

										0x00.
0x5F	JESD204B Link CTRL 1	Open	Tail bits mode: 0 = fill with 0s, 1 = fill with 9-bit PN sequence	JTX transport layer test: 0 = not enabled, 1 = long transport layer test enabled	Multiframe alignment character insertion: 0 = disabled, 1 = enabled	ILAS mode: 00 = ILAS disabled, 01 = ILAS enabled (normal mode), 11 = ILAS always on (test mode)		Frame alignment character insertion: 0 = enabled, 1 = disabled	0 = JTX link enabled, 1 = JTX link disabled	0x14	
0x60	JESD204B Link CTRL 2	Reserved		SYNCINB± pin invert: 0 = not inverted, 1 = inverted	SYNCINB± pin input bias: 0 = disabled, 1 = enabled	Open	Open	JTX output invert: 0 = normal, 1 = inverted	Reserved	0x10	
0x61	JESD204B Link CTRL 3	Reserved	Reserved	Test data injection point: 01 = 10-bit data injected at 8b/10b encoder output, 10 = 8-bit data at scrambler input		JTX test mode patterns: 0000 = normal operation (test mode disabled), 0001 = alternating checkerboard, 0010 = 1/0 word toggle, 0011 = PN sequence PN23, 0100 = PN sequence PN9, 0101= continuous/repeat user test mode, 0110 = single user test mode, 0111 = reserved, 1000 = modified RPAT test sequence (8-bit data only), 1100 = PN sequence PN7, 1101 = PN sequence PN15, other setting are unused				0x00	
0x62	JESD204B Link CTRL 4	Reserved								0x00	

0x64	JESD204B DID Configuration	Device identification (DID) = C0					0xC0	Read Only
0x65	JESD204BBID Configuration	Open	Open	Open	Open	JTX bank identification (BID) number	0x00	
0x66	JESD204B LID Configuration 0	Open	Open	Open	JTX lane identification (LID) number for Lane 0		0x00	
0x67	JESD204B LID Configuration 1	Open	Open	Open	JTX lane identification (LID) number for Lane 1		0x01	
0x68	JESD204B LID Configuration 2	Open	Open	Open	JTX lane identification (LID) number for Lane 2		0x02	
0x69	JESD204B LID Configuration 3	Open	Open	Open	JTX lane identification (LID) number for Lane 3		0x03	
0x6E	JESD204B parameters, SCR/L	JESD204B scrambling (SCR): 0 = disabled, 1 = enabled	Open	Open	JESD204B serial lane control: 0 = one lane per link (L = 1), 1 = two lanes per link (L = 2), 2 = unused, 3 = four lanes per link (L = 4), 4 to 31 = unused		0x80	
0x6F	JESD204B parameters, F	JESD204B number of octets per frame (F); calculated value, F = (2 × M)/L					0x00	Read Only
0x70	JESD204B parameters, K	Open	Open	Open	JESD204B number of frames per multiframe (K); K = register contents + 1, but also must be a multiple of four octets		0x1F	
0x71	JESD204B parameters, M	JESD204B number of converters (M): 0 = one converter (M = 1), 1 = two converters (M = 2), 3 = four converters (M = 4, default)					0x03	
0x72	JESD204B parameters, CS/N	00 = number of control bits sent per sample (CS = 0)	Open	JTX converter resolution (N): 0x0F = 16-bit, 0x0D = 14-bit, 0x0B = 12-bit, 0x09 = 10-bit			0x0F	
0x73	JESD204B parameters, subclass/Np	JESD204B subclass; 0x0 = Subclass 0; 0x1 = Subclass 1 (default)		JESD204B number of bits per sample (N’); N’ = register contents + 1			0x2F	
0x74	JESD204B parameters, S	Reserved		JESD204B converter samples per frame (S); S = register contents + 1			0x20	Read Only
0x75	JESD204B parameters, HD and CF	JESD204B HD value =	Open	Open	JESD204B control words per frame clock cycle per link (CF = 0, fixed)		0x00	Read Only

		0									
0x76	JESD204BRESV1	JESD204B Serial Reserved Field No. 1 in link configuration, see Table 12 (RES1)								0x00	
0x77	JESD204BRESV2	JESD204B Serial Reserved Field No. 2 in link configuration, see Table 12 (RES2)								0x00	
0x78	JESD204BCHKSUM0	JESD204B serial checksum value in link configuration, see Table 12 for Lane 0 (FCHK)									Read Only
0x79	JESD204BCHKSUM1	JESD204B serial checksum value in link configuration, see Table 12 for Lane 1 (FCHK)									Read Only
0x7A	JESD204BCHKSUM2	JESD204B serial checksum value in link configuration, see Table 12 for Lane 2 (FCHK)									Read Only
0x7B	JESD204BCHKSUM3	JESD204B serial checksum value in link configuration, see Table 12 for Lane 3 (FCHK)									Read Only
0x80	JTX physical lane disable	Open	Open	Open	Open	Lane 3: 0 = enabled, 1 = disabled	Lane 2: 0 = enabled, 1 = disabled	Lane 1: 0 = enabled, 1 = disabled	Lane 0: 0 = enabled, 1 = disabled	0x00	Lane serialize and output driver powered down.
0x82	JESD204B Lane Assign 1	Open	Physical Lane 1 assignment: 000 = Logical Lane 0, 001 = Logical Lane 1, 010 = Logical Lane 2, 011 = Logical Lane 3			Open	Physical Lane 0 assignment: 000 = Logical Lane 0, 001 = Logical Lane 1, 010 = Logical Lane 2, 011 = Logical Lane 3			0x10	
0x83	JESD204B Lane Assign 2	Open	Physical Lane 3 assignment: 000 = Logical Lane 0, 001 = Logical Lane 1, 010 = Logical Lane 2, 011 = Logical Lane 3			Open	Physical Lane 2 assignment: 000 = Logical Lane 0, 001 = Logical Lane 1, 010 = Logical Lane 2, 011 = Logical Lane 3			0x32	
0x86	JESD204B Lane inversion	Open	Open	Open	Open	Lane 3: 0 = no invert, 1 = invert	Lane 2: 0 = no invert, 1 = invert	Lane 1: 0 = no invert, 1 = invert	Lane 0: 0 = no invert, 1 = invert	x00	
0x8B	JESD204BLMFC offset	Open	Open	Open	Local multiframe clock (LMFC) phase offset value; reset value for LMFC phase Local multiframe clock (LMFC) phase offset value; reset value for LMFC phase counter when SYSREF± is asserted; used for deterministic delay applications					0x00	

0xA0	JTX User Pattern Octet 0,LSB	User test pattern most significant byte,Octet 0								0x00	
0xA1	JTX User Pattern Octet 0,MSB	User test pattern most significant byte,Octet 0								0x00	
0xA2	JTX User Pattern Octet 1,LSB	User test pattern most significant byte,Octet 1								0x00	
0xA3	JTX User Pattern Octet 1,MSB	User test pattern most significant byte,Octet 1								0x00	
0xA4	JTX User Pattern Octet 2,LSB	User test pattern most significant byte,Octet 2								0x00	
0xA5	JTX User Pattern Octet 2,MSB	User test pattern most significant byte,Octet 2								0x00	
0xA6	JTX User Pattern Octet 3,LSB	User test pattern most significant byte,Octet 3								0x00	
0xA7	JTX User Pattern Octet 3,MSB	User test pattern most significant byte,Octet 3								0x00	
0xF5	JTX converter mapping	JTX Converter3: 0=ADCA, 1=ADCB, 2=ADCC, 3=ADCD		JTX Converter2: 0=ADCA, 1=ADCB, 2=ADCC, 3=ADCD		JTX Converter1: 0=ADCA, 1=ADCB, 2=ADCC, 3=ADCD		JTX Converter0: 0=ADCA, 1=ADCB, 2=ADCC, 3=ADCD		0xE4	
0x100	Resolution/sample rate override	Open	Override enable	Resolution: 0=16 bits, 1=14 bits, 2=12 bits,3=10bits	Open	Sample rate: 001=40MSPS, 010=50MSPS, 011=65MSPS, 100=80MSPS, 101=105MSPS, 110=125MSPS				0x00	Sample rate override(requires transfer register,0xFF).
0x101	User I/O Control 2	Open	Open	Open	Open	Open	Open	Open	SDIO pull-down	0x00	Disable SDIO pull-down

0x102	User I/O Control 3	Open	Open	Open	Open	VCM power-down	Open	Open	Open	0x00	VCM control
0x109	Clock divider sync control	Clock divider sync mode:0=use SYNC pin,1=use SYSREF±pins	Reserved					Reset clock divider sync received	Sync clock divider enable:0=disabled,1=enabled	0x00	
0x10A	Clock divider sync received	Open	Open	Open	Open	Open	Open	Open	Clock divider sync received	0x00	Read Only

MEMORY MAP REGISTER DESCRIPTIONS

For additional general information about functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, Interfacing to High Speed ADCs via SPI.

- **Device Index (Register 0x05)**

Certain features in the map that are designated as local can be set independently for each channel, whereas other features apply globally to all channels (depending on context), regardless of the channel is selected. Bits[3:0] of Register 0x05 can select which data channels are affected.

- **(Register 0xFF)**

All registers except Register 0x100 are updated the moment they are written. Setting Bit 0 of the transfer register high invokes the settings in the resolution/sample rate override register (Address 0x100).

- **Power Modes (Register 0x08)**

  - Bit 5—PDWN Pin Function

If set to 1, the PDWN pin initiates standby mode. If set to 0 (cleared), the PDWN pin initiates full power-down mode.

- Bit 4—JTX Standby Mode

If set, the JTX block enters standby mode when chip standby is activated. Only the PLL is left running in standby mode. If cleared, the JTX block remains running when chip standby is activated.

- Bits[1:0]—Power Mode

In normal operation (Bits[1:0] = 00), all ADC channels and the JTX block are active.

In full power-down mode (Bits[1:0] = 01), all ADC channels and the JTX block are powered down, and the digital datapath clocks are disabled, while the digital datapath is reset. The outputs are disabled.

In standby mode (Bits[1:0] = 10), all ADC channels are partially powered down, and the digital datapath clocks are disabled. If JTX standby mode is set, the outputs are also disabled.

During a digital reset (Bits[1:0] = 11), all the digital datapath clocks and the outputs (where applicable) on the chip are reset, except for the SPI port.

Note that the SPI is always left under control of the user; that is, it is never automatically disabled or in reset (except by power-on reset). When the digital reset is deactivated, a foreground calibration sequence is initiated.

- **Enhancement Control (Register 0x0C)**

- Bit 2—Chop Mode

For applications that are sensitive to offset voltages and other low frequency noise, such as

homodyne or direct conversion receivers, chopping in the first stage of the CD96AD56-125 is a feature that can be enabled by setting Bit 2. In the frequency domain, chopping translates offsets and other low frequency noise to $f_{CLK}/2$ where it can be filtered.

- **Output Mode (Register 0x14)**
  - Bits[7:5]—JTX CS Mode

Defines the meaning of the JTX control bits.

  - Bits[1:0]—Output Format

By default, this field is set to 1 for data output in twos complement format. Setting this field to 0 changes the output mode to offset binary.

- **Clock Phase Control (Register 0x16)**
  - Bits[6:4]—Input Clock Phase Adjust

When the clock divider (Register 0x0B) is used, the applied clock is at a higher frequency than the internal sampling clock. Bits[6:4] determine at which phase the external clock sampling occurs. This is only applicable when the clock divider is used. Setting Bits[6:4] greater than Register 0x0B, Bits[2:0] is prohibited.

- **JTX User Pattern (Register 0xA0 to Register 0xA7)**

The pattern in these registers is output on all active lanes when Register 0x61, Bits[3:0] are set to 5 or 6. A 32-bit pattern, the concatenation of Register 0xA0, Register 0xA2, Register 0xA4, and Register 0xA6 is inserted before the scrambler if Register 0x61, Bits[5:4] are set to 2. If Register 0x61, Bits[5:4] are set to 1 (a 40-bit pattern), the concatenation of Register 0xA1, Bits[1:0] and Register 0xA0, Bits[7:0]; Register 0xA3, Bits[1:0] and Register 0xA2, Bits[7:0]; Register 0xA5,

Bits[1:0] and Register 0xA4, Bits[7:0]; Register 0xA7, Bits[1:0] and Register 0xA6, Bits[7:0] is inserted after the 8b/10b encoder.

- **Resolution/Sample Rate Override (Register 0x100)**

This register allows the user to downgrade the resolution and/or the maximum sample rate (for lower power) in applications that do not require full resolution and/or sample rate. Settings in this register are not initialized until Bit 0 of the transfer register (Register 0xFF) is written high.

Bits[2:0] do not affect the sample rate; they affect the maximum sample rate capability of the ADC.

Writing to Register 0x100 reverts other registers to defaults. If nondefault configurations are desired, write to Register 0x100 first, and then perform other desired SPI operations to preserve the desired configuration.

- **User I/O Control 2 (Register 0x101)**

Bit 0—SDIO Pull-Down

Bit 0 can be set to disable the internal 30 kΩ pull-down resistor on the SDIO pin. This setting can limit the loading when many devices are connected to the SPI bus.

- **User I/O Control 3 (Register 0x102)**

Bit 3—VCM Power-Down

Bit 3 can be set high to power down the internal VCM generator. This feature is used when applying an external reference.

Application Descriptions

- **DESIGN GUIDELINES**

Before starting system level design and layout of the CD96AD56-125, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

- **CLOCK STABILITY CONSIDERATIONS**

When powered on, the CD96AD56-125 enters an initialization phase during which an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the CD96AD56-125 requires a stable clock. If the ADC clock source is not present or not stable during ADC power-up, it disrupts the state machine and causes the ADC to start up in an unknown state. To correct this, an initialization sequence must be reinvoked after the ADC clock is stable by issuing a digital reset via Register 0x08. In the default configuration (internal V_{REF}, ac-coupled input) where V_{REF} and V_{CM} are supplied by the ADC itself, a stable clock during power-up is sufficient. In the case where V_{REF} and/or V_{CM} are supplied by an external source, these, too, must be stable at power-up; otherwise, a subsequent digital reset via Register 0x08 is needed. Interruption of the sample clock during operation and changes in sample rate also necessitate a digital reset. The pseudo code sequence for a digital reset is as follows:

SPI_Write (0x08, 0x03); # Digital Reset SPI_Write (0x08, 0x00); # Normal Operation

- **EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS**

It is mandatory that the exposed pad on the underside of the ADC connect to analog ground (AGND) to achieve the best electrical and thermal performance. A continuous, exposed (no

solder mask) copper plane on the PCB must mate to the CD96AD56-125 exposed pad, Pin 0.

The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. Fill or plug these vias with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and the PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This partitioning prevents the solder from pooling and provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. See the evaluation board for a PCB layout example. For detailed information about the packaging and PCB layout of chip scale packages, refer to the AN-772 Application Note, A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP).

- **VCM**

Decouple the VCM pin to ground with a 0.1μF capacitor.

- **REFERENCE DECOUPLING**

Externally bypass the VREF pin to ground with a low ESR, 1.0 μF capacitor in parallel with a low ESR, 0.1 μF ceramic capacitor.

- **SPI PORT**

When the full dynamic performance of the converter is required, do not activate the SPI port. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other

devices, it may be necessary to provide buffers between this bus and the CD96AD56-125 to keep these signals from transitioning at the converter input pins during critical sampling periods.

- **POWER AND GROUND RECOMMENDATIONS**

When connecting power to the CD96AD56-125, it is recommended to use separate 1.8 V supplies: one supply for analog (AVDD), a separate shared supply for the digital outputs (DRVDD), and the digital (DVDD). DRVDD must be kept at the same voltage as DVDD. SVDD can be shared with any of the other supplies if 1.8 V SPI operation is desired. The designer can use several different decoupling capacitors to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PCB level and close to the pins of the device with minimal trace length.

When using the CD96AD56-125, a single PCB ground plane is sufficient. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

Package Outline Dimensions

QFN-56

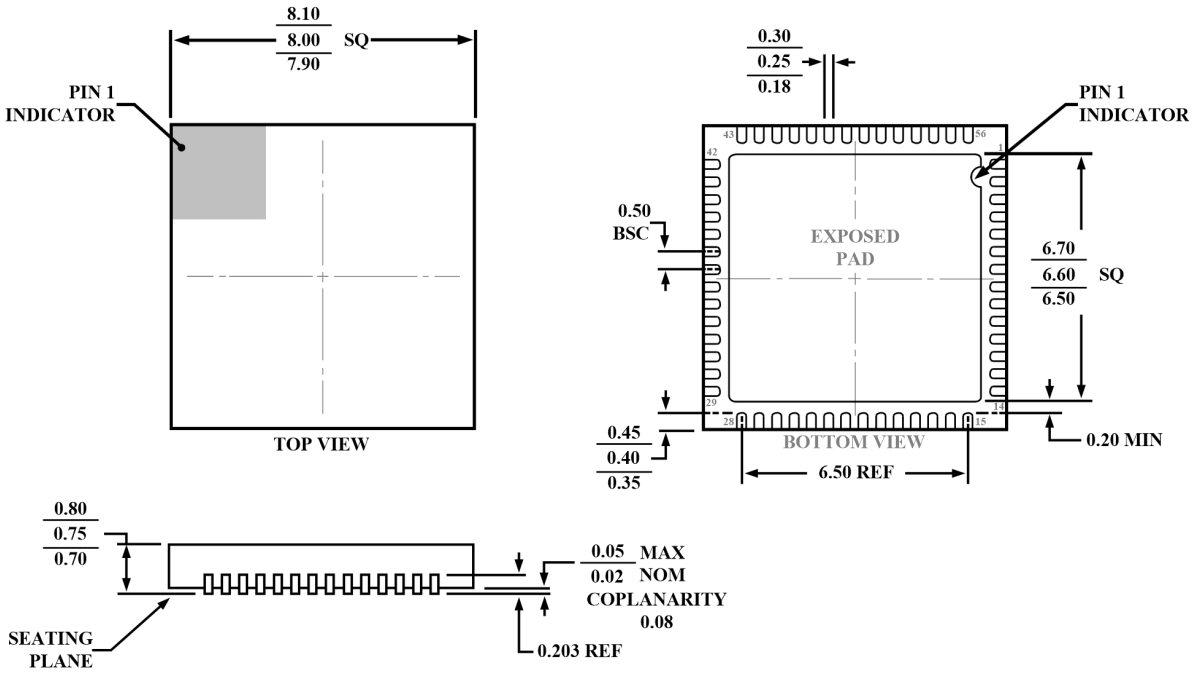

Figure 63.56 Pin lead packaging (plastic packaging)

8mm×8mm，Dimensions shown in millimeters

Figure 17. 72-Lead Outline Package [QFN]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD96AD56-125	-40℃+85℃	QFN-56	Tray，260

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.5.20	Initial version	Regular update	WW	LYL	