CoreadDvices
承芯微电子

CDLM321_CDLM358_CDLM324

Dual-Channel High-Voltage Operational Amplifier

Version: Rev 1.0.0 Date: 2025-5-26

Features

- Single-Supply Operation from +3V ~+24V
- Dual-Supply Operation from 1.5V ~ 12V
- Gain-Bandwidth Product: 1MHz (Typ.)
- Low Input Bias Current: 45nA ±(Typ.)
- Low Offset Voltage: 5mV (Max.)
- Quiescent Current: 250μA per Amplifier (Typ.)
- Operating Temperature: -25°C ~ +80°C
- Small Package:

  CDLM321 Available in SOT23-5 SC70-5 Packages

  CDLM358 Available in SOP-8 and MSOP-8 Packages

  CDLM324 Available in SOP-14 Package

Application

- Walkie-Talkie
- Battery Management
- Transducer Amplifiers
- Summing Amplifiers
- Multivibrators
- Oscillators
- Portable Systems

Description

The CDLM358 family have a high gain-bandwidth product of 1MHz, a slew rate of 0.4V/μs, and a quiescent current of 250μA/amplifier at 5V. The CDLM358 family is designed to provide optimal performance in low voltage and low noise systems.

The maximum input offset voltage is 5mV for CDLM358 family. The operating range iμs from 3V to 24V. The CDLM321 single is availμable in Green SOT-23-5 packages. The CDLM358 Dual is available in Green SOP-8 and MSOP-8 packages. The CDLM324 Quad is available in Green SOP-14 package.

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Chinese version:CDLM321_CDLM358_CDLM324

Contents

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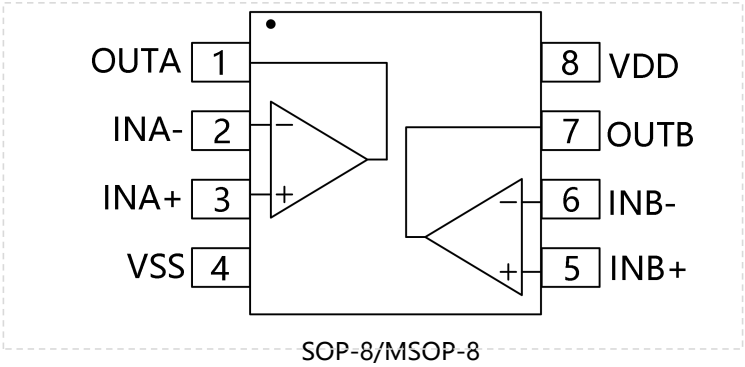
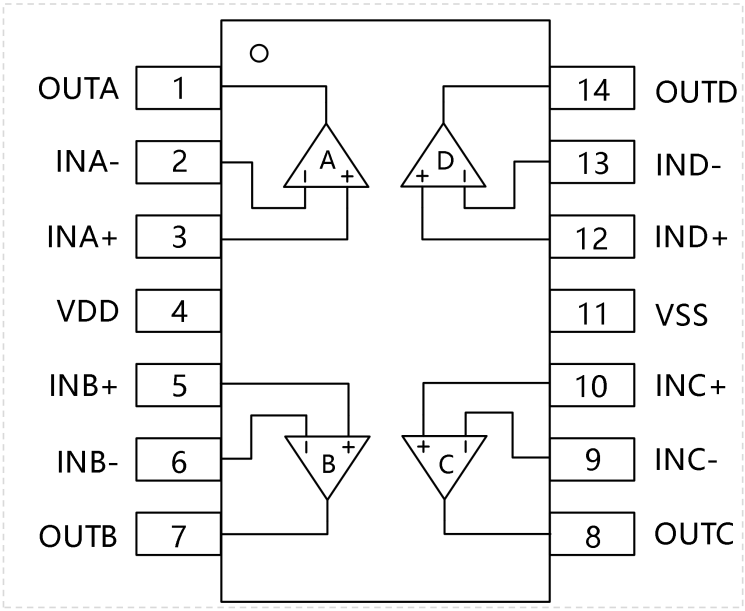
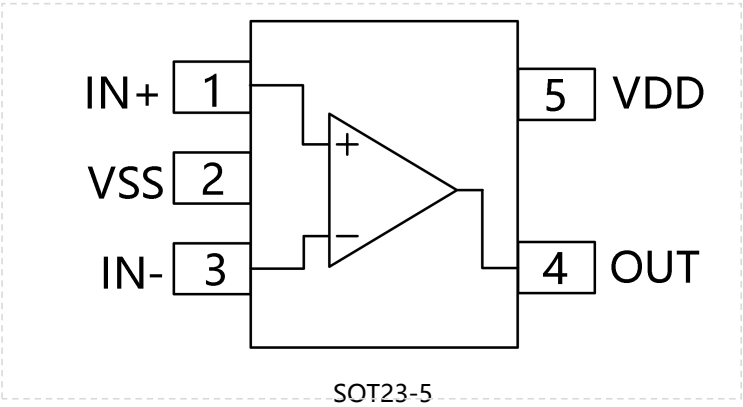
Pin Configurations



SOP-8/MSOP-8



SOP14



SOT23-5

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Absolute Maximum Ratings

Condition	Symbol	Max
Power Supply Voltage	V_{CC}	±12V or 24V
Differential input voltage	V_I(DIFF)	24V
Input Voltage	V_I	-0.3V~24V
Operating Temperature Range	T_{OPR}	-25℃ ~+80℃
Storage Temperature Range	T_{STG}	-65℃ ~+150℃

Electrical characteristics

(At V_S = +15V, T_A=25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	CDLM321/CDLM358/CDLM324			
			TYP	MIN/MAX OVER TEMPERATURE		
			+25℃	+25℃	UNITS	MIN/MAX
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	V_{CM} = VS/2	0.4	5	mV	MAX
Input Bias Current	I_B		44		nA	TYP
Input Offset Current	I_{OS}		3		nA	TYP
Common-Mode Voltage Range	V_{CM}	V_S = 5.5V	-0.1 to +4		V	TYP
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0V to V_S-1.5V	90	70	dB	MIN
Open-Loop Voltage Gain	A_{OL}	R_L = 5kΩ,V_O = 1V to 11V	100	90	dB	MIN
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		7		μV/℃	TYP
OUTPUT CHARACTERISTICS						
Output Voltage Swing from Rail	V_{OH}	R_L = 2kΩ	11		V	MIN
	V_{OL}	R_L = 2kΩ	5	20	mV	MAX
	V_{OH}	R_L = 10kΩ	12	13	V	MIN
	V_{OL}	R_L = 10kΩ	5	20	mV	MAX
Output Current	I_{SOURCE}	R_L = 10Ω to V_S/2	40	60	mA	MAX
	I_{SINK}		40	60		
POWER SUPPLY						
Operating Voltage Range				3	V	MIN
				24	V	MAX
Power Supply Rejection Ratio	PSRR	V_S = +5V to +30V, V_{CM} = +0.5V	100	75	dB	MIN

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Quiescent Current / Amplifier	I_Q		250	400	μA	MAX
DYNAMIC PERFORMANCE						
Gain-Bandwidth Product	GBP		1		MHz	TYP
Slew Rate	SR	G = +1, 2V Output Step	0.4		V/μs	TYP

Typical Characteristics

Fig.1 Input Voltage Range

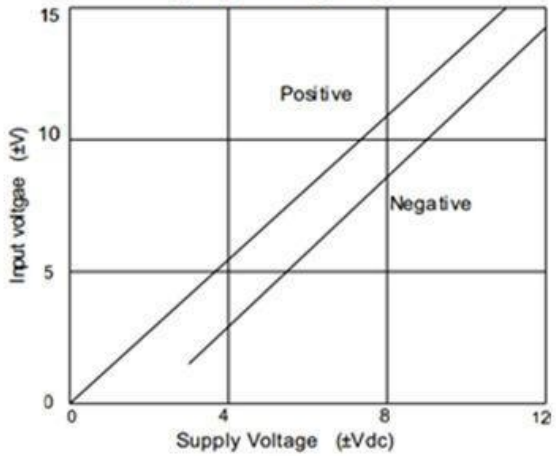

Fig.2 Input Current

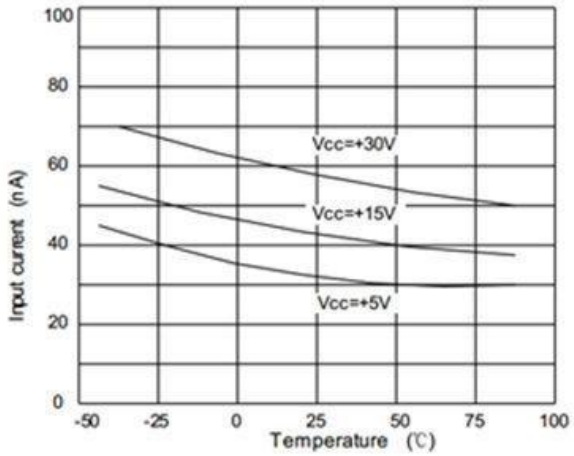

Fig.3 Supply Current

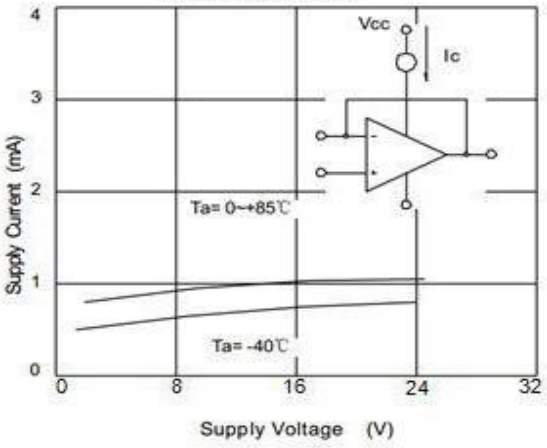

Fig.4 Voltage Gain

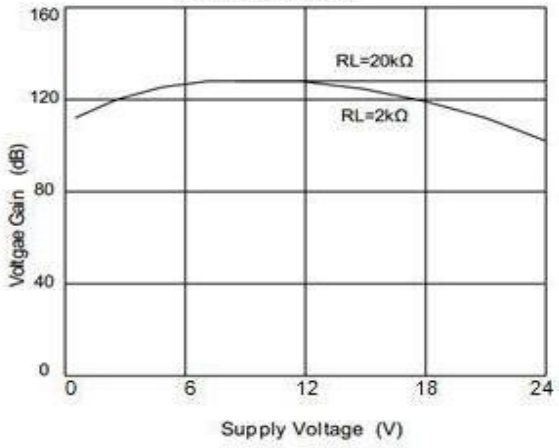

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Fig.5 Open Loop Frequency response

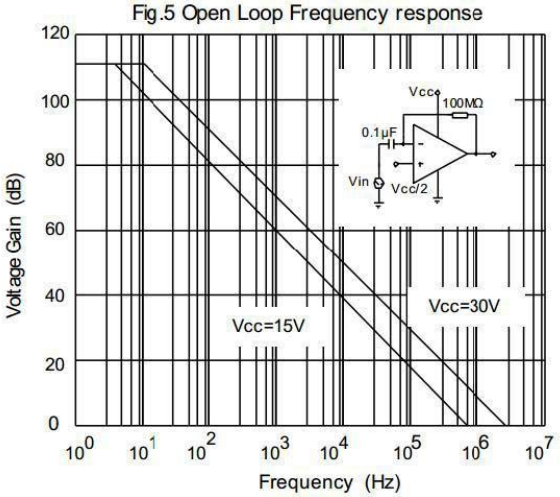

Fig.6 Common-mode rejection Ratio

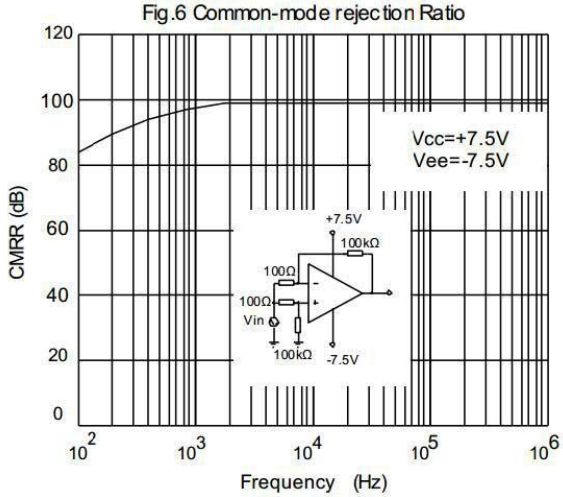

Fig.7

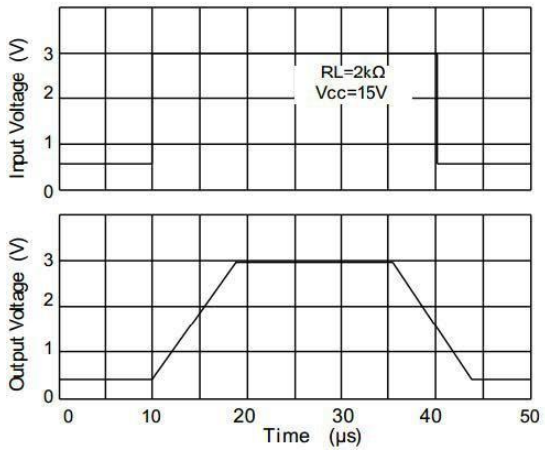

Fig.8 voltage Follower pulse response (small signal)

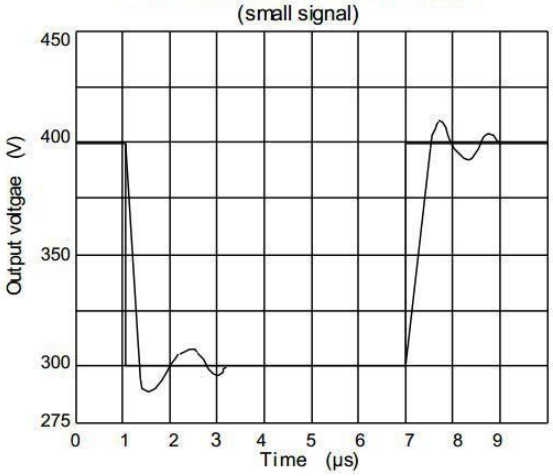

Fig.9 Large signal Frequency Response

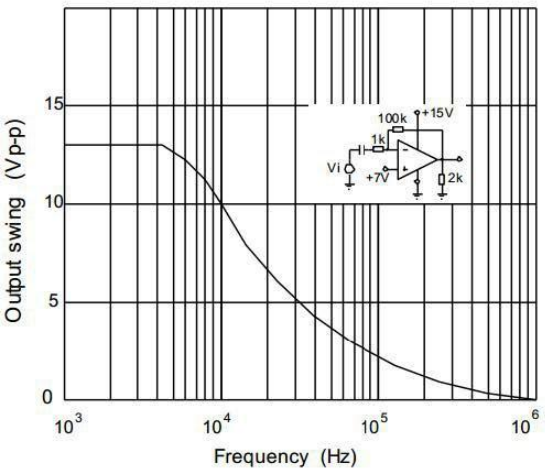

Fig.10 Output Characteristics current sourcing

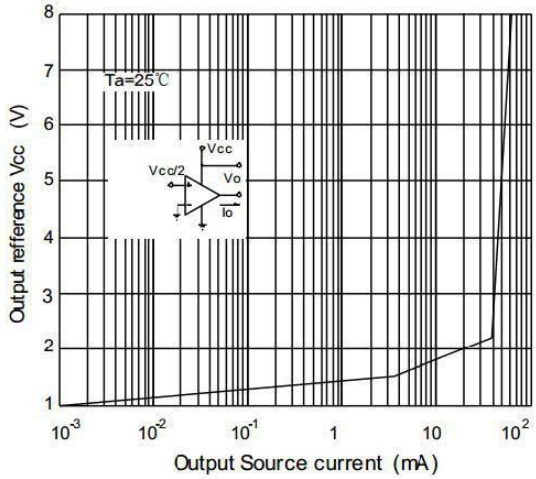

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Fig.11 Output Characteristics Current sinking

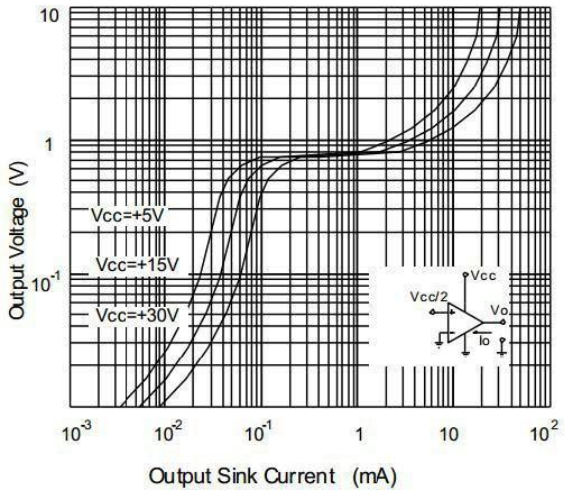
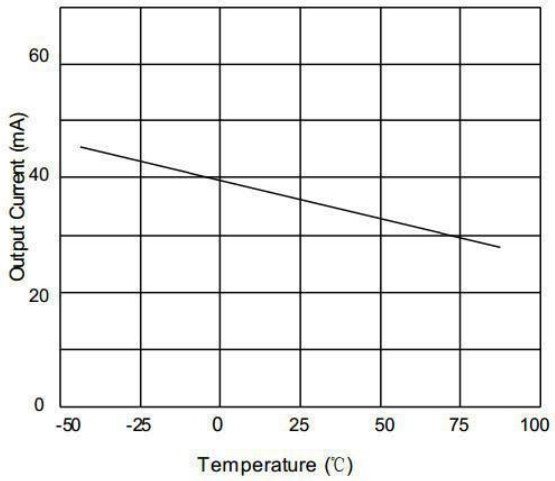


Fig.12 Current Limiting



Application Notes

Size

CDLM358 family series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The small footprints of the CDLM358 family packages save space on printed circuit boards and enable the design of smaller electronic products.

Power Supply Bypassing and Board Layout

CDLM358 family series operates from a single 3V to 24V supply or dual ±1.5V to ±12V supplies. For best performance, a 0.1μF ceramic capacitor should be placed close to the VDD pin in single supply operation. For dual supply operation, both VDD and VSS supplies should be bypassed to ground with separate 0.1μF ceramic capacitors.

Low Supply Current

The low supply current (typical 250uA per channel) of CDLM358 family will help to maximize battery life.

Operating Voltage

CDLM358 family operates under wide input supply voltage (3V to 24V). In addition, all temperature specifications apply from -25 ℃ to +80℃. Most behavior remains unchanged throughout the full operating voltage range. These guarantees ensure operation throughout the single Li-Ion battery lifetime

Capacitive Load Tolerance

The CDLM358 family is optimized for bandwidth and speed, not for driving capacitive loads. Output capacitance will create a pole in the amplifier’ s feedback path, leading to excessive peaking and potential oscillation. If dealing with load capacitance is a requirement of the application, the two strategies to consider are (1) using a small resistor in series with the amplifier’ s output and the load capacitance and (2) reducing the bandwidth of the amplifier’ s

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feedback loop by increasing the overall noise gain. Figure 2. shows a unity gain follower using the series resistor strategy. The resistor isolates the output from the capacitance and, more importantly, creates a zero in the feedback path that compensates for the pole created by the output capacitance.

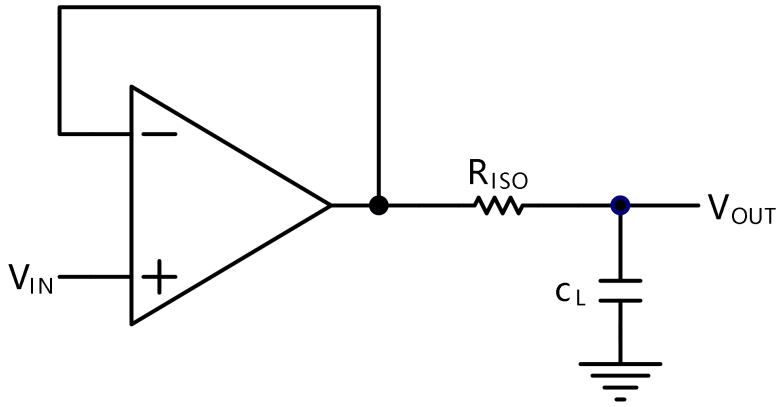

Figure 2. Indirectly Driving a Capacitive Load Using Isolation Resistor

The bigger the RISO resistor value, the more stable VOUT will be. However, if there is a resistive load RL in parallel with the capacitive load, a voltage divider (proportional to RISO/RL) is formed, this will result in a gain error.

The circuit in Figure 3 is an improvement to the one in Figure 2. RF provides the DC accuracy by feed-forward the VIN to RL. CF and RISO serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier’ s inverting input, thereby preserving the phase margin in the overall feedback loop. Capacitive drive can be increased by increasing the value of CF. This in turn will slow down the pulse response.

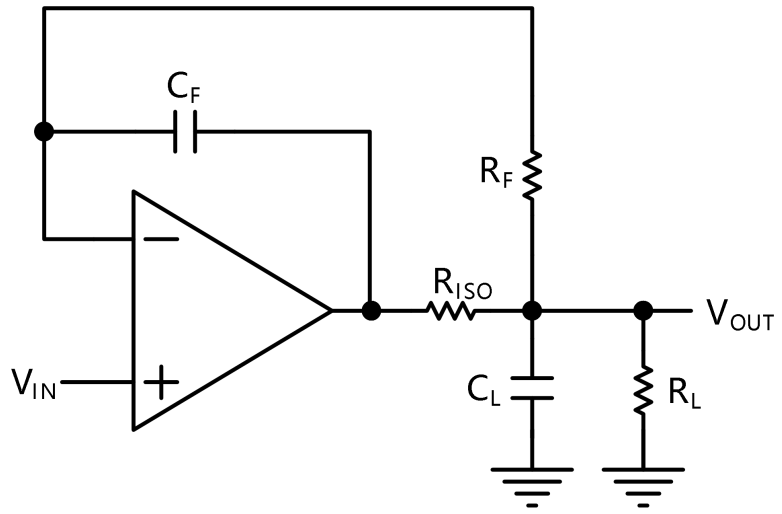

Figure 3. Indirectly Driving a Capacitive Load with DC Accuracy

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Typical Application Circuits

Differential amplifier

The differential amplifier allows the subtraction of two input voltages or cancellation of a signal common the two inputs. It is useful as a computational amplifier in making a differential to single-end conversion or in rejecting a common mode signal. Figure 4. shown the differential amplifier using CDLM358 family.

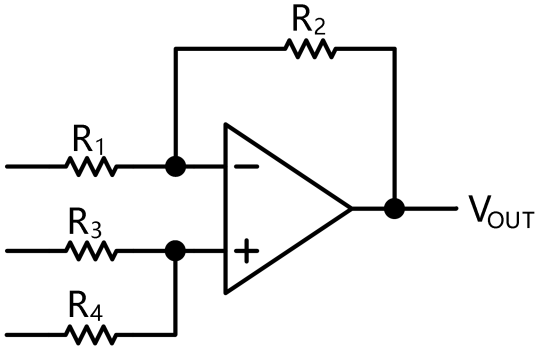


Figure 4. Differential Amplifier

$$V_{OUT} = \left(\frac{R_1 + R_2}{R_3 + R_4}\right)\frac{R_4}{R_1}V_{IN} - \frac{R2}{R1}V_{IP} + \left(\frac{R_1 + R_2}{R_3 + R_4}\right)\frac{R_3}{R_1}V_{REF}$$

If the resistor ratios are equal (i.e. R1=R3 and R2=R4), then

$$V_{OUT} = \frac{R_2}{R_1}(V_{IP} - V_{IN}) + V_{REF}$$

Low Pass Active Filter

The low pass active filter is shown in Figure 5. The DC gain is defined by –R2/R1. The filter has a -20dB/decade roll-off after its corner frequency $f_C = 1/(2\pi R_3 C_1)$.

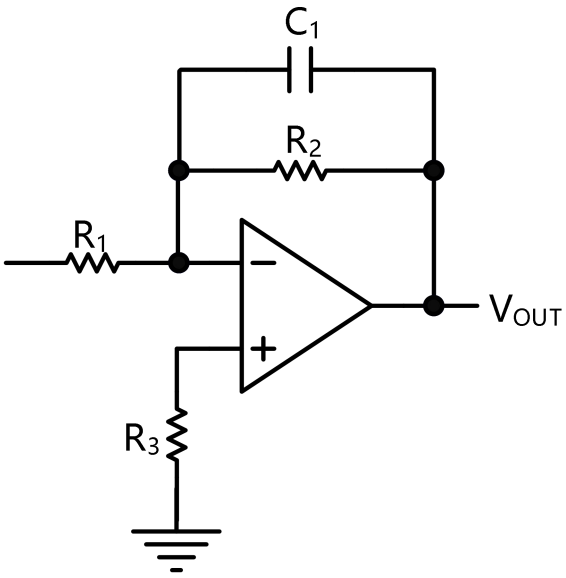


Figure 5. Low Pass Active Filter

Instrumentation Amplifier

The triple CDLM358 family can be used to build a three-op-amp instrumentation amplifier as shown in Figure 6. The amplifier in Figure 6 is a high input impedance differential amplifier with gain of R2/R1. The two differential voltage followers assure the high input impedance of the amplifier.

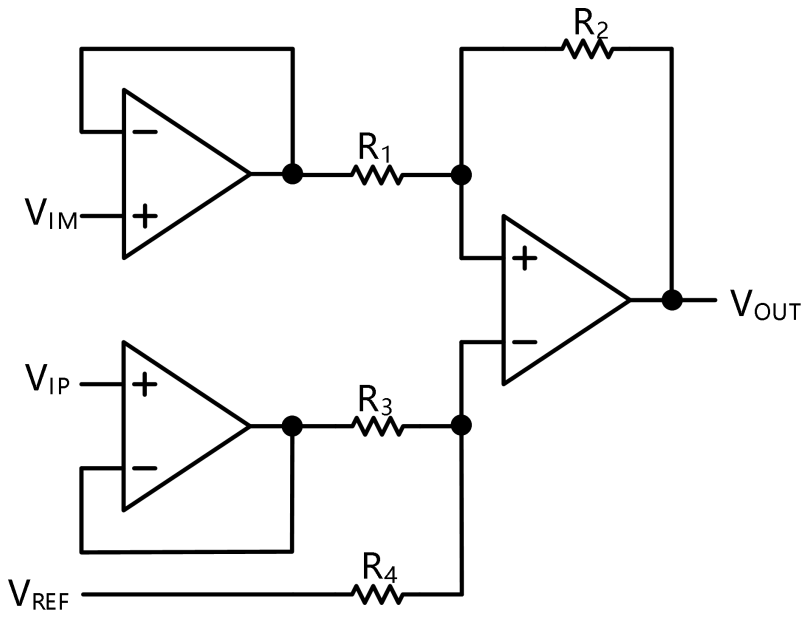
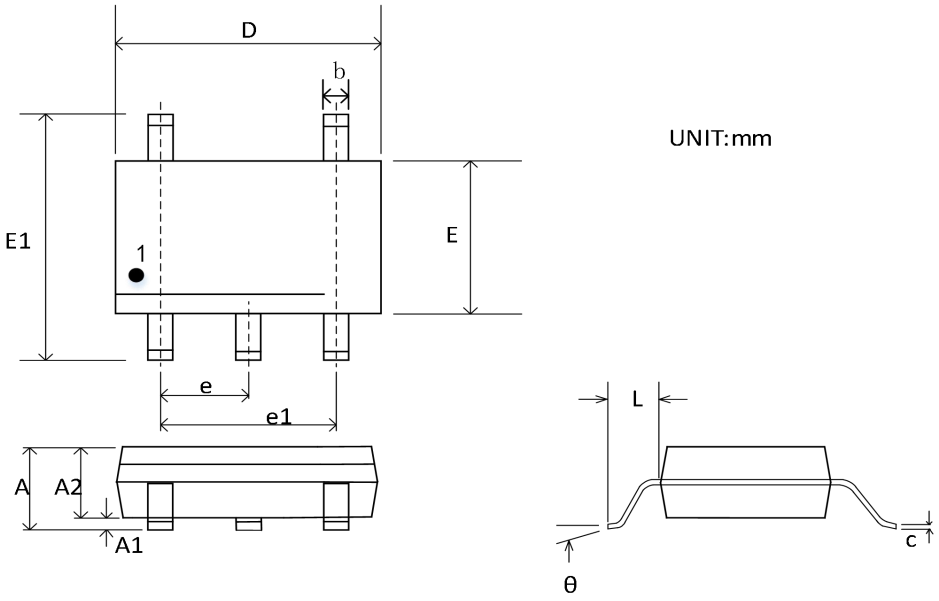


Figure 6. Instrument Amplifier

Package Outline Dimensions

SOT23-5



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.650	2.950
e	0.950 BSC	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

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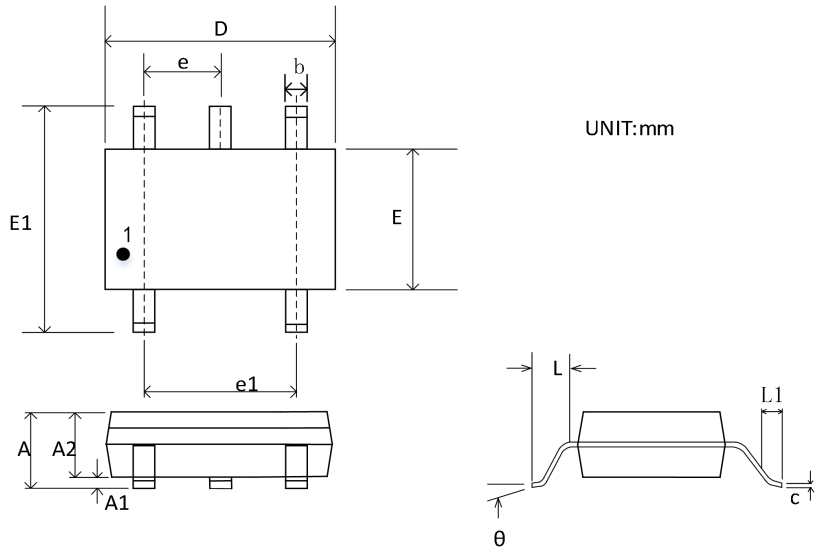
SC70-5



Symbol	Dimensions In Millimeters	
	Min	Max
A	0.900	1.100
A1	0.000	0.100
A2	0.900	1.000
b	0.150	0.350
C	0.080	0.150
D	2.000	2.200
E	1.150	1.350
E1	2.150	2.450
e	0.650 TYP	
e1	1.200	1.400
L	0.525 REF	
L1	0.260	0.460
θ	0°	8°

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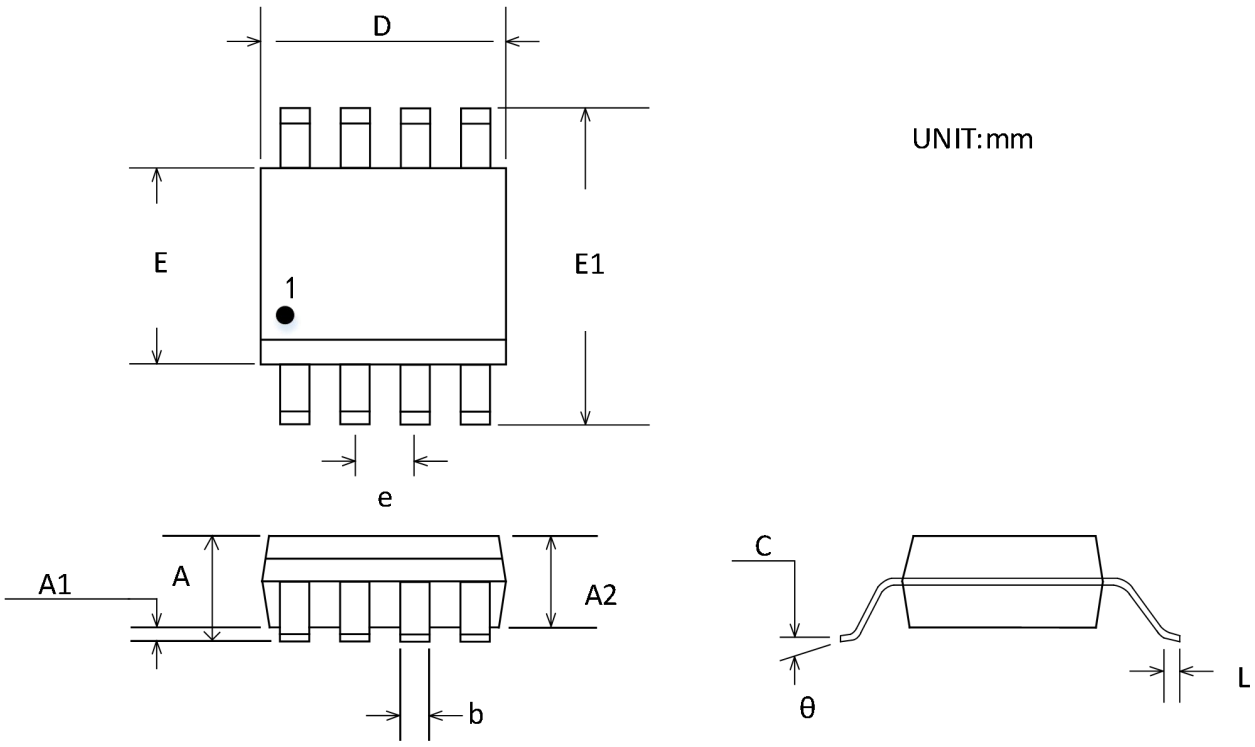
MSOP-8



UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	0.820	1.100
A1	0.020	0.150
A2	0.750	0.950
b	0.250	0.380
c	0.090	0.230
D	2.900	3.100
E	2.900	3.100
E1	4.750	5.050
e	0.650 BSC	
L	0.400	0.800
θ	0°	6°

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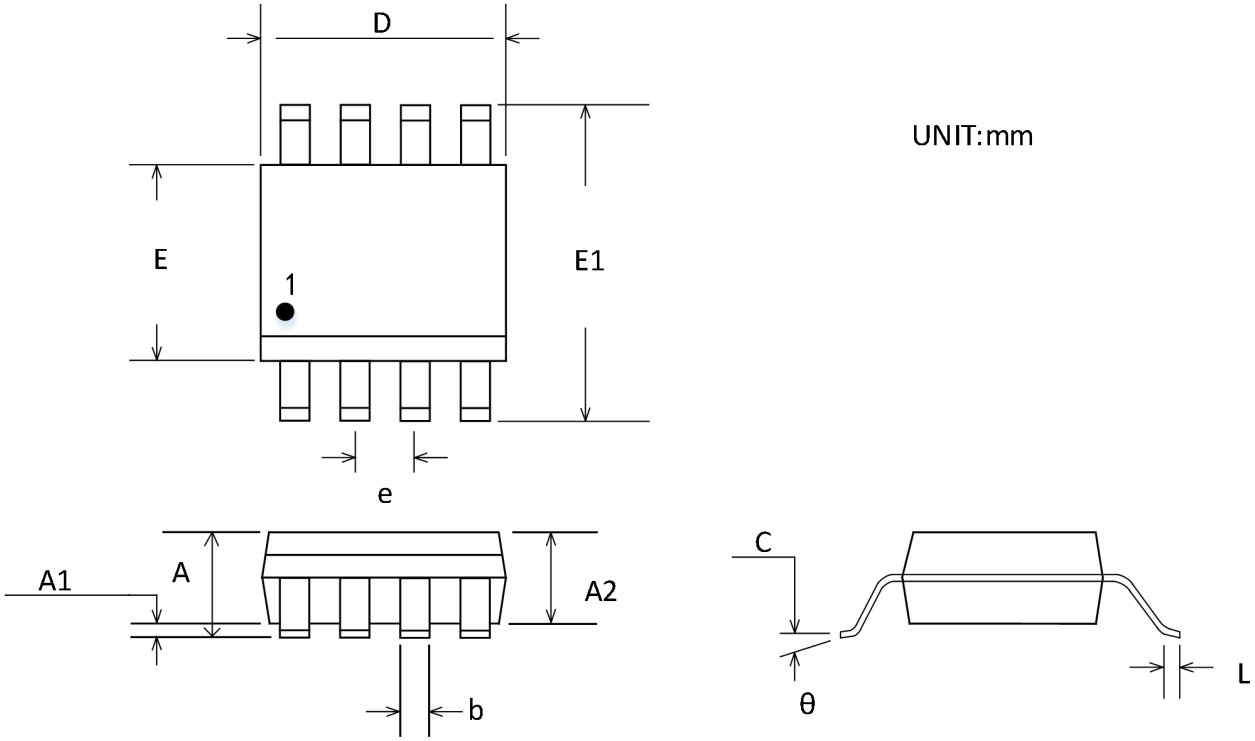
SOP-8



UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.800	5.000
E	3.800	4.000
E1	5.800	6.200
e	1.270 BSC	
L	0.400	1.270
θ	0°	8°

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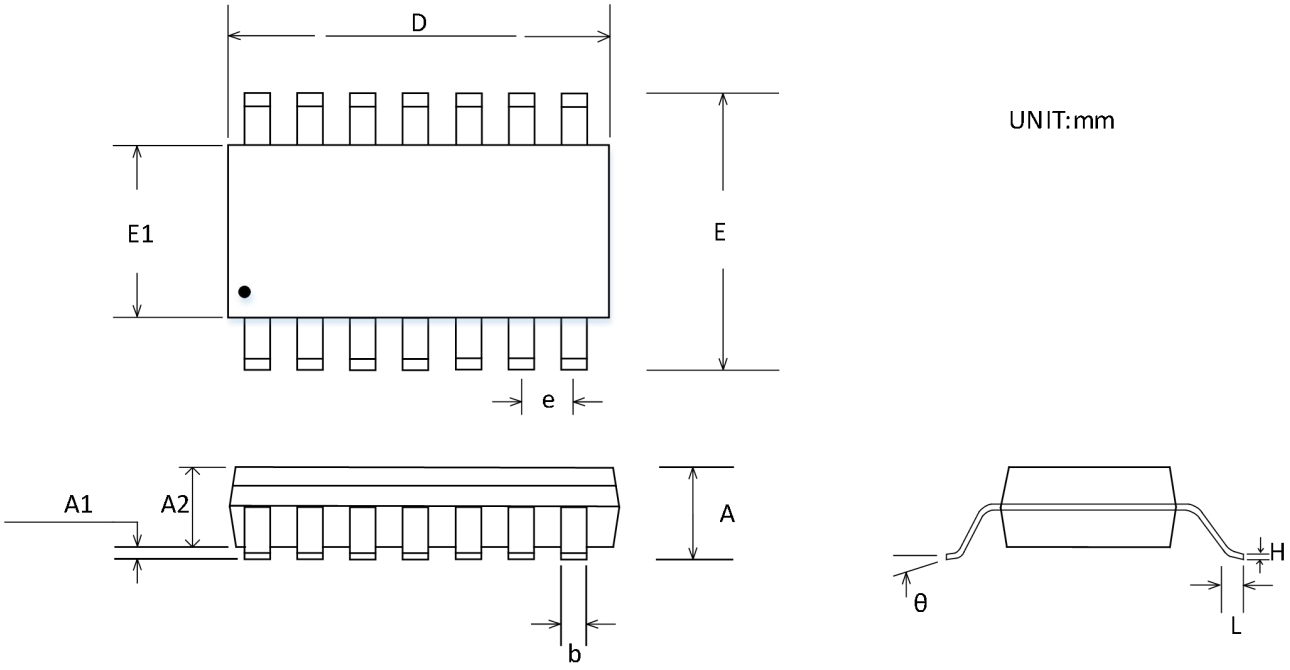
SOP-14



UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
b	0.31	0.51
D	8.55	8.75
E	5.80	6.20
E1	3.80	4.00
e	1.27BSC	
H	0.17	0.25
L	0.40	1.27
θ	0°	8°

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Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDLM358AS8	-25℃~80℃	SOP-8	Tape and Reel,2500
CDLM358AS8-RL	-25℃~80℃	SOP-8	Tape and Reel,3000
CDLM358AS8-REEL	-25℃~80℃	SOP-8	Tape and Reel,4000
CDLM358AMS8	-25℃~80℃	MSOP-8	Tape and Reel,3000
CDLM324AS14	-25℃~80℃	SOP-14	Tape and Reel,2500
CDLM324AS14-RL	-25℃~80℃	SOP-14	Tape and Reel,3000
CDLM324AS14-REEL	-25℃~80℃	SOP-14	Tape and Reel,4000
CDLM321AST5	-25℃~80℃	SOT23-5	Tape and Reel,3000
CDLM321ASC7	-25℃~80℃	SC70-5	Tape and Reel,3000

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Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.5.26	Initial version	Regular update	WW	LYL	