CoreadDvices
承芯微电子

CD1040

High speed CAN transceiver

Version: Rev 1.0.0 Date: 2025-6-25

Features

- Fully compatible with the ISO 11898 standard
- High speed (up to 1 MBaud)
- Very low-current standby mode with remote wake-up capability via the bus
- Very low ElectroMagnetic Emission (EME)
- Differential receiver with high common-mode range for ElectroMagnetic Immunity (EMI)
- Transceiver in unpowered state disengages from the bus (zero load)
- Input levels compatible with 3.3 V and 5 V devices
- Voltage source for stabilizing the recessive bus level if split termination is used (further improvement of EME)
- At least 110 nodes can be connected
- Transmit Data (TXD) dominant time-out function
- Bus pins protected against transients in automotive environments
- Bus pins and pin SPLIT short-circuit proof to battery and ground
- Thermally protected.

Application

- Automotive Electronics

Chinese version:CD1040

Description

The CD1040 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is primarily intended for high speed applications, up to 1 MBaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The CD1040 is the next step up from the CD1050 high speed CAN transceiver. Being pin compatible and offering the same excellent EMC performance, the CD1040 also

features:

An ideal passive behaviour when supply voltage is off

A very low-current standby mode with remote wake-up capability via the bus.

This makes the CD1040 an excellent choice in nodes which can be in power-down or standby mode in partially powered networks.

The CD1040 is available in 8-lead SOP packages.

Contents

Pin Configurations

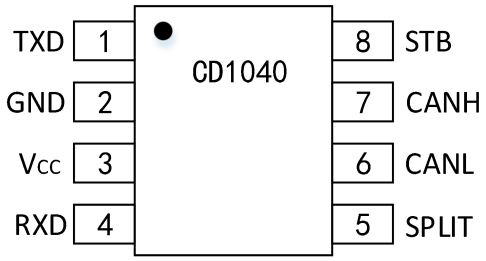


Figure 1. SOP8 Pin Configuration

Pin Description

Table 1. Pin description

Pin No.	Pin Name	Description
1	TXD	transmit data input
2	GND	ground supply
3	V_{CC}	supply voltage
4	RXD	receive data output; reads out data from the bus lines
5	SPLIT	common-mode stabilization output
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	standby mode control input

Notes:

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor via a 0.75 µH series inductor and a 10 Ω series resistor.
3. Junction temperature in accordance with IEC 60747-1. An alternative definition of Tvj is: Tvj = Tamb + P × Rth(vj-amb),
where Rth(vj-amb) is a fixed value to be used for the calculating of Tvj. The rating for Tvj limits the allowable combinations of power dissipation (P) and ambient temperature (Tamb).

Functional Block diagram

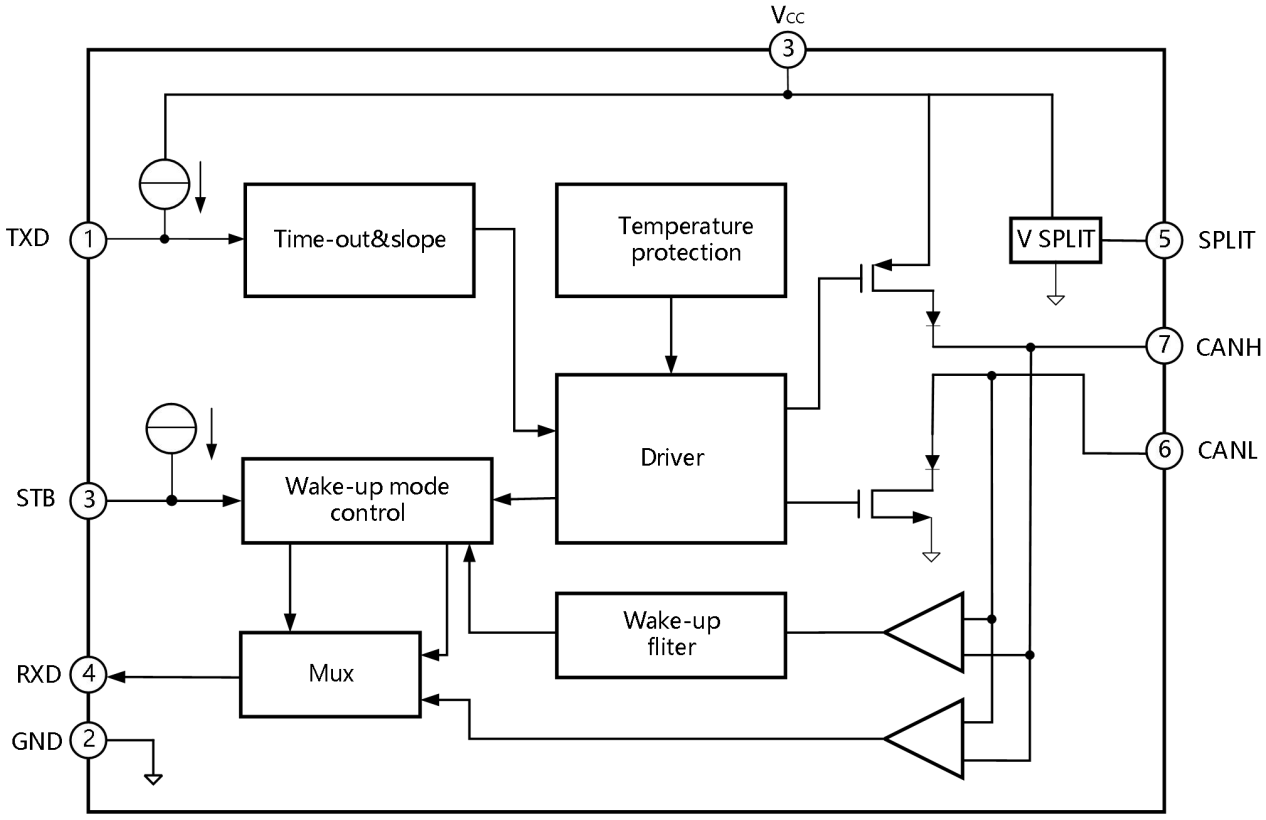


Figure 2. Functional Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Numerical range	Units
supply voltage	V_{CC}	no time limit	-0.3~6	V
		operating range	4.75~5.25	V
DC voltage on pin TXD	V_{TXD}		-0.3~VCC+0.3	V
DC voltage on pin RXD	V_{RXD}		-0.3~VCC+0.3	V
DC voltage on pin STB	V_{STB}		-0.3~VCC+0.3	V
DC voltage on pin CANH	V_{CANH}	0<VCC<5.25V, no time limit	-27~40	V
DC voltage on pin CANL	V_{CANL}	0<VCC<5.25V, no time limit	-27~40	V
DC voltage on pin SPLIT	V_{SPLIT}	0<VCC<5.25V, no time limit	-27~40	V
Transient voltages on pins CANH, CANL and SPLIT	V_{TRT}	according to ISO7637	-200~200	V
electrostatic discharge voltage	V_{ESD}	Human Body Model (HBM); note 1 pins CANH and CANL and SPLIT −6 +6 kV	-6~6	kV
		all other pins	-4~4	kV
		Machine Model (MM); note 2	-200~200	V
virtual junction temperature	T_{VJ}	note 3	-40~150	℃
Storage temperature	T_{STG}		-55~150	℃
Lead Temperature (soldering, 10sec)	T_{LEAD}	--	245	℃

Electrical Characteristics

VCC = 4.75 to 5.25 V, T_{vj} = −40 to +150 °C and R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC; note 1.

表 3.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply (pin V_{CC})						
supply current	I_{CC}	standby mode	5	10	15	μA
		normal mode : recessive $V_{TXD}=V_{CC}$	2.5	5	10	mA
		normal mode : dominant $V_{TXD}=0V$	30	50	70	mA
Transmit data input (pin TXD)						
HIGH-level input voltage	V_{IH}		2	--	V_{CC}+0.3	V
LOW-level input voltage	V_{IL}		-0.3	--	0.8	V
HIGH-level input current	I_{IH}	$V_{TXD}=V_{CC}$	-5	0	5	μA
LOW-level input current	I_{IL}	normal mode: $V_{TXD}=0V$	-100	-200	-300	μA
input capacitance	C_I	not tested	--	5	10	pF
Standby mode control input (pin STB)						
HIGH-level input voltage	V_{IH}		2	--	V_{CC}+0.3	V
LOW-level input voltage	V_{IL}		-0.3	--	0.8	V
HIGH-level input current	I_{IH}	$V_{STB}=V_{CC}$	--	0	--	mA
LOW-level input current	I_{IL}	$V_{STB}=0V$	-1	-4	-10	mA
Receive data output (pin RXD)						
HIGH-level output voltage	V_{OH}	standby: I_{RXD}=-100μA	V_{CC}-1.1	V_{CC}-0.7	V_{CC}-0.4	V
HIGH-level output current	I_{OH}	normal mode: V_{RXD}=-V_{CC}-0.4	-0.1	-0.4	-1	mA
LOW-level output current	I_{OL}	V_{RXD}=0.4	2	6	20	mA
Common-mode stabilization output (pin SPLIT)						
output voltage	V_O	normal mode:	0.3V_{CC}	0.5VCC	0.7V_{CC}	V

		-500<I_O<500μA				
leakage current	$\|I_L\|$	standby mode: -22V<V_{SPLIT}<35V	--	0	5	μA
Bus lines (pins CANH and CANL)						
dominant output voltage	$V_{(CANH)(dom)}$	V_{TXD} = 0V	3	3.6	4.25	V
dominant output voltage	$V_{(CANL)(dom)}$	V_{TXD} = 0V	0.5	1.4	1.75	V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bus lines (pins CANH and CANL)						
matching of dominant output voltage (VCC - V_{CANH} - V_{CANL})	VO(Dom)(m)		-100	0	150	mV
differential bus output voltage (V_{CANH} −V_{CANL})	VO(dif)(bus)	V_{TXD} = 0V; dominant; 45Ω< R_L <65Ω	1.5	--	3	V
		V_{TXD} = V_{CC}; recessive; no load	-50	--	50	mV
recessive output voltage	$V_{(CANL)}$ (reces)	normal mode: V_{TXD} = V_{CC}; no load	2	0.5 V_{CC}	3	V
		standby mode; no load	-0.1	0	0.1	V
short-circuit output current	$I_{O(CANL)}$ (reces)	V_{TXD} = 0V; V_{CANH} = 0V	-40	-70	-95	mA
	$I_{O(CANL)}$ (sc)	V_{TXD} = 0V; V_{CANL} = 40V	40	70	100	mA
recessive output current	$I_{O(CANH)}$ (sc)	-27V<V_{CAN}<32V	-2.5	--	2.5	mA
differential receiver threshold voltage	$V_{dif(th)}$	− 12V < V_{CANH} < 12V; normal mode	0.5	0.7	0.9	V
		− 12V < V_{CANL} < 12V standby mode	0.5	0.7	1.15	V
differential receiver hysteresis voltage	$V_{dif(hys)}$	normal mode −12V < VCANH < 12V; −12V < VCANL < 12V;	50	70	100	mV
input leakage current	ILI	V_{CC} = 0V,V_{CANH} = V_{CANL}= 5V	-5	0	5	μA
common-mode input resistance	Ri(cm)	standby or normal mode	15	25	35	kΩ
common-mode input resistance matching	Ri(cm)(m)	V_{CANH} = V_{CANL}	-3	0	3	%

differential input resistance	$R_{i(dif)}$	standby or normal mode	25	50	75	kΩ
Timing characteristics;						
delay TXD to bus active	$t_{d(TXD-BUSon)}$	normal mode	25	70	110	ns
delay TXD to bus inactive	$t_{d(TXD-BUSoff)}$		10	50	95	ns
delay bus active to RXD	$t_{d(BUSon-RXD)}$		15	65	115	ns
delay bus inactive to RXD	$t_{d(BUSoff-RXD)}$		35	100	160	ns
propagation delay TXD to RXD	$t_{PD(TXD-RXD)}$	V_{STB} = 0V	40	--	255	ns
TXD dominant time-out	$t_{dom(TXD)}$	V_{TXD} = 0V	300	600	1000	μs
dominant time for wake-up via bus	t_{BUS}	standby mode	0.75	1.75	5	μs
delay standby mode to normal mode	$t_{d(stb-norm)}$	normal mode	5	7.5	10	μs
Thermal shutdown						
shutdown junction temperature	$T_{j(sd)}$		155	165	180	℃

FUNCTIONAL DESCRIPTION

The CD1040 provides two modes of operation which are selectable via pin STB. See Table 1 for a description of the modes of operation.

Table 4. Operating modes

Mode	PIN STB	PIN RXD	
		LOW	HIGH
Normal	L	bus dominant	bus recessive
Standby	H	wake-up request detected	no wake-up request detected

NORMAL MODE

In this mode the transceiver is able to transmit and receive data via the bus lines CANH and CANL. See Fig.1 for the block diagram. The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD via the multiplexer (MUX). The slope of the output signals on the bus lines is fixed and optimized in a way that lowest ElectroMagnetic Emission (EME) is guaranteed.

STANDBY MODE

In this mode the transmitter and receiver are switched off,and the low-power differential receiver will monitor the bus lines. A HIGH level on pin STB activates this low-power receiver and the wake-up filter, and after t_{BUS} the state of the CAN bus is reflected on pin RXD.
The supply current on VCC is reduced to a minimum in such a way that ElectroMagnetic Immunity (EMI) is guaranteed and a wake-up event on the bus lines will be recognized.
In this mode the bus lines are terminated to ground to reduce the supply current (ICC) to a minimum. A diode is added in series with the high-side driver of RXD to prevent a reverse current from RXD to VCC in the unpowered state. In normal mode this diode is bypassed. This diode is not bypassed in standby mode to reduce current consumption.

Split circuit

Pin SPLIT provides a DC stabilized voltage of 0.5VCC. It is turned on only in normal mode. In standby mode pin SPLIT is floating. The VSPLIT circuit can be used to stabilize the recessive common-mode voltage by connecting pin SPLIT to the centre tap of the split termination (see Fig.4). In case of a recessive bus voltage <0.5VCC due to the presence of an unsupplied transceiver in the network with a significant leakage current from the bus lines to ground, the split circuit will stabilize this recessive voltage to 0.5VCC. So a start of transmission does not cause a step in the common-mode signal which would lead to poor ElectroMagnetic Emission (EME) behaviour.

Wake-up

In the standby mode the bus lines are monitored via a low-power differential comparator. Once the low-power differential comparator has detected a dominant bus level for more than tBUS, pin RXD will become LOW.

Over-temperature detection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature Tj(sd), the output drivers will be disabled until the virtual junction temperature becomes lower than Tj(sd) and TXD becomes recessive again.
By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

TXD dominant time-out function

A ‘TXD dominant time-out’ timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW level on pin TXD exceeds the internal timer value (tdom), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time tdom defines the minimum possible bit rate of 40 kBaud.

Fail-safe features

Pin TXD provides a pull-up towards VCC in order to force a recessive level in case pin TXD is unsupplied.Pin STB provides a pull-up towards VCC in order to force the transceiver into standby mode in case pin STB is unsupplied. In the event that the VCC is lost, pins TXD, STB and RXD will become floating to prevent reverse supplying conditions via these pins.

Typical Application

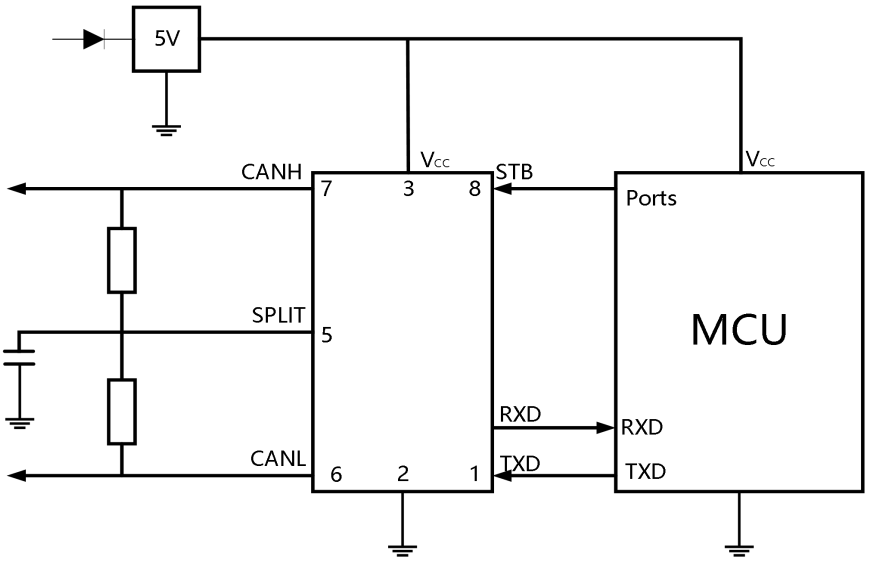


Figure 3. Typical application for 5 V microcontroller

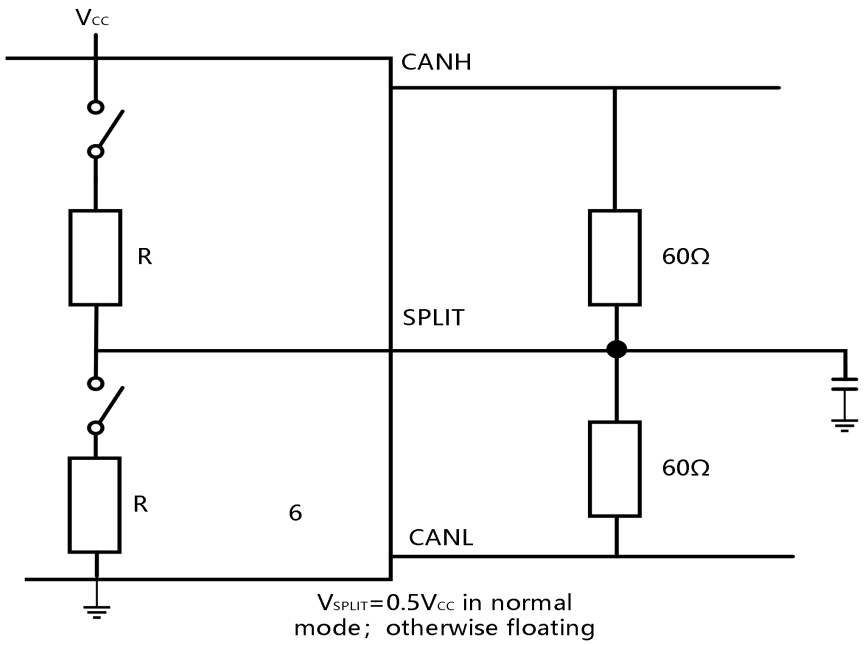
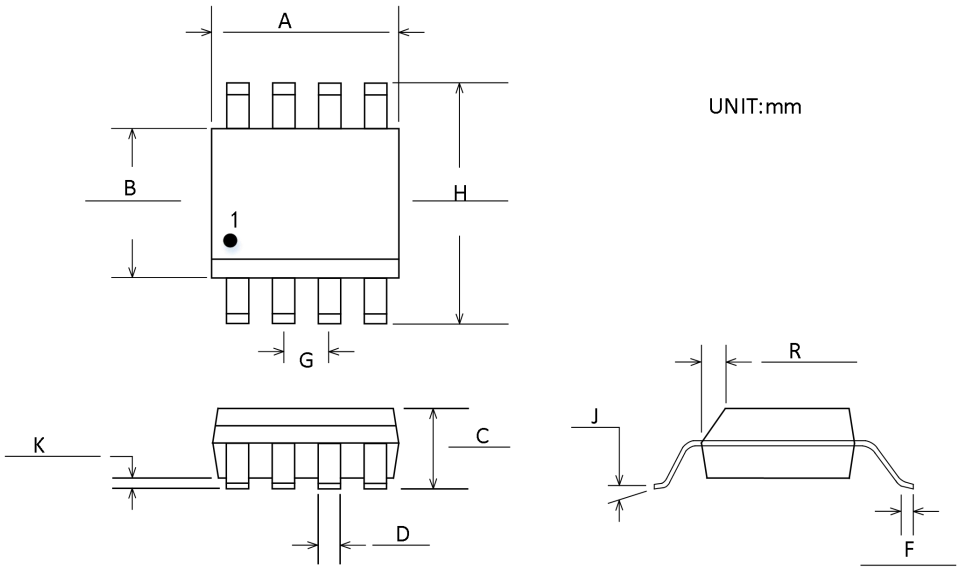


Figure 4. Stabilization circuitry and application

Package Outline Dimensions

SOP-8



Symbol	Dimensions (mm)	
	Min	Max
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.31	0.51
F	0.40	1.27
G	1.27BSC	
H	5.80	6.20
J	0°	8°
K	0.10	0.25
R	0.25	0.50

Figure 5 . 8-Lead Outline Package [SOP-8]

Chinese version:CD1040

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD1040AS8	-40℃~150℃	SOP-8	Tape and Reel, 2500
CD1040AS8	-40℃~150℃	SOP-8	Tape and Reel, 3000
CD1040AS8	-40℃~150℃	SOP-8	Tape and Reel, 4000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.25	Initial version	Regular update	WW	LYL	