CoreadDvices
承芯微电子

CDG711_CDG712_CDG713

Quad, SPST Switches

Version: Rev 1.0.0 Date: 2025-6-18

Features

- 1.8 V to 5.5 V single supply
- Low on resistance (2Ω Typ) at VDD=5.5V
- Low on resistance flatness(0.3Ω Typ)at
- −3 dB bandwidth > 200 MHz
- Rail-to-rail operation
- 16-lead TSSOP and SOP packages
- Fast switching times: tON = 16 ns tOFF = 10
- Typical power consumption: (< 0.01 μW)
- TTL/CMOS compatible

Application

- Cell phones
- Video switching
- Communication systems
- Battery-powered systems
- USB 1.1 signal switching circuits
- Mechanical reed relay replacement

Description

The CDG711, CDG712, and CDG713 are monolithic CMOS devices containing four independently selectable switches. These switches are designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents, and high bandwidth.

They are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Corebai. Fast switching times and high bandwidth make the parts suitable for switching USB 1.1 data signals and video signals.

The CDG711, CDG712, and CDG713 contain four independent single-pole/single-throw (SPST) switches. The CDG711 and CDG712 differ only in that the digital control logic is inverted. The CDG711 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the CDG712. The CDG713 contains two switches whose digital control logic is similar to the CDG711, while the logic is inverted on the other two switches,please refer to the product function block diagram Figure 2 for details.

Each switch conducts equally well in both directions when On. The CDG713 exhibits break-before-make switching action.

The CDG711/CDG712/CDG713 are available in 16-lead TSSOP and 16-lead SOP packages.

Contents

Features ..... - 1 -
Application ..... - 1 -
Description ..... - 1 -
Product Highlights ..... - 3 -
Pin Configurations ..... - 3 -
Functional Block diagram ..... - 4 -
Absolute Maximum Ratings ..... - 5 -
Electrical Characteristics ..... - 5 -
Typical Characteristics ..... - 8 -
Test Circuit ..... - 9 -
Package Outline Dimensions ..... - 10 -
Package/Ordering Information ..... - 11 -
Revision Log ..... - 12 -

Product Highlights

1. 1.8 V to 5.5 V Single-Supply Operation. The CDG711, CDG712, and CDG713 offer high performance and are fully specified and guaranteed with 3V and 5V supply rails.
2. Very Low R_{ON} (4.5Ω maximum at 5 V, 8Ω maximum at 3V). At supply voltage of 1.8V, R_{ON} is typically 35Ω over the temperature range.
3. Low On Resistance Flatness.
4. −3dB Bandwidth >200 MHz.
5. Low Power Dissipation. CMOS construction ensures low power dissipation.
6. Fast t_{ON}/t_{OFF}.
7. Break-Before-Make Switching. This prevents channel shorting when the switches are configured as a multiplexer (CDG713 only).

16-Lead TSSOP and 16-Lead SOP Packages.

Pin Configurations

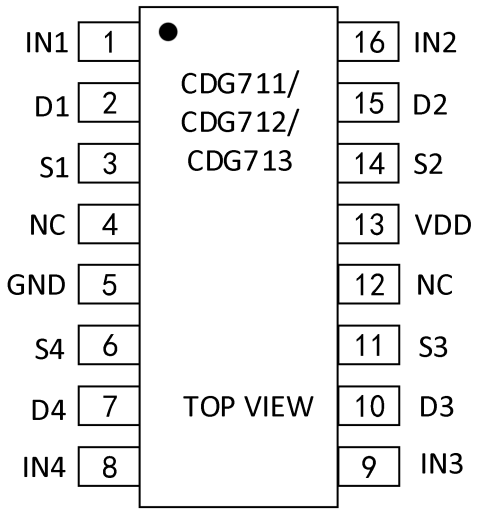


Figure 1. TSSOP16/SOP16 Pin Configuration

Pin description

Pin No.	Pin Name	Description
1	IN1	Digital Control Input. Its logic state controls the status of the Switch S1-D1.
2	D1	Drain Pin. Can be used as input or output.
3	S1	Source Pin. Can be used as input or output.
4	NC	Not internally connected.
5	GND	The most negative power supply pin.
6	S4	Source Pin. Can be used as input or output.
7	D4	Drain Pin. Can be used as input or output.
8	IN4	Digital Control Input. Its logic state controls the status of the Switch S4-D4.
9	IN3	Digital Control Input. Its logic state controls the status of the Switch S3-D3.
10	D3	Drain Pin. Can be used as input or output.
11	S3	Source Pin. Can be used as input or output.
12	NC	Not internally connected.
13	V_{DD}	The most positive power supply pin.
14	S2	Source Pin. Can be used as input or output.
15	D2	Drain Pin. Can be used as input or output.
16	IN2	Digital Control Input. Its logic state controls the status of the Switch S2-D2.

Functional Block diagram

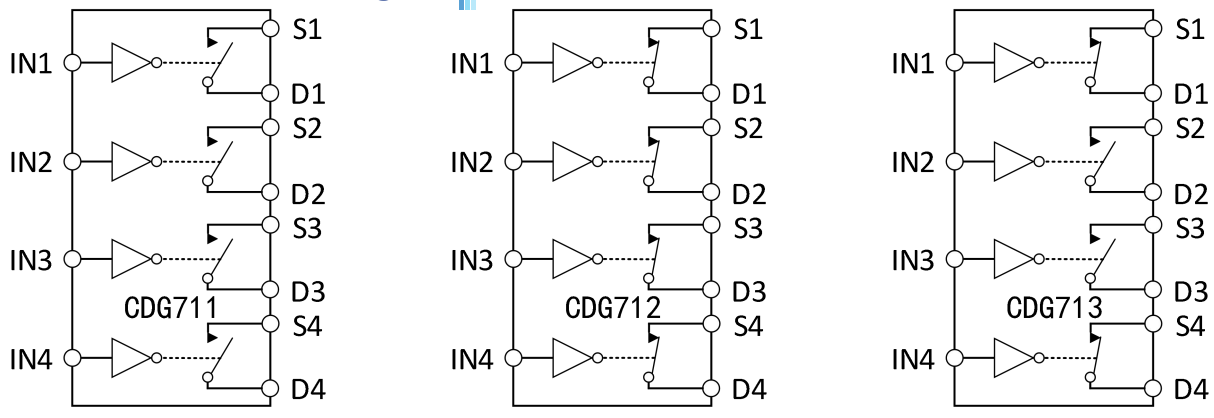


Figure 2. Switches shown for a logic "1" input

Table 2. Truth Table(CDG711/CDG712)

CDG711 In	CDG712 In	Switch Condition
0	1	ON
1	0	OFF

Table 3. Truth Table(CDG713)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs1	−0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA
Continuous Current, S or D	30mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package, Power Dissipation	430mW
θ_{JA} Thermal Impedance	150°C/W
θ_{JC} Thermal Impedance	27°C/W
Lead Temperature, Soldering Vapor Phase(60 sec)	215°C
IR Reflow, Peak Temperature (<20sec)	220°C
ESD	2kV

Electrical Characteristics

VDD = +5 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	2.5	4	--	--	4.5	V_S=0V to V_{DD}, I_S=−10mA;See Figure 6	Ω
On Resistance Match Between Channels (ΔR_{ON})				--	0.05	0.3	V_S=0 V to V_{DD}, I_S=−10mA	Ω
On Resistance Flatness	--	0.5	--	--	--	1.0	V_S=0 V to V_{DD}, I_S=−10mA	Ω

(RFLAT(ON))								
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.2	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 7	nA
Drain Off Leakage ID (Off)	--	± 0.01	±0.1	--	--	±0.2	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 7	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±0.2	V_S=V_D=1V, or 4.5V;See Figure 8	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	11	--	--	--	16	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{OFF}	--	6	--	--	--	10	R_L=300Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D (CDG713 Only)	--	6	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=3V;	ns
Charge Injection	--	3	--				V_S=2V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-58	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-78	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-90	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
Bandwidth −3 dB	--	200	--				R_L=50Ω, C_L=5pF;	MHz
C_S	--	10	--					pF
C_D	--	10	--					pF
C_D, C_S (On)	--	22	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+5.5V, Digital inputs=0V or 5V	μA

VDD = +3 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	5	--	--	5.5	8	V_S=0V to V_{DD}, I_S=−	Ω

							10mA;See Figure 6	
On Resistance Match Between Channels (ΔR_{ON})	--	0.1	--	--	--	--	V_S=0 V to V_{DD}, I_S=−10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	--	--	--	2.5	--	V_S=0 V to V_{DD}, I_S=−10mA	Ω
Leakage Currents							V_{DD}=+3.3V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.2	V_S=3V/1V, V_D=1V/3V;See Figure 7	nA
Drain Off Leakage ID (Off)	--	± 0.01	±0.1	--	--	±0.2	V_S=3V/1V, V_D=1V/3V;See Figure 7	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±0.2	V_S=V_D=1V, or 3V;See Figure 8	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.0	--	--		V
Input Low Voltage, V_{INL}				--	--	0.4		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	13	--	--	--	20	R_L=300Ω,C_L=35pF,V_S=2V	ns
t_{OFF}	--	7	--	--	--	12	R_L=300Ω,C_L=35pF,V_S=2V	ns
Break-Before-Make Time Delay, t_D (CDG713 Only)	--	7	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=2V;	ns
Charge Injection	--	3	--				V_S=1.5V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-58	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-78	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-90	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
Bandwidth −3 dB	--	200	--				R_L=50Ω, C_L=5pF;	MHz
C_S	--	10	--					pF
C_D	--	10	--					pF
C_D, C_S (On)	--	22	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+3.3V, Digital inputs=0V or 3V	μA

Typical Characteristics

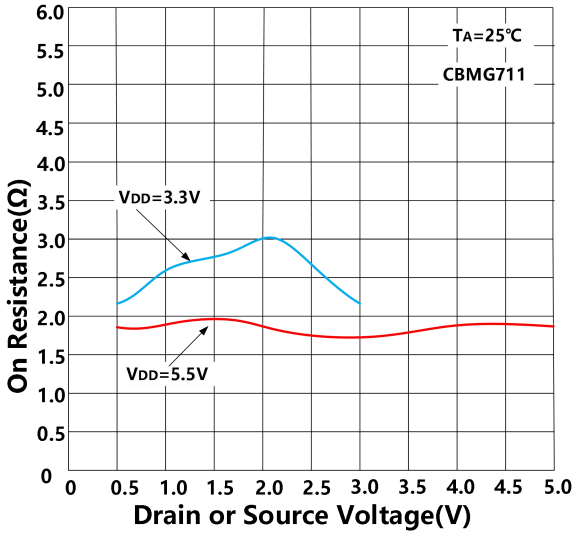


Figure 3.On Resistance vs. V_D (V_S)-(CDG711)

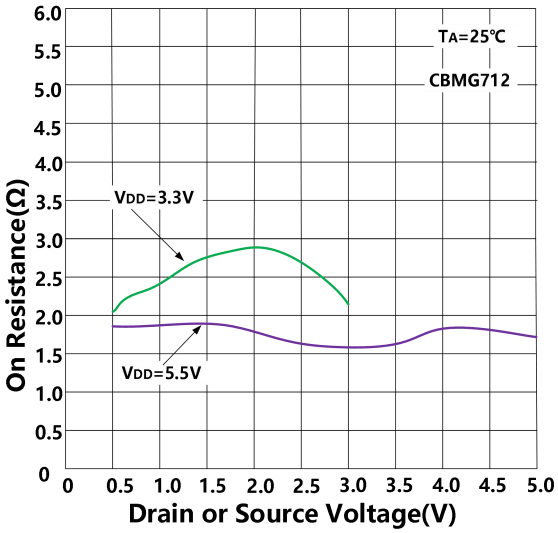


Figure 4.On Resistance vs. V_D (V_S)-(CDG712)

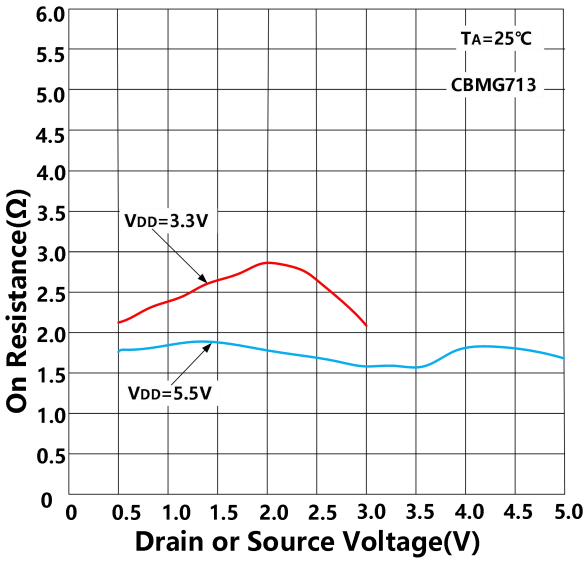
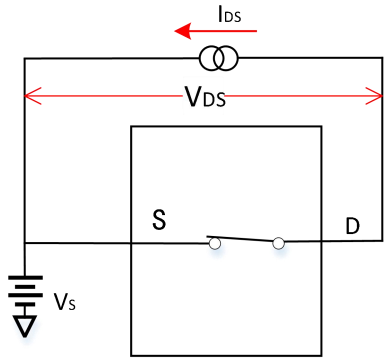


Figure 5.On Resistance vs. V_D (V_S)-(CDG713)

Chinese version:CDG711_CDG712_CDG713

Test Circuit



RON=V_{DS}/I_{DS}

Figure 6. On Resistance

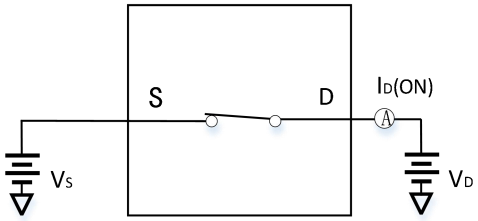


Figure 7. On Leakage

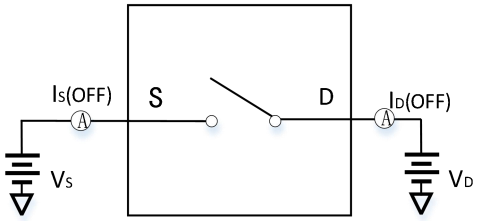


Figure 8. Off Leakage

Chinese version:CDG711_CDG712_CDG713

Package Outline Dimensions

TSSOP-16

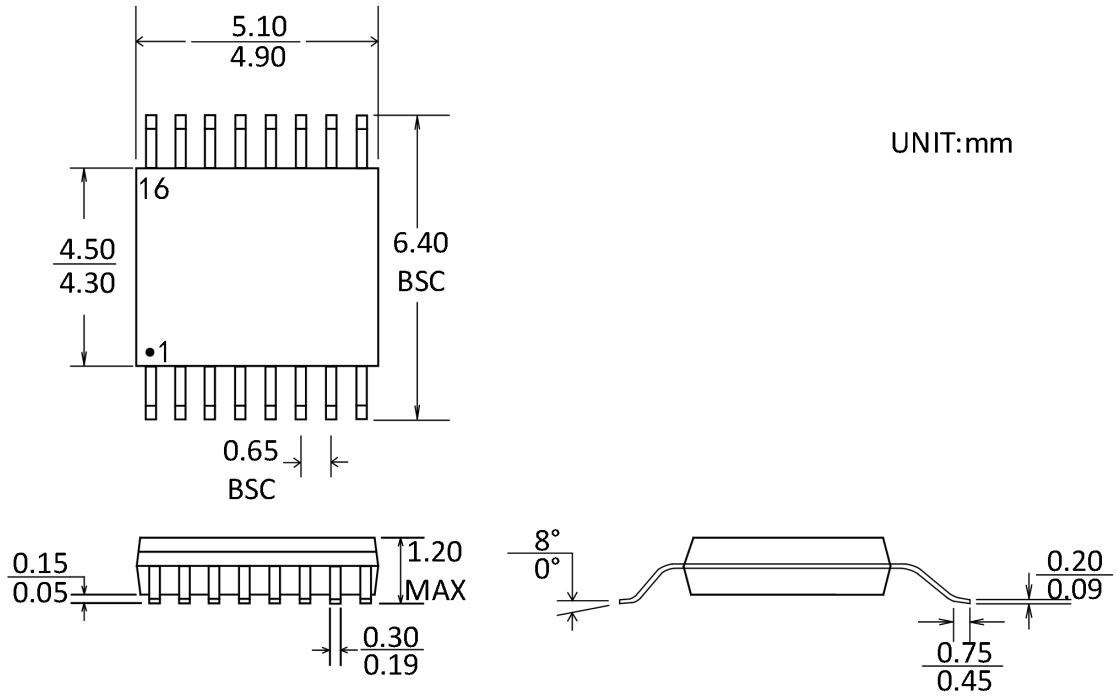


Figure 9. 16-Lead Thin Shrink Small Outline Package [TSSOP]

SOP-16

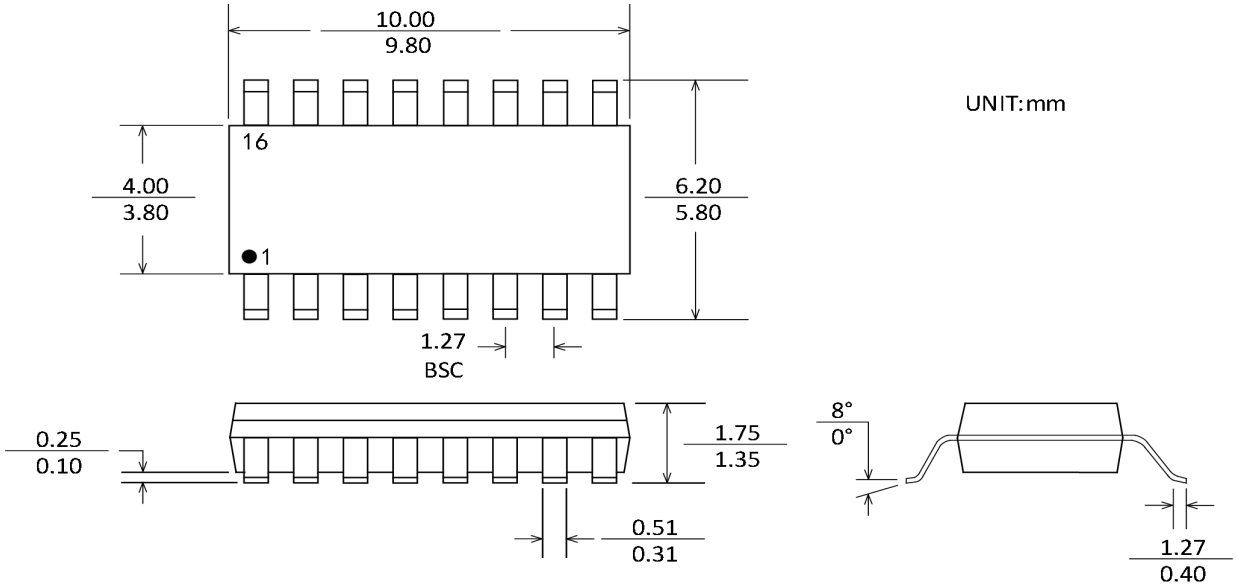


Figure 10. 16-Lead Standard Small Outline Package [SOP]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDG711AS16	-40℃~85℃	SOP-16	Tape and Reel, 2500
CDG711ATS16	-40℃~85℃	TSSOP-16	Tape and Reel, 2500
CDG712AS16	-40℃~85℃	SOP-16	Tape and Reel, 2500
CDG712ATS16	-40℃~85℃	TSSOP-16	Tape and Reel, 2500
CDG713AS16	-40℃~85℃	SOP-16	Tape and Reel, 2500
CDG713ATS16	-40℃~85℃	TSSOP-16	Tape and Reel, 2500

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.18	Initial version	Regular update	WW	LYL	