CoreadDvices
承芯微电子

CDG714_CDG715

Serially Controlled, Octal SPST Switches

Version: Rev 1.0.0 Date: 2025-6-18

Features

- SPI/QSPI/MICROWIRE-compatible interface
- CDG715: I 2C-compatible interface (CDG715)
- 2.7 V to 5.5 V single supply
- ±2.5 V dual supply
- 2.5 Ω on resistance
- 0.6 Ω on resistance flatness
- 0.1 nA leakage currents
- Octal SPST
- Power-on reset
- Fast switching times
- TTL/CMOS compatible
- 24-lead TSSOP

Application

- Data acquisition systems
- Communication systems
- Relay replacement
- Audio and video switching

Description

The CDG714/CDG715 are complementary metal-oxide semiconductor (CMOS), octal single-pole, single-throw (SPST) switches, controlled via either a 2- or 3-wire serial interface. On resistance is closely matched between the switches and is flat over the full signal range. Each switch conducts equally well in both directions, and the input signal range extends to the supplies. Data is written to these devices in the form of 8 bits, each bit corresponding to one channel.

The CDG714 uses a 3-wire serial interface that is compatible with serial peripheral interface (SPI), QSPI™, MICROWIRE™ interface standards, and most digital signal processing (DSP) interface standards. The output of the shift register DOUT enables a number of these devices to be daisy-chained.

The CDG715 uses a 2-wire serial interface that is compatible with the I 2 C interface standard. The CDG715 has four hardwired and the CDG715 is available in a 24-lead TSSOP. addresses, selectable from two external address pins (A0 and A1). The pins allow the two LSBs of the 7-bit slave address to be set by the user. A maximum of four of these devices may be connected to the bus. On power-up of these devices, all switches are in the off condition, and the internal registers contain all zeros.

A low power consumption and operating supply range of 2.7 V to 5.5 V make these devices ideal

for many applications. These devices can also be supplied from a dual ±2.5 V supply. The CDG714,CDG715 are available in a 24-lead TSSOP.

Contents

Product Highlights

1. 2- or 3-wire serial interface.

2. Single-/dual-supply operation. The CDG714 and CDG715 are fully specified and guaranteed with 3 V, 5 V, and ±2.5 V supply rails.

3. Low on resistance, typically 2.5 Ω.

4. Low leakage.

5. Power-on reset.

6. A 24-lead TSSOP for both the CDG714 and the CDG715 .

Pin Configurations

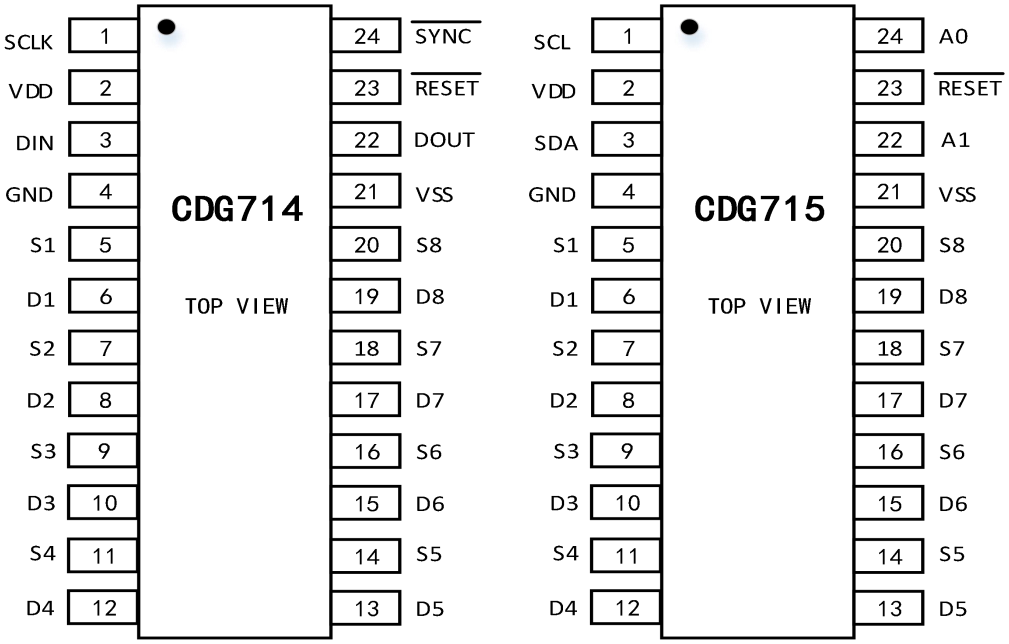


Figure 1. TSSOP24 Pin Configuration

Pin description

CDG714

Pin No.	Pin Name	Description
1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices accommodate serial input rates of up to 30 MHz.
2	V_{DD}	Positive Analog Supply Voltage
3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4	GND	Ground (0 V) Reference.
5,7,9,11,14,16,18,20	Sx	Source. These pins may be an input or an output.
6,8,10,12,13,15,17,19	Dx	Drain. These pins may be an input or an output.
21	V_{SS}	Negative Analog Supply Voltage. For single-supply operation, tie this pin to ground.
22	DOUT	Serial Data Output. This pin allows a number of devices to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. DOUT is an open-drain output that is pulled to the supply with an external pull-up resistor.
23	RESET	Active Low Control Input. This pin clears the input register and turns all switches to the off condition.
24	SYNC	Active Low Control Input. This pin is the frame synchronization signal for the input data. When SYNC goes low, this pin powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clock cycle. Taking SYNC high updates the switches.

CDG715

Pin No.	Pin Name	Description
1	SCL	Serial Clock Line. This pin is used in conjunction with the SDA line to clock data into the 8-bit input shift register. Clock rates of up to 400 kbps are accommodated with this 2-wire serial interface.
2	VDD	Positive Analog Supply Voltage
3	SDA	Serial Data Line. This pin is used in conjunction with the SCL line to clock data into the 8-bit input shift register during the write cycle and used to read back one byte of data during the read cycle. SDA is a bidirectional open-drain data line that is pulled to the supply with an external pull-up resistor
4	GND	Ground (0 V) Reference.

5,7,9,11,14,16,18,20	Sx	Source. These pins may be an input or an output.
6,8,10,12,13,15,17,19	Dx	Drain. These pins may be an input or an output.
21	VSS	Negative Analog Supply Voltage. For single-supply operation, tie this pin to ground.
22	A1	Address Input. This pin sets the second LSB of the 7-bit slave address.
23	RESET	Active Low Control Input. This pin clears the input register and turns all switches to the off condition.
24	A0	Address Input. This pin sets the LSB of the 7-bit slave address.

Functional Block diagram

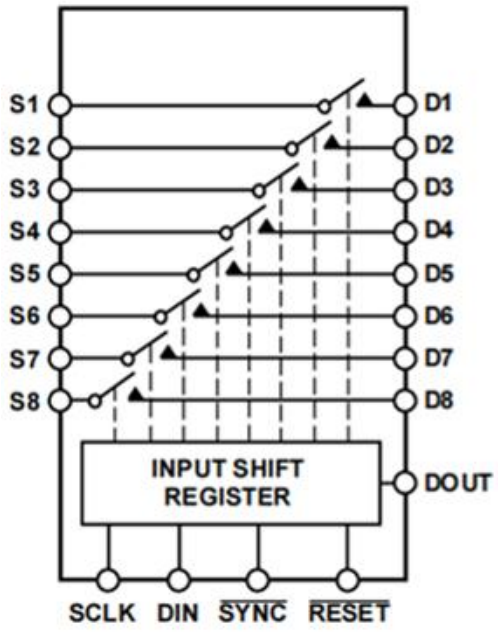


Figure 2. CDG714

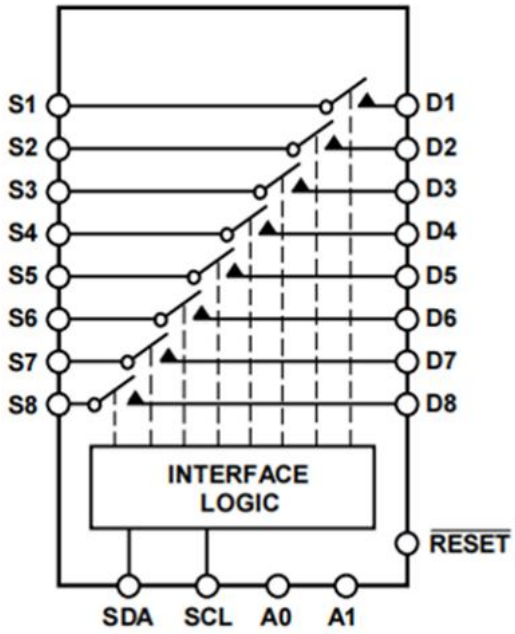


Figure 3. CDG715

Absolute Maximum Ratings

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs1	−0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA
Continuous Current, S or D	30mA
Operating Temperature Range	−40°C to +85°C

Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	150°C/W
Lead Temperature, Soldering Vapor Phase(60 sec)	300°C
IR Reflow, Peak Temperature (<20sec)	235°C
ESD	2kV

Electrical Characteristics

VDD = +5 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	2.5	4.5	--	--	5	V_S=0V to V_{DD}, I_S=10mA;See Figure 6	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	0.4	0.8	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	0.6	--	--	--	1.2	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=1V/4.5V, V_D=4.5V/1V;See Figure 8	nA
Drain Off Leakage I_D (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=1V/4.5V, V_D=4.5V/1V;See Figure 8	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±0.3	V_S=V_D=1V, or 4.5V;See Figure 7	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Digital Input Capacitance, C_{IN}	--	3	--	--	--	--		pF
DIGITAL OUTPUT, CDG714,DOUT								

Output Voltage Low, V_{OL}	--	--	--	--	--	0.4	I_{SINK} = 6 mA	V
Digital Output Capacitance, C_{OUT}	--	4	--	--	--	--		pF
DIGITAL INPUTS, SCL, SDA								
Input Voltage High, V_{INH}	--	--	--	0.7*V_{DD}		V_{DD}+0.3	V_{IN} = 0 V to V_{DD}	
Input Voltage High, V_{INL}	--	--	--	-0.3		0.3*V_{DD}		
Input Leakage Current, I_{IN}	--	0.005V	--	--	--	--		
Input Hysteresis, VHYST	0.05*VDD	--	--	--	--	--		
Input Capacitance, CIN	--	6	--	--	--	--		
Dynamic Characteristics								
t_{on}(CDG714)	--	20	--	--	--	32	R_L=300 Ω,C_L=35pF,V_S=3V	ns
t_{on}(CDG715)	--	95	--	--	--	140	R_L=300 Ω,C_L=35pF,V_S=3V	ns
t_{OFF}(CDG714)	--	8	--	--	--	15	R_L=300 Ω,C_L=35pF,V_S=3V	ns
t_{OFF}(CDG715)	--	85	--	--	--	130	R_L=300 Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D	--	8	--	1	--	--	R_L=30 Ω,C_L=35pF,V_S=3V;	ns
Charge Injection,Q_{INJ}	--	±3	--				V_S=2V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-60	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-80	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-70	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
	--	-90	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB
Bandwidth −3 dB	--	155	--				R_L=50Ω, C_L=5pF;	MHz
Insertion Loss	--	-0.3	--					
C_S	--	11	--					pF
C_D	--	11	--					pF
C_D, C_S (On)	--	22	--					pF
Power Requirements								

I_{DD}	--	10	--	--	--	20	V_{DD}=+5.5V, Digital inputs=0V or 5V	μA

VDD = +3 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	6	11	--	--	12	V_S=0V to V_{DD}, I_S=10mA;See Figure 6	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	0.4	1.2	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	--	--	--	3.5	--	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+3.3V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=1V/3V, V_D=3V/1V;See Figure 8	nA
Drain Off Leakage I_D (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=1V/3V, V_D=3V/1V;See Figure 8	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±0.3	V_S=V_D=1V, or 3V;See Figure 7	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.0	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Digital Input Capacitance, C_{IN}	--	3	--	--	--	--		pF
DIGITAL OUTPUT, CDG714,DOUT								
Output Voltage Low, V_{OL}	--	--	--	--	--	0.4	I_{SINK} = 6 mA	V
Digital Output Capacitance, C_{OUT}	--	4	--	--	--	--		pF
DIGITAL INPUTS, SCL, SDA								
Input Voltage High, V_{INH}	--	--	--	0.7*V_{DD}		V_{DD}+0.3	V_{IN} = 0 V to V_{DD}	
Input Voltage High, V_{INL}	--	--	--	-0.3		0.3*V_{DD}		

Input Leakage Current, I_{IN}	--	0.005V	--	--	--	±1		
Input Hysteresis, V_{HYST}	0.05*VDD	--	--	--	--	--		
Input Capacitance, C_{IN}	--	6	--	--	--	--		
LOGIC OUTPUT, (SDA)								
Output Voltage Low, V_{OL}	--	--	--	--	--	0.4	I_{SINK} = 3 mA	
	--	--	--	--	--	0.6	I_{SINK} = 6 mA	
Dynamic Characteristics								
t_{on}(CDG714)	--	35	--	--	--	65	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{on}(CDG715)	--	130	--	--	--	200	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{OFF}(CDG714)	--	11	--	--	--	20	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{OFF}(CDG715)	--	115	--	--	--	180	R_L=300Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D	--	8	--	1	--	--	R_L=30Ω,C_L=35pF,V_S=3V;	ns
Charge Injection,Q_{INJ}	--	±2	--				V_S=2V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-60	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-80	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-70	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
	--	-90	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB
Bandwidth −3 dB	--	155	--				R_L=50Ω, C_L=5pF;	MHz
Insertion Loss	--	-0.4	--					
C_S	--	11	--					pF
C_D	--	11	--					pF
C_D, C_S (On)	--	22	--					pF
Power Requirements								
I_{DD}	--	10	--	--	--	20	V_{DD}=+3.3V, Digital inputs=0V or 3.3V	μA

Typical Characteristics

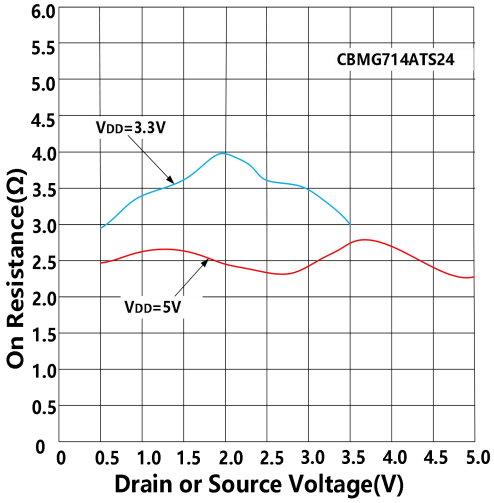


Figure 4.On Resistance vs. V_D (V_S)-(CDG714)

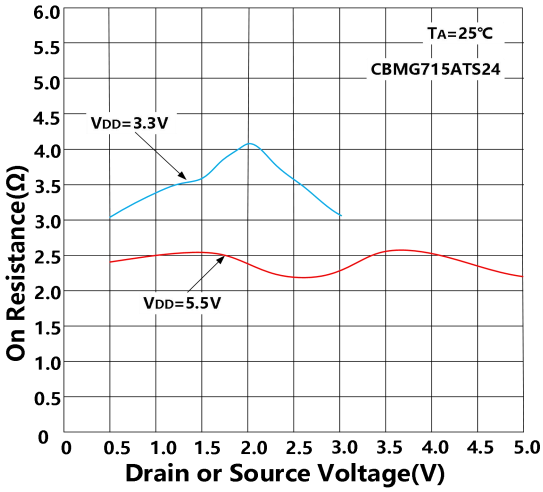
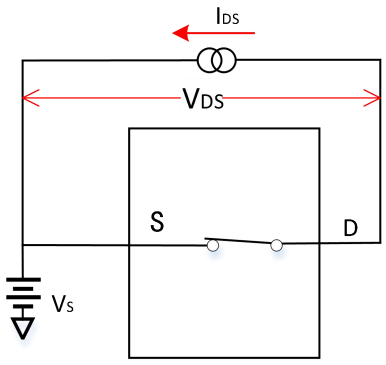


Figure 5.On Resistance vs. V_D (V_S)-(CDG715)

Test Circuit



RON=V_{DS}/I_{DS}

Figure 6. On Resistance

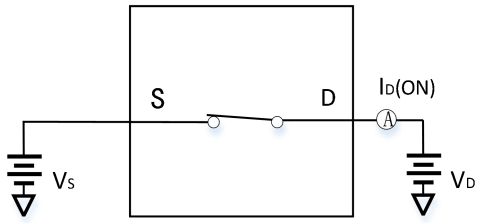


Figure 7. On Leakage

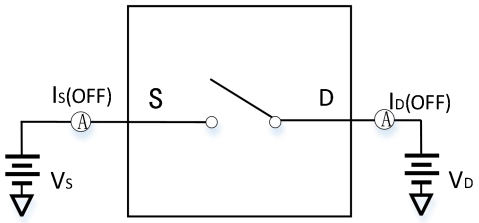


Figure 8. Off Leakage

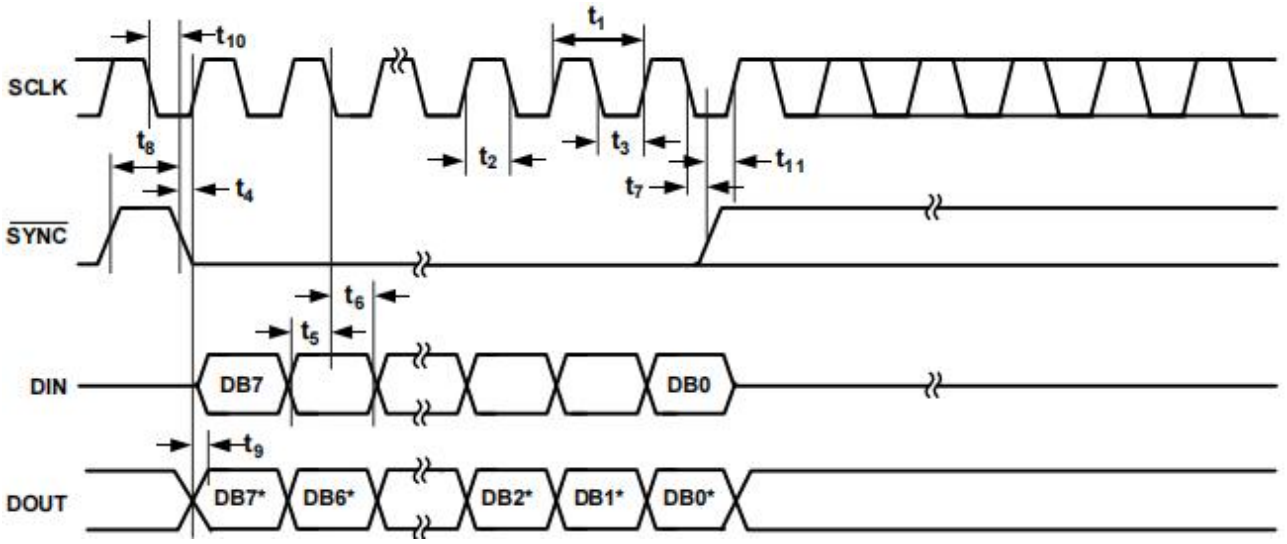


Figure 9. 3-Wire Serial Interface Timing Diagram

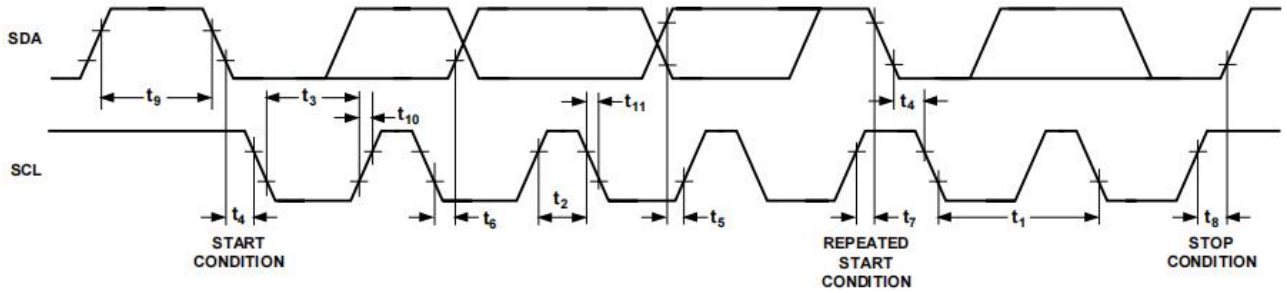


Figure 10. 2-Wire Serial Interface Timing Diagram

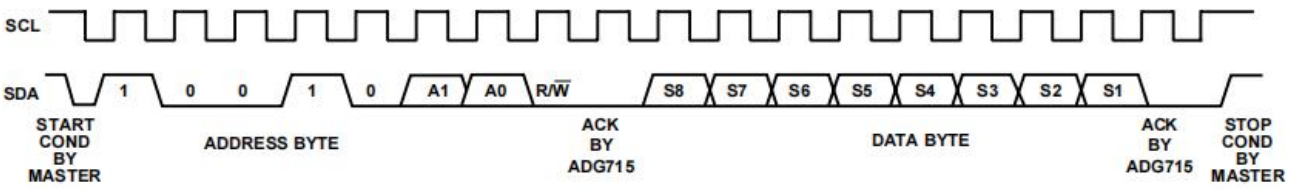


Figure 11. CDG715 Write Sequence

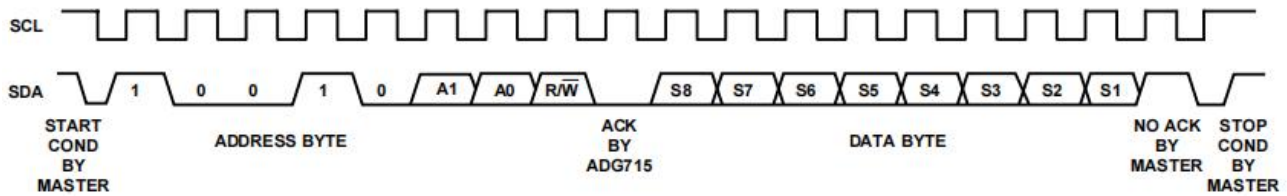


Figure 12. CDG715 Readback Sequence

Package Outline Dimensions

TSSOP-24

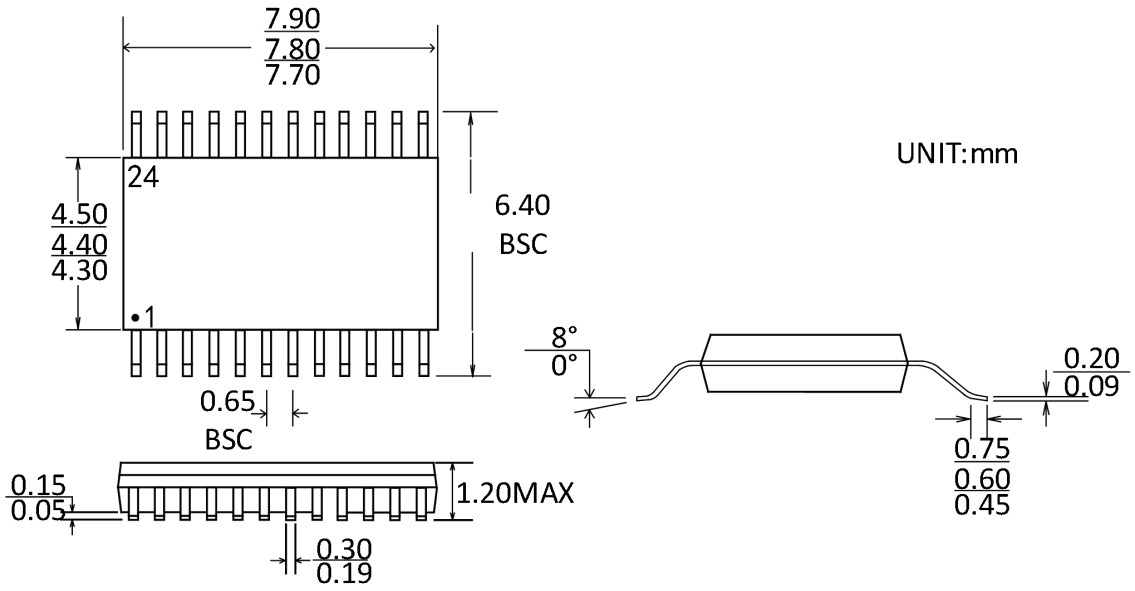


Figure 11. 24-Lead Outline Package [TSSOP]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDG714ATS24	-40℃~85℃	TSSOP-24	Tape and Reel, 3000
CDG715ATS24	-40℃~85℃	TSSOP-24	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.18	Initial version	Regular update	WW	LYL	