CoreadDvices
承芯微电子

CDG721_CDG722_CDG723

Dual, SPST Switches

Version: Rev 1.0.0 Date: 2025-6-18

Features

- 1.8 V to 5.5 V single supply
- Low on resistance (3Ω Max),at VDD=5.5V
- Low on resistance flatness
- −3 dB bandwidth > 200 MHz
- 8-lead MSOP and QFN8 packages
- Fast switching times: t_{ON} = 20 ns t_{OFF} = 10 ns
- Typical power consumption: (< 0.1 μW)
- TTL/CMOS compatible

Application

- Cell phones
- Video switching
- Sample hold systems
- Audio signal routing
- Communication systems
- Battery-powered systems
- USB 1.1 signal switching circuits
- Mechanical reed relay replacement

Description

The CDG721, CDG722, and CDG723 are monolithic CMOS SPST switches. These switches are designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage currents. The devices are packaged in both a tiny 3 mm × 2 mm LFCSP and an MSOP, making them ideal for space-constrained applications.

The CDG721, CDG722, and CDG723 are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices, Inc. The CDG721, CDG722, and CDG723 contain two independent single-pole/single-throw (SPST) switches.

The CDG721 and CDG722 differ only in that both switches are normally open and normally closed, respectively. In the CDG723, Switch 1 is normally open and Switch 2 is normally closed. Each switch of the CDG721, CDG722, and CDG723 conducts equally well in both directions when on. The CDG723 exhibits break-before-make switching action.

Chinese version:CDG721_CDG722_CDG723

Contents

Product Highlights

1. 1.8 V to 5.5 V single-supply operation.

2. Very low R_{ON} (3Ω max at V_{DD}= 5V, 5Ω max at V_{DD}= 3V).

3. Low on resistance flatness.

4. −3dB bandwidth >200 MHz.

5. Low power dissipation. CMOS construction ensures low power dissipation.

6. 8-lead MSOP, QFN-8 Package

Pin Configurations

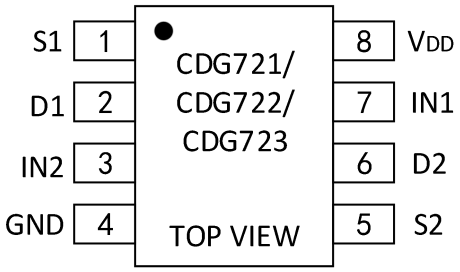


Figure 1. MSOP8 Pin Configuration

Pin description

Pin No.	Pin Name	Description
1	S1	Source Pin 1. May be an input or an output.
2	D1	Drain Pin 1. May be an input or an output.
3	IN2	Logic Control Input for Switch S2→D2.
4	GND	Ground (0 V) Reference.
5	S2	Source Pin 2. May be an input or an output.
6	D2	Drain Pin 2. May be an input or an output.
7	IN1	Logic Control Input for Switch S1→D1.
8	V_{DD}	Positive Power Supply Input.

Functional Block diagram

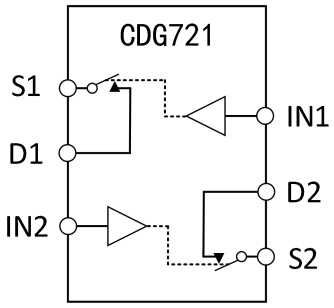


Figure 2. CDG721

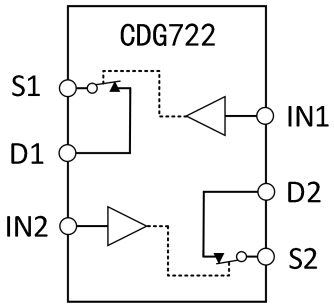


Figure 3. CDG721

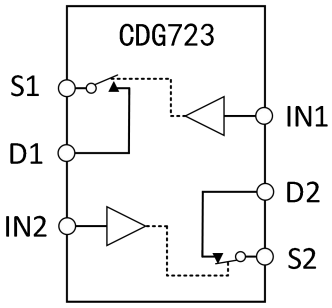


Figure 4. CDG723

Figure 2. Switches shown for a logic "1" input

Truth Table(CDG721/CDG722)

CDG711 In	CDG712 In	Switch Condition
0	1	OFF
1	0	ON

Truth Table(CDG723)

Logic	Switch 1	Switch 2
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs1	−0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA
Continuous Current, S or D	30mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP Package	
θ_{JA} Thermal Impedance	206°C/W
Lead Temperature, Soldering Vapor Phase(60 sec)	215°C
IR Reflow, Peak Temperature (<20sec)	220°C

ESD	2kV

Electrical Characteristics

VDD = +5 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			-40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	2	4	--	--	5	V_S=0V to V_{DD}, I_S=−10mA;See Figure 8	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	0.3	--	--	--	1.0	V_S=0 V to V_{DD}, I_S=−10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	0.5	--	--	--	1.5	V_S=0 V to V_{DD}, I_S=−10mA	Ω
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	--	--	--	--	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 10	nA
Drain Off Leakage ID (Off)	--	± 0.01	--	--	--	--	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 10	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	--	--	--	--	V_S=V_D=1V, or 4.5V;See Figure 9	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	14	--	--	--	20	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{OFF}	--	6	--	--	--	10	R_L=300Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D (CDG723 Only)	--	7	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=3V;	ns
Charge Injection	--	2	--				V_S=2V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-60	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-80	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-77	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB

	--	-97	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB
Bandwidth −3 dB	--	200	--				R_L=50Ω, C_L=5pF;	MHz
C_S	--	7	--					pF
C_D	--	7	--					pF
C_D, C_S (On)	--	18	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+5.5V, Digital inputs=0V or 5V	μA

VDD = +3 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25℃			-40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	3.5	7	--	--	10	V_S=0V to V_{DD}, I_S=−10mA;See Figure 8	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	0.3	--	--	--	1.0	V_S=0 V to V_{DD}, I_S=−10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	1.5	--	--	--	--	V_S=0 V to V_{DD}, I_S=−10mA	Ω
Leakage Currents							V_{DD}=+3.3V	
Source Off Leakage I_S (Off)	--	± 0.01	--	--	--	--	V_S=3V/1V, V_D=1V/3V;See Figure 10	nA
Drain Off Leakage ID (Off)	--	± 0.01	--	--	--	--	V_S=3V/1V, V_D=1V/3V;See Figure 10	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	--	--	--	--	V_S=V_D=1V, or 3V;See Figure 9	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.0	--	--		V
Input Low Voltage, V_{INL}				--	--	0.4		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	16	--	--	--	24	R_L=300Ω,C_L=35pF,V_S=2V	ns
t_{OFF}	--	7	--	--	--	11	R_L=300Ω,C_L=35pF,V_S=2V	ns
Break-Before-Make Time Delay, t_D (CDG713 Only)	--	7	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=2V	ns
Charge Injection	--	2	--				V_S=1.5V; R_S=0Ω, C_L=1nF	pC

Off Isolation	--	-60	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-80	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-77	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-97	--				R_L=50Ω, C_L=5pF, f=1MHz	
Bandwidth −3 dB	--	200	--				R_L=50Ω, C_L=5pF	MHz
C_S	--	7	--					pF
C_D	--	7	--					pF
C_D, C_S (On)	--	18	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+3.3V, Digital inputs=0V or 3V	μA

Typical Characteristics

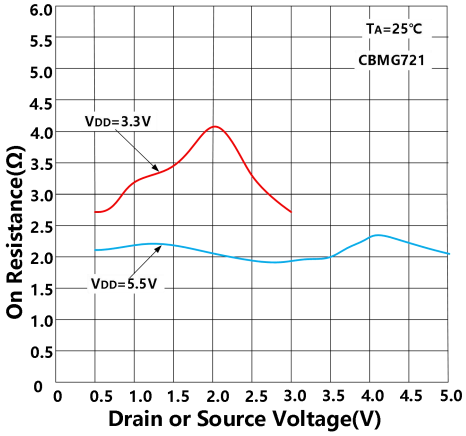


Figure 5.On Resistance vs. V_D (V_S)-(CDG721)

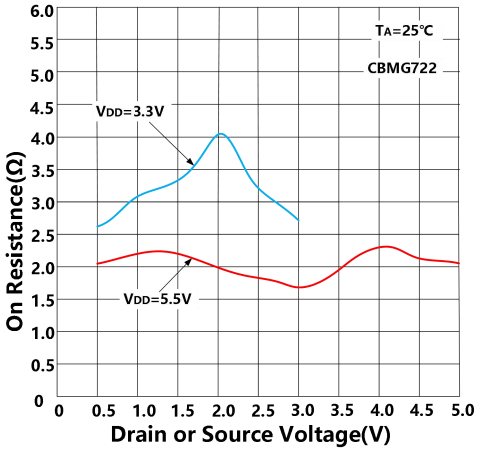


Figure 6.On Resistance vs. V_D (V_S)-(CDG722)

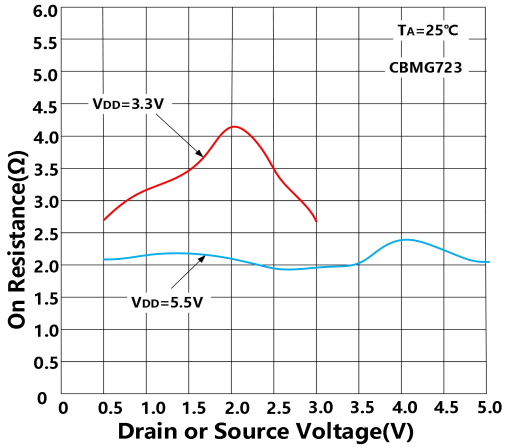
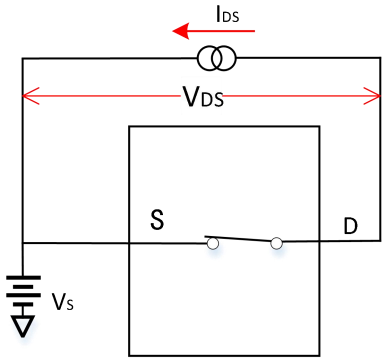


Figure 7.On Resistance vs. V_D (V_S)-(CDG723)

Test Circuit



RON=V_{DS}/I_{DS}

Figure 8. On Resistance

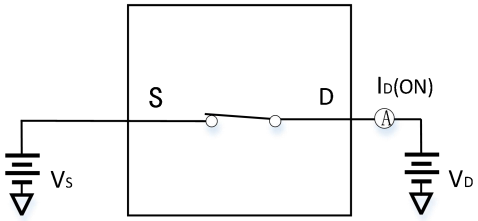


Figure 9. On Leakage

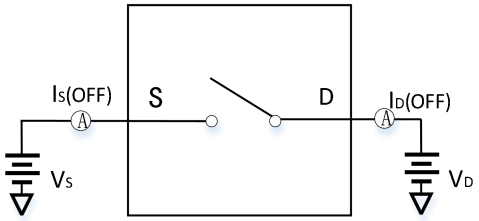


Figure 10. Off Leakage

Chinese version:CDG721_CDG722_CDG723

Package Outline Dimensions

MSOP-8

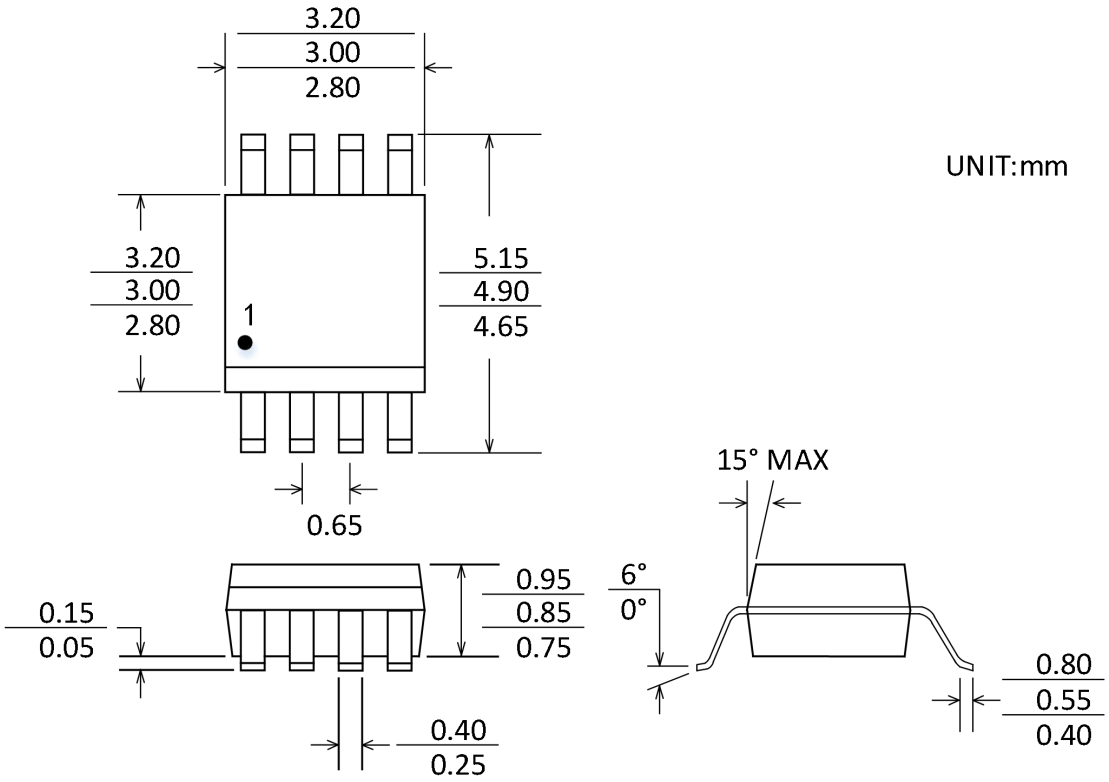


Figure 11. 8-Lead Mini Small Outline Package [MSOP]

Chinese version:CDG721_CDG722_CDG723

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDG721AMS8	-40℃~85℃	MSOP-8	Tape and Reel, 3000
CDG722AMS8	-40℃~85℃	MSOP-8	Tape and Reel, 3000
CDG723AMS8	-40℃~85℃	MSOP-8	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.18	Initial version	Regular update	WW	LYL	