CoreadDvices
承芯微电子

CDG726_CDG732

16/32 Channel Analog Multiplexers

Version: Rev 1.0.0 Date: 2025-6-18

Features

- 1.8 V to 5.5 V single-supply operation
- ±2.5 V dual-supply operation
- On resistance: 3.5 Ω at 25°C (+5 V single
- 0.5 Ω on-resistance flatness at 25°C (+5 V
- Rail-to-rail operation
- Transition times: 23 ns typical at 25°C
- Single 32-to-1 channel multiplexer
- Dual/differential 16-to-1 channel multiplexer
- 48-lead TQFP

Application

- Relay replacement
- Optical applications
- Data acquisition systems
- Communication systems
- Battery-powered systems
- Audio and video switching
- Medical instrumentation
- Automatic test equipment (ATE)

Description

The CDG726/CDG732 are monolithic, complementary metal oxide semiconductor (CMOS) 32-channel and dual 16-channel analog multiplexers. The CDG732 switches one of 32 inputs (S1 to S32) to a common output, D, as determined by the 5-bit binary address lines A0, A1, A2, A3, and A4. The CDG726 switches one of 16 inputs as determined by the 4-bit binary address lines A0, A1, A2, and A3. On-chip latches facilitate microprocessor interfacing. The CDG726 may also be configured for differential operation by tying $\overline{CSA}$ and $\overline{CSB}$ together. An $\overline{EN}$ input is used to enable or disable the devices. When disabled, all channels are switched off. These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, and leakage currents. They operate from a single supply of +1.8 V to +5.5 V and a ±2.5 V dual supply, making them ideally suited to a variety of applications. On resistance is in the region of a few ohms and is closely matched between switches and very flat over the full signal range. These devices can operate equally well as either multiplexers or demultiplexers and have an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. The CDG726/CDG732 are available in a 48- lead TQFP. For functionally equivalent devices with serial interface.

Contents

Product Highlights

1. +1.8 V to +5.5 V single- or ±2.5 V dual-supply operation. These devices are specified and guaranteed with +5 V ± 10%, +3 V ± 10% single-supply, and ±2.5 V ± 10% dual-supply rails.
2. An on resistance of 3.5 Ω.
3. Guaranteed break-before-make switching action.
4. 48-lead TQFP package.

Pin Configurations

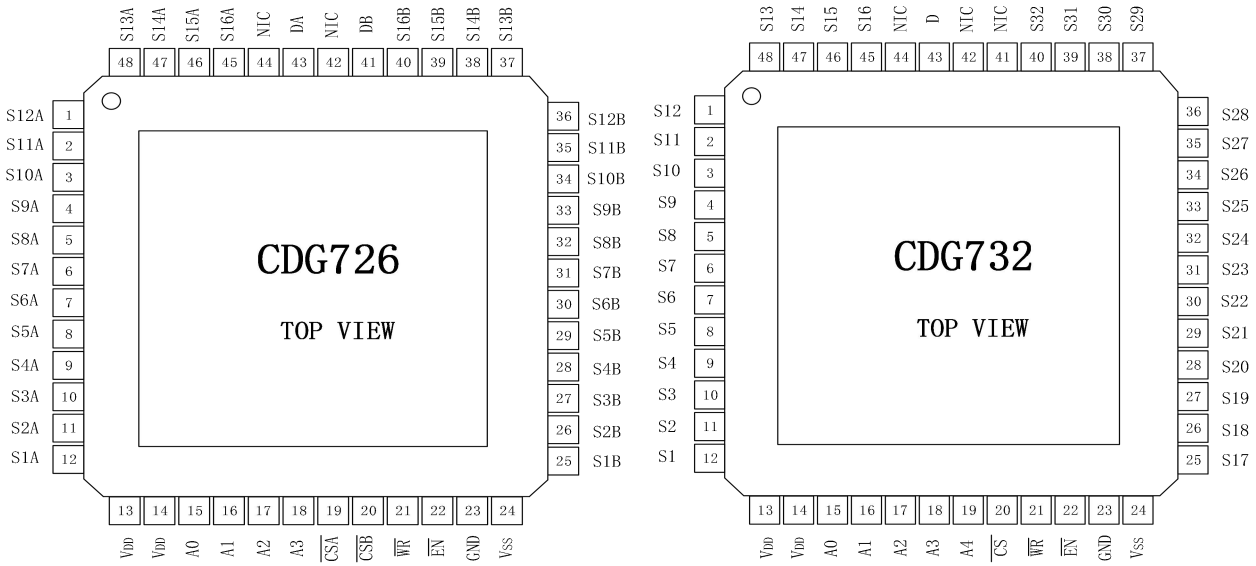


Figure 1. TQFP-48 Pin Configuration

CDG726 Pin Function Description

Pin No.	Pin Name	Description
1 to 12, 45 to 48	S16A to S1A	Source Terminal. This pin may be an input or output.
13, 14	V_{DD}	Most Positive Power Supply Potential.
15 to 18	A0 to A3	Logic Control Inputs.

19	$\overline{CSA}$	Chip Select Pin A. $\overline{CSA}$ is active low. If a differential output configuration is required, tie $\overline{CSA}$ and $\overline{CSB}$ together.
20	$\overline{CSB}$	Chip Select Pin B. $\overline{CSB}$ is active low. If a differential output configuration is required, tie $\overline{CSB}$ and $\overline{CSA}$ together.
21	$\overline{WR}$	Write pin. When $\overline{WR}$ is low, the logic control inputs (A0 to A3) control which state the switches are in. On the rising edge of $\overline{WR}$, the logic control input data is latched.
22	$\overline{EN}$	Active Low, Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, the Ax logic control inputs determine the on switches. The EN input signal is not latched by $\overline{WR}$.
23	GND	Ground (0 V) Reference.
24	V_{SS}	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect this pin to GND.
25 to 40	S1B to S16B	Source Terminal. This pin may be an input or output.
41	DB	Drain Terminal. This pin may be an input or output.
42, 44	NIC	Not Internally Connected. Do not connect to this pin.
43	DA	Drain Terminal. This pin may be an input or output.

CDG732 Pin Function Description

Pin No.	Pin Name	Description
1 to 12, 45 to 48	S16 to S1	Source Terminal. This pin may be an input or output.
13, 14	VDD	Most Positive Power Supply Potential.
15 to 19	A0 to A4	Logic Control Inputs.
20	$\overline{CS}$	Chip Select Pin. $\overline{CS}$ is active low.
21	$\overline{WR}$	Write Pin. When $\overline{WR}$ is low, the logic control inputs (A0 to A4) control which state the switches are in. On the rising edge of $\overline{WR}$, the logic control input data is latched.
22	$\overline{EN}$	Active Low, Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, the Ax logic control inputs

		determine the on switches. The $\overline{EN}$ input signal is not latched by $\overline{WR}$.
23	GND	Ground (0 V) Reference.
24	VSS	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, connect this pin to GND.
25 to 40	S17 to S32	Source Terminal. This pin may be an input or output.
41, 42, 44	NIC	Not Internally Connected. Do not connect to this pin.
43	D	Drain Terminal. This pin may be an input or output.

Functional Block diagram

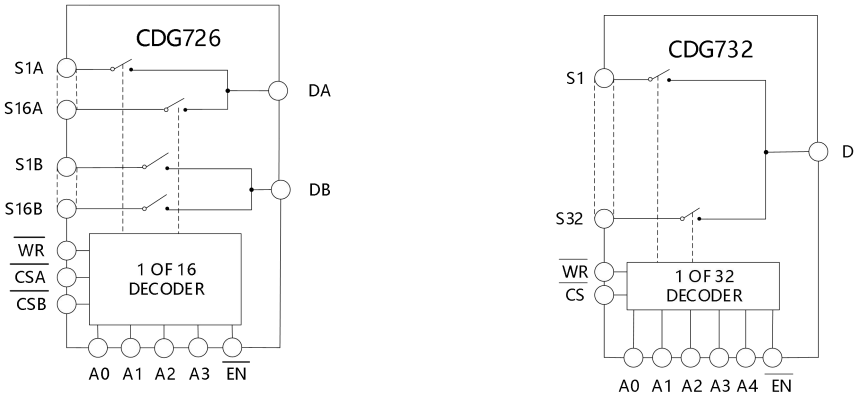


Figure 2. Functional Block Diagram

CDG726Truth Table

A3	A2	A1	A0	$\overline{EN}$	$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	On Switch
X	X	X	X	X	1	1	L→H	Latches control input data
X	X	X	X	X	1	1	X	No change in switch condition
X	X	X	X	1	X	X	X	None
0	0	0	0	0	0	0	0	S1A to DA, S1B to DB
0	0	0	1	0	0	0	0	S2A to DA, S2B to DB
0	0	1	0	0	0	0	0	S3A to DA, S3B to DB
0	0	1	1	0	0	0	0	S4A to DA, S4B to DB
0	1	0	0	0	0	0	0	S5A to DA, S5B to DB
0	1	0	1	0	0	0	0	S6A to DA, S6B to DB
0	1	1	0	0	0	0	0	S7A to DA, S7B to DB
0	1	1	1	0	0	0	0	S8A to DA, S8B to DB

1	0	0	0	0	0	0	0	S9A to DA, S9B to DB
1	0	0	1	0	0	0	0	S10A to DA, S10B to DB
1	0	1	0	0	0	0	0	S11A to DA, S11B to DB
1	0	1	1	0	0	0	0	S12A to DA, S12B to DB
1	1	0	0	0	0	0	0	S13A to DA, S13B to DB
1	1	0	1	0	0	0	0	S14A to DA, S14B to DB
1	1	1	0	0	0	0	0	S15A to DA, S15B to DB
1	1	1	1	0	0	0	0	S16A to DA, S16B to DB

CDG732Truth Table

A4	A3	A2	A1	A0	$\overline{EN}$	$\overline{CS}$	$\overline{WR}$	On Switch
X	X	X	X	X	X	1	L→H	Latches control input data
X	X	X	X	X	X	1	X	No change in switch condition
X	X	X	X	X	1	X	X	None
0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	2
0	0	0	1	0	0	0	0	3
0	0	0	1	1	0	0	0	4
0	0	1	0	0	0	0	0	5
0	0	1	0	1	0	0	0	6
0	0	1	1	0	0	0	0	7
0	0	1	1	1	0	0	0	8
0	1	0	0	0	0	0	0	9
0	1	0	0	1	0	0	0	10
0	1	0	1	0	0	0	0	11
0	1	0	1	1	0	0	0	12
0	1	1	0	0	0	0	0	13
0	1	1	0	1	0	0	0	14
0	1	1	1	0	0	0	0	15
0	1	1	1	1	0	0	0	16
1	0	0	0	0	0	0	0	17
1	0	0	0	1	0	0	0	18
1	0	0	1	0	0	0	0	19
1	0	0	1	1	0	0	0	20

Chinese version:CDG726_CDG732

1	0	1	0	0	0	0	0	21
1	0	1	0	1	0	0	0	22
1	0	1	1	0	0	0	0	23
1	0	1	1	1	0	0	0	24
1	1	0	0	0	0	0	0	25
1	1	0	0	1	0	0	0	26
1	1	0	1	0	0	0	0	27
1	1	0	1	1	0	0	0	28
1	1	1	0	0	0	0	0	29
1	1	1	0	1	0	0	0	30
1	1	1	1	0	0	0	0	31
1	1	1	1	1	0	0	0	32

Note：X is don’ t care, L is low, and H is high.

Absolute Maximum Ratings

Parameter	Rating
VDD to VSS	7 V
VDD to GND	−0.3V to +7V
VSS to GND	+0.3V to −7V
Analog, Digital Inputs1	−0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Digital Inputs1	−0.3V to VDD+0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA
Continuous Current, S or D	30mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance(TQFP48)	54.6°C/W

Electrical Characteristics

V_{DD} = +5 V±10%, V_{SS}=GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	3.5	5.5	--	5	6	V_S=0V to V_{DD}, I_S=10mA;See Figure 4	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	0.3	0.8	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness ($R_{FLAT(ON)}$)	--	0.5	--	--	--	1	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	± 0.25	--	--	±1	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 6	nA
Source Off Leakage I_D (Off)	--	± 0.05	±1	--	--	±5	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 6	nA
Channel On Leakage I_D, I_S (On)	--	± 0.05	±1	--	--	±5	V_S=V_D=1V, or 4.5V;See Figure 5	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current I_{INL} or I_{INH}	--	0.005	--	--	--	±0.5	V_{IN}=V_{INL} or V_{INH}	μA
Digital Input Capacitance(C_{IN})	--	5	--					pF
Dynamic Characteristics								
Transition Time($t_{TRANSITION}$)	--	23	34				RL = 300 Ω, CL = 35 pF,V_{S1} = 3 V/0 V, V_{S32} = 0 V/3 V	
t_{on}($\overline{CS}$,$\overline{WR}$)	--	18	25	--	--	32	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{OFF}($\overline{CS}$,$\overline{WR}$)	--	17	23	--	--	29	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{ON}($\overline{EN}$)	--	24	32	--	--	40	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{OFF}($\overline{EN}$)	--	16	22	--	--	25	R_L=300Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D	--	18	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=3V;	ns
Off Isolation	--	-72	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-72	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB

Bandwidth −3 dB(CDG726)	--	34	--					MHz
Bandwidth −3 dB(CDG732)		18	--					MHz
C_S(Off)	--	13	--					pF
C_D(Off) (CDG726)	--	170	--					pF
C_D(Off) (CDG732)	--	340	--					pF
C_D, C_S (On)-CDG726	--	175	--				f=1MHz;	pF
C_D, C_S (On)-CDG732	--	350	--				f=1MHz;	pF
Power Requirements								
I_{DD}	--	10	--	--	--	20	V_{DD}=+5.5V, Digital inputs=0V or 5V	μA

V_{DD} = +3 V±10%, V_{SS}=GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	4.5	11	--	--	12	V_S=0V to V_{DD}, I_S=10mA;See Figure 4	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	0.35	--	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness ($R_{FLAT(ON)}$)	--	1.5	--	--	3	--	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+3.3V	
Source Off Leakage I_S (Off)	--	± 0.01	± 0.25	--	--	±1	V_S=3V/1V, V_D=1V/3V;See Figure 6	nA
Source Off Leakage I_D (Off)	--	± 0.05	±1	--	--	±5	V_S=3V/3V, V_D=3V/1V;See Figure 6	nA
Channel On Leakage I_D, I_S (On)	--	± 0.05	±1	--	--	±5	V_S=V_D=1V, or 3V;See Figure 5	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current I_{INL} or I_{INH}	--	0.005	--	--	--	±0.5	V_{IN}=V_{INL} or V_{INH}	μA
Digital Input Capacitance(C_{IN})	--	5	--	--	--	--		pF
Dynamic Characteristics								
Transition Time($t_{TRANSITION}$)	--	34	52	--	--	62	RL = 300 Ω, CL = 35 pF,V_{S1} = 2 V/0 V, V_{S32} = 0 V/2 V	

$T_{on}(\overline{CS},\overline{WR})$	--	29	43	--	--	52	R_L=300Ω,C_L=35pF,V_S=2V	ns
$t_{OFF}(\overline{CS},\overline{WR})$	--	26	38	--	--	42	R_L=300Ω,C_L=35pF,V_S=2V	ns
$t_{ON}(\overline{EN})$	--	33	48	--	--	55	R_L=300Ω,C_L=35pF,V_S=2V	ns
$t_{OFF}(\overline{EN})$	--	19	25	--	--	28	R_L=300Ω,C_L=35pF,V_S=2V	ns
Break-Before-Make Time Delay, t_D	--	26	--	1	--	--	R_L=300Ω,C_L=35pF,V_S=2V	ns
Off Isolation	--	-72	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-72	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB
Bandwidth −3 dB(CDG726)	--	34	--					MHz
Bandwidth −3 dB(CDG732)		18	--					MHz
C_S(Off)	--	13	--					pF
C_D(Off) (CDG726)	--	170	--					pF
C_D(Off) (CDG732)	--	340	--					pF
C_D, C_S (On)-CDG726	--	175	--				f=1MHz;	pF
C_D, C_S (On)-CDG732	--	350	--				f=1MHz;	pF
Power Requirements								
I_{DD}	--	5	--	--	--	10	V_{DD}=+3.3V, Digital inputs=0V or 3.3V	μA

Typical Characteristics

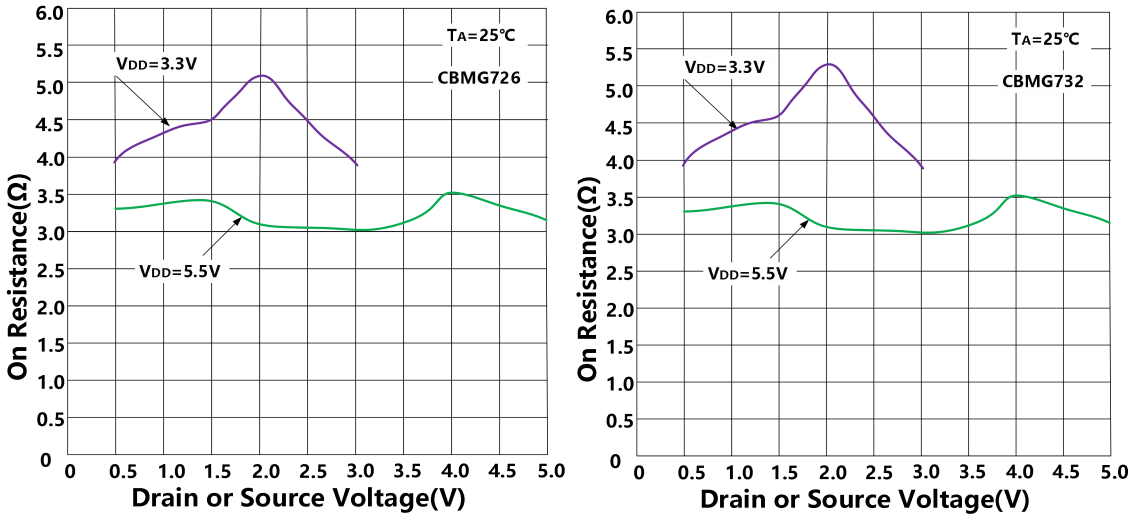
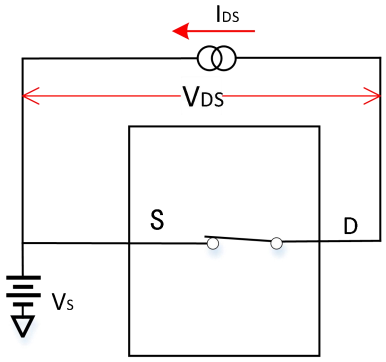


Figure 3.On Resistance vs. V_D (V_S)

Test Circuit



RON=V_{DS}/I_{DS}

Figure 4. On Resistance

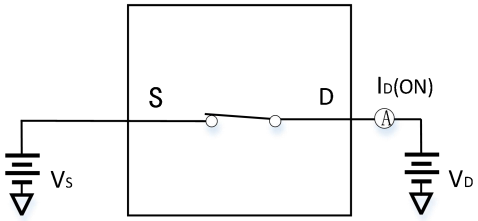


Figure 5. On Leakage

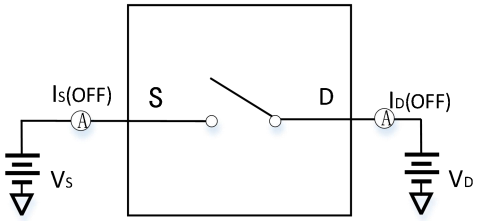


Figure 6. Off Leakage

Package Outline Dimensions

TQFP-48

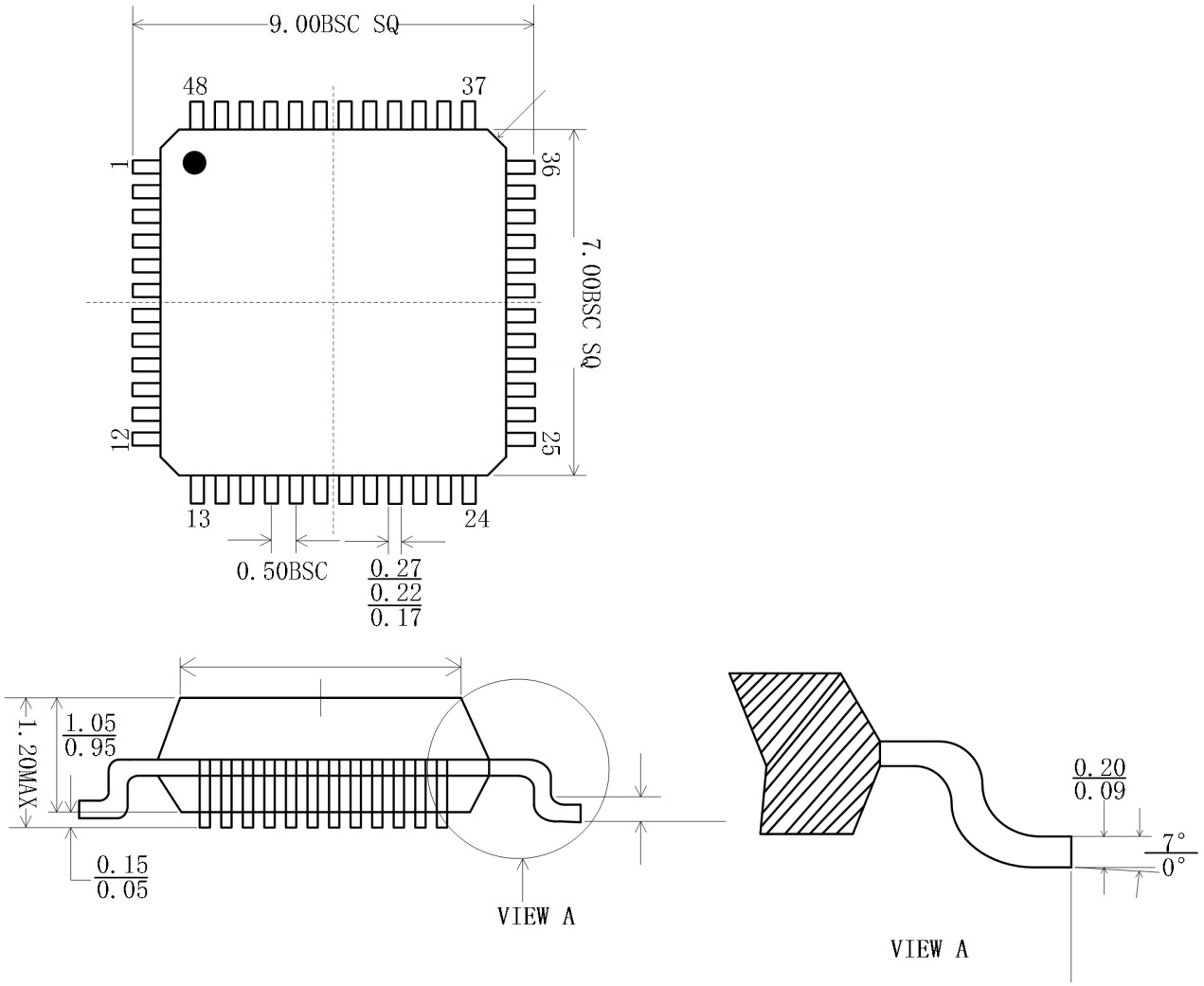


Figure 7.48-Lead Thin Plastic Quad Flat Package [TQFP]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDG726TQFP48	-40℃~85℃	TQFP-48	Tray, 1000
CDG732TQFP48	-40℃~85℃	TQFP-48	Tray, 1000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.18	Initial version	Regular update	WW	LYL	