CoreadDvices
承芯微电子

CDG728_CDG729

2-Wire Serially Controlled, Matrix Switches

Version: Rev 1.0.0 Date: 2025-6-18

Features

- 2-Wire Serial Interface
- 2.7 V to 5.5 V single supply
- 2.5 Ω on resistance
- 0.75 Ω on resistance flatness
- 100pA leakage currents
- Single 8-to-1 Matrix Switch CDG728
- Dual 4-to-1 Matrix Switch CDG729
- Power-on Reset
- 16-lead TSSOP

Application

- Data acquisition systems
- Communication systems
- Relay replacement
- Audio and video switching

Description

The CDG728 and CDG729 are CMOS analog matrix switches with a serially controlled 2-wire interface. The CDG728 is an 8-channel matrix switch, while the CDG729 is a dual 4-channel matrix switch. On resistance is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers, demultiplexers or switch arrays and the input signal range extends to the supplies.

The CDG728 and CDG729 utilize a 2-wire serial interface that is compatible with the I2 C™ interface standard. Both have two external address pins (A0 and A1). This allows the 2 LSBs of the 7-bit slave address to be set by the user. Four of each of the devices can be connected to the one bus. The CDG728 also has a RESET pin that should be tied high if not in use. Each channel is controlled by one bit of an 8-bit word. This means that these devices may be used in a number of different confifigurations; all, any, or none of the channels may be on at any one time.

On power-up of the device, all switches will be in the OFF condition and the internal shift register will contain all zeros. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. The CDG728 and CDG729 are available in 16-lead TSSOP packages.

Chinese version:CDG728 CDG729

Contents

Product Highlights

1. 2-Wire Serial Interface.

2. Single Supply Operation. The CDG728 and CDG729 are

fully specifiied and guaranteed with 3 V and 5 V supply rails.

3. Low On Resistance 2.5 Ω typical.

4. Any confifiguration of switches may be on at any one time.

5. Guaranteed Break-Before-Make Switching Action.

6. Small 16-Lead TSSOP Package.

Pin Configurations

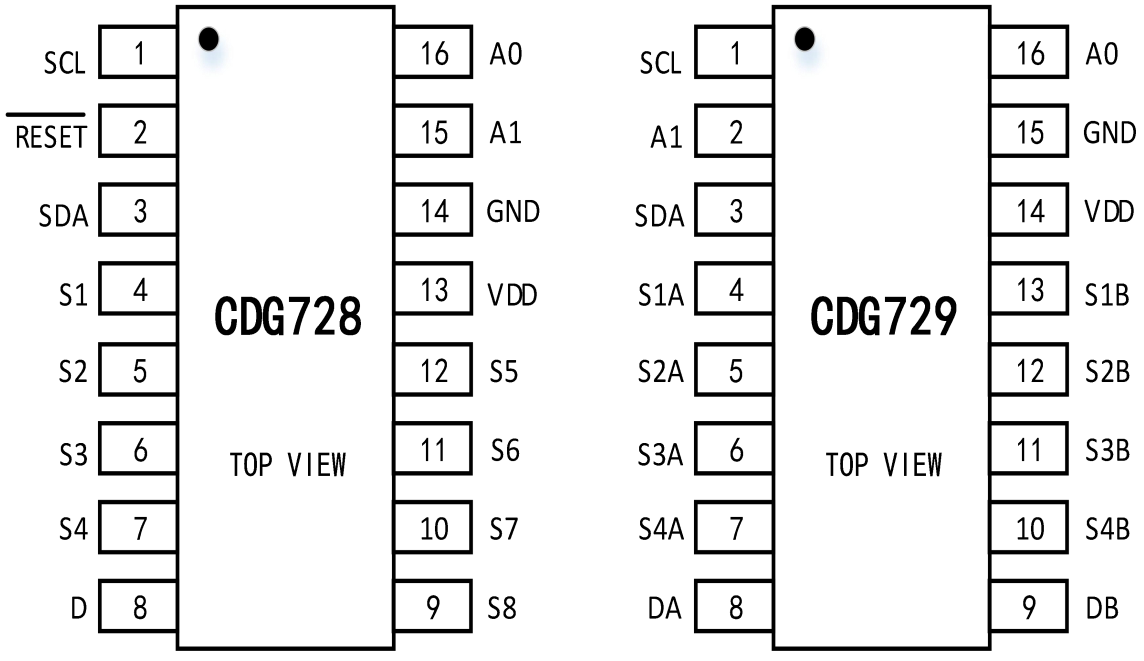


Figure 1. TSSOP16 Pin Configuration

Pin description

CDG728/CDG729

CDG728	CDG729	Pin Name	Description
1	1	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 8-bit input shift register. Clock rates of up to 400 kbit/s can be accommodated with this 2-wire serial interface.
2		$\overline{\text{RESET}}$	Active low control input that clears the input register and turns all switches to the OFF condition.
3	3	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 8-bit input shift register during the write cycle and used to read back 1 byte of data during the read cycle. It is a bidirectional open-drain data line which should be pulled to the supply with an external pull-up resistor.
4,5,6,7	4,5,6,7	Sxx	Source. These pins may be an input or an output.
8	8,9	Dx	Drain. These pins may be an input or an output.
9,10,11,12	10,11,12,13	Sxx	Source. These pins may be an input or an output.
13	14	V_{DD}	Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
14	15	GND	Ground (0 V) Reference.
15	2	A1	Address Input. Sets the second least significant bit of the 7-bit slave address.
16	16	A0	Address Input. Sets the least significant bit of the 7-bit slave address.

Functional Block diagram

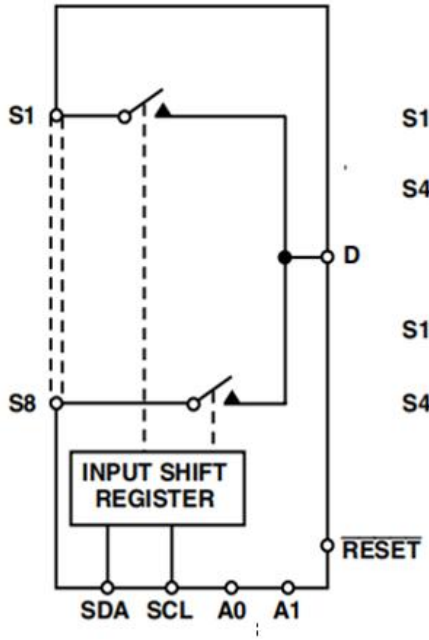


Figure 2. CDG728

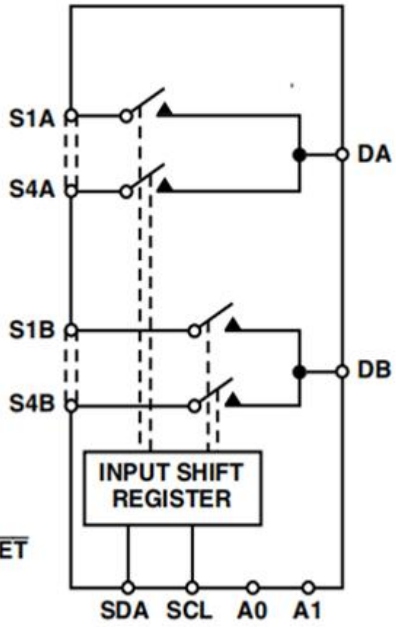


Figure 3. CDG729

Absolute Maximum Ratings

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs1	−0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA
Continuous Current, Each S	30mA
Continuous Current D, CDG729	80mA
Continuous Current D, CDG728	120mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature, Soldering	As per JEDEC J-STD-020
ESD	2kV

Electrical Characteristics

VDD = +5 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	2.5	4.5	--	--	5	V_S=0V to V_{DD}, I_S=10mA;See Figure 6	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	0.4	0.8	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	0.75	--	--	--	1.2	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=1V/4.5V, V_D=4.5V/1V;See Figure 8	nA
Drain Off Leakage I_D (Off)	--	± 0.01	±0.1	--	--	±1	V_S=1V/4.5V, V_D=4.5V/1V;See Figure 8	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±1	V_S=V_D=1V, or 4.5V;See Figure 7	nA
Logic Inputs (A0,A1)								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Digital Input Capacitance, C_{IN}	--	6	--	--	--	--		pF
Logic OUTPUT, SDA								
Output Voltage Low, V_{OL}	--	--	--	--	--	0.4	I_{SINK} = 3 mA	V
	--	--	--	--	--	0.6	I_{SINK} = 6 mA	V
DIGITAL INPUTS, SCL, SDA								
Input Voltage High, V_{INH}	--	--	--	0.7*V_{DD}		V_{DD}+0.3	V_{IN} = 0 V to V_{DD}	V
Input Voltage High, V_{INL}	--	--	--	-0.3		0.3*V_{DD}		V
Input Leakage Current, I_{IN}	--	0.005V	--	--	--	±1.0		μA

Input Hysteresis, VHYST	0.05 *VDD	--	--	--	--	--		V
Input Capacitance, CIN	--	6	--	--	--	--		pF
Dynamic Characteristics								
t_{on}	--	95	--	--	--	140	R_L=300 Ω,C_L=35pF,V_S=3V	ns
t_{OFF}	--	85	--	--	--	130	R_L=300 Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D	--	8	--	1	--	--	R_L=30 Ω,C_L=35pF,V_S=3V;	ns
Charge Injection,Q_{INJ}	--	±3	--				V_S=2.5V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-55	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-75	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-55	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
	--	-75	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB
Bandwidth −3 dB(CDG728)	--	65	--				R_L=50Ω, C_L=5pF;	MHz
Bandwidth −3 dB(CDG729)	--	100	--				R_L=50Ω, C_L=5pF;	MHz
C_S (OFF)	--	13	--					pF
C_D(OFF)-CDG728	--	85	--					pF
C_D(OFF)-CDG729	--	42	--					pF
C_D, C_S (On)-CDG728	--	96	--					pF
C_D, C_S (On)-CDG729	--	48	--					pF
Power Requirements								
I_{DD}	--	10	--	--	--	20	V_{DD}=+5.5V，Digital inputs=0V or 5V	μA

VDD = +3 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			-40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	6	11	--	--	12	V_S=0V to V_{DD}, I_S=10mA;See Figure 6	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	0.4	1.2	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	--	--	--	3.5	--	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+3.3V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=1V/3V, V_D=3V/1V;See Figure 8	nA
Drain Off Leakage I_D (Off)	--	± 0.01	±0.1	--	--	±1	V_S=1V/3V, V_D=3V/1V;See Figure 8	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±1	V_S=V_D=1V, or 3V;See Figure 7	nA
Logic Inputs (A0,A1)								
Input High Voltage, V_{INH}				2.0	--	--		V
Input Low Voltage, V_{INL}				--	--	0.4		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Digital Input Capacitance, C_{IN}	--	3	--	--	--	--		pF
DIGITAL INPUTS, SCL, SDA								
Input Voltage High, V_{INH}	--	--	--	0.7*V_{DD}	--	V_{DD}+0.3	V_{IN} = 0 V to V_{DD}	
Input Voltage High, V_{INL}	--	--	--	-0.3	--	0.3*V_{DD}		
Input Leakage Current, I_{IN}	--	0.005V	--	--	--	±1.0		
Input Hysteresis, V_{HYST}	0.05*VDD	--	--	--	--	--		
Input Capacitance, C_{IN}	--	3	--	--	--	--		

LOGIC OUTPUT, (SDA)								
Output Voltage Low, V_{OL}	--	--	--	--	--	0.4	I_{SINK} = 3 mA	
	--	--	--	--	--	0.6	I_{SINK} = 6 mA	
Dynamic Characteristics								
t_{on}	--	130	--	--	--	200	R_L=300 Ω,C_L=35pF,V_S=3V	ns
t_{OFF}	--	115	--	--	--	180	R_L=300 Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D	--	8	--	1	--	--	R_L=30 Ω,C_L=35pF,V_S=3V;	ns
Charge Injection,Q_{INJ}	--	±3	--				V_S=2V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-55	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-75	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-55	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
	--	-75	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB
Bandwidth −3 dB(CDG728)	--	65	--				R_L=50Ω, C_L=5pF;	MHz
Bandwidth −3 dB(CDG729)	--	100	--					
C_S (OFF)	--	13	--					pF
C_D (OFF)-CDG728	--	65	--					pF
C_D (OFF)-CDG729		100						
C_D, C_S (On)-CDG728	--	96	--					pF
C_D, C_S (On)-CDG729	--	48	--					pF
Power Requirements								
I_{DD}	--	10	--	--	--	20	V_{DD}=+3.3V, Digital inputs=0V or 3.3V	μA

Typical Characteristics

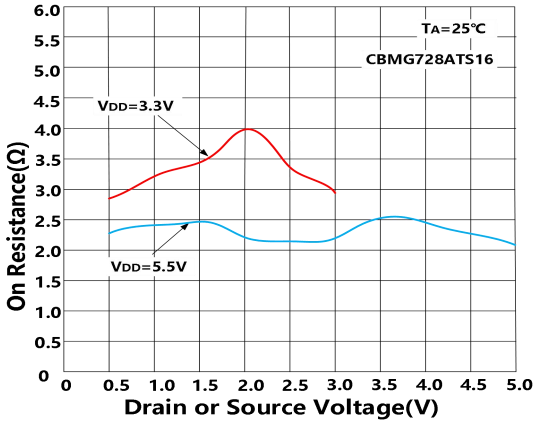


Figure 4.On Resistance vs. V_D (V_S)-(CDG728)

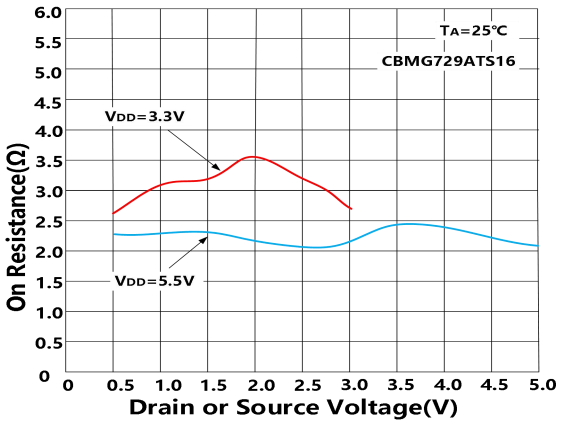
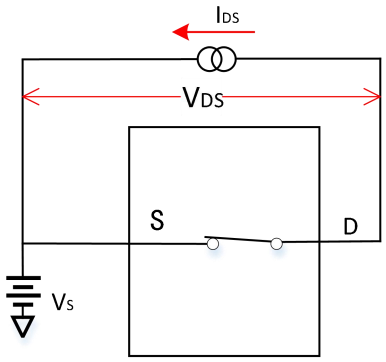


Figure 5.On Resistance vs. V_D (V_S)-(CDG729)

Test Circuit



RON=V_{DS}/I_{DS}

Figure 6. On Resistance

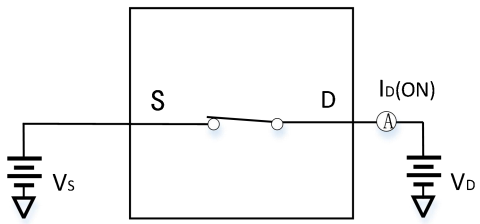


Figure 7. On Leakage

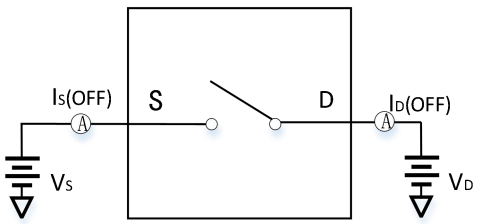


Figure 8. Off Leakage

Chinese version:CDG728_CDG729

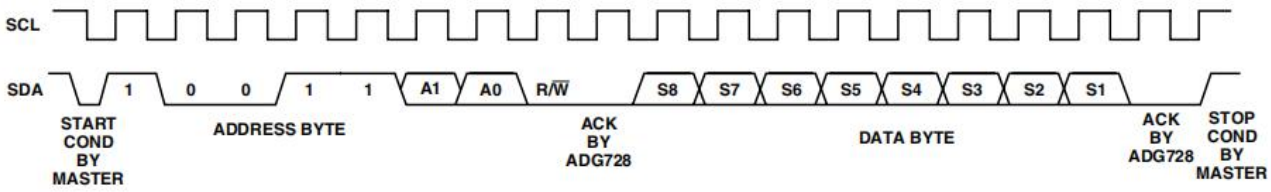


Figure 9. CDG728 Write Sequence

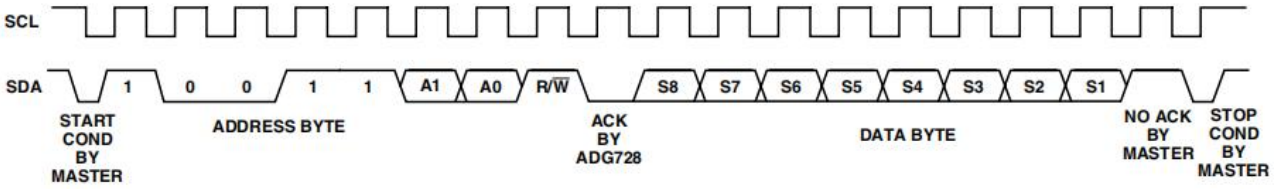


Figure 10. CDG728 Readback Sequence

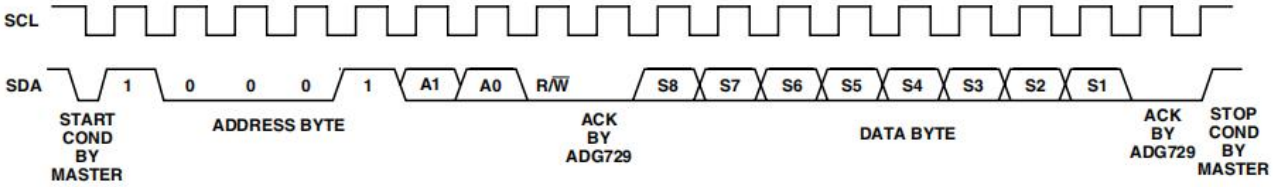


Figure 11. CDG729 Write Sequence

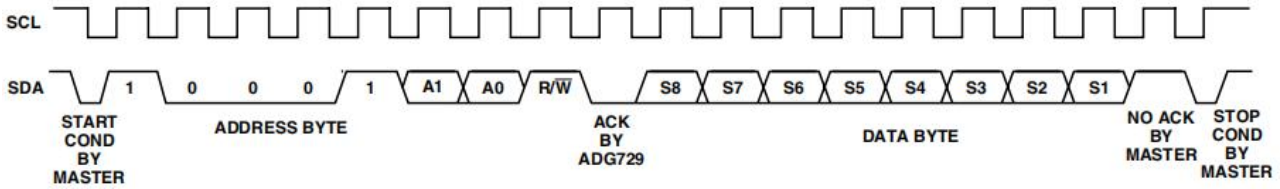


Figure 12. CDG729 Readback Sequence

Package Outline Dimensions

TSSOP-16

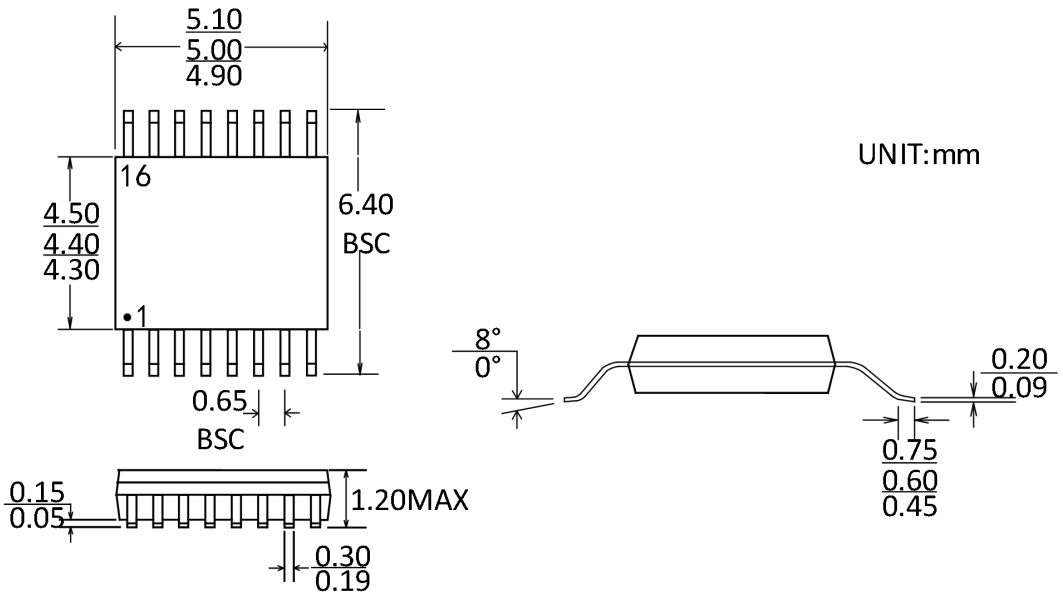


Figure 11. 24-Lead Outline Package [TSSOP]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDG728ATS16	-40℃~85℃	TSSOP-16	Tape and Reel, 3000
CDG729ATS16	-40℃~85℃	TSSOP-16	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.18	Initial version	Regular update	WW	LYL	