CoreadDvices
承芯微电子

CDG733_CDG734

Triple/Quad SPDT Switches

Version: Rev 1.0.0 Date: 2025-6-18

Features

- 1.8V to 5.5V Single Supply
- 2.5V Dual Supply
- 2.Ω On Resistance
- 0.5Ω On Resistance Flatness
- 100pA Leakage Currents
- 19ns Switching Times
- Triple SPDT: CDG733
- Quad SPDT: CDG734
- Small TSSOP and QSOP Packages
- Low Power Consumption
- TTL/CMOS Compatible Inputs

Application

- Data acquisition systems
- Communication systems
- Relay replacement
- Audio and video switching
- Battery Powered Systems

Description

The CDG733 and CDG734 are low voltage, CMOS devices comprising three independently selectable SPDT (single pole, double throw) switches and four independently selectable SPDT switches respectively.

Low power consumption and operating supply range of 1.8 V to 5.5 V and dual ±2.5 V make the CDG733 and CDG734 ideal for battery powered, portable instruments. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. An EN input on the CDG733 is used to enable or disable the device. When disabled, all channels are switched OFF.

These 2–1 multiplexers/SPDT switches are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, high signal bandwidths, and low leakage currents. On resistance is in the region of a few ohms, is closely matched between switches, and is very flat over the full signal range. These parts can operate equally well in either direction and have an input signal range that extends to the supplies.

The CDG733 is available in small TSSOP and QSOP packages, while the CDG734 is available in a small TSSOP package.

Contents

Product Highlights

1. Single/Dual Supply Operation. The ADG733 and ADG734 are fully specified and guaranteed with 3 V and 5 V single supply rails and ±2.5 V dual supply rails.

2. Low On Resistance (2.5 Ω typical)

3. Low Power Consumption (<0.01 μW)

4. Guaranteed Break-Before-Make Switching Action

Pin Configurations

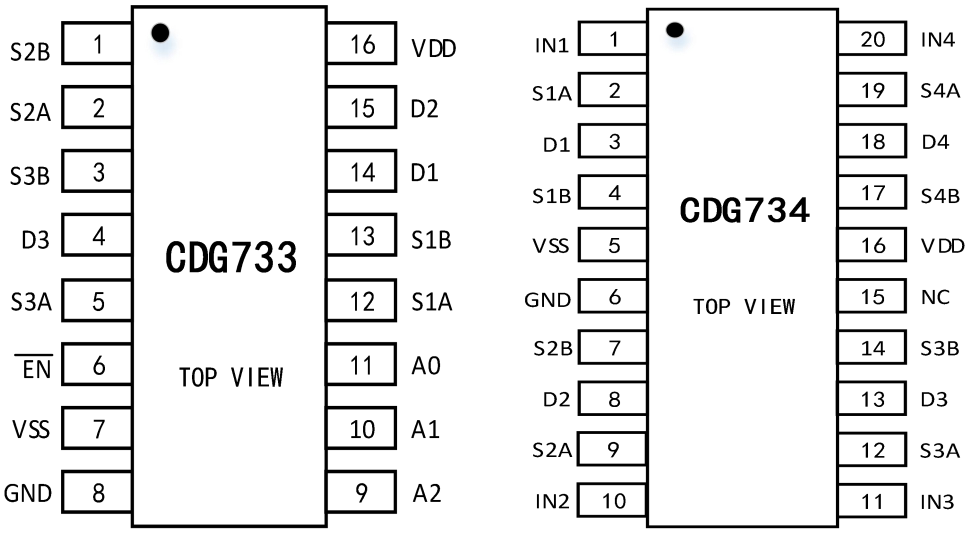


Figure 1. TSSOP16,TSSOP20 Pin Configuration

Pin description (CDG733)

Pin No.	Pin Name	Description
1	S2B	Source Pin S2B. May be an input or an output.
2	S2A	Source Pin S2A. May be an input or an output.
3	S3B	Source Pin S3B. May be an input or an output.
4	D3	Drain Pin D3. May be an input or an output.
5	S3A	Source Pin S3A. May be an input or an output.
6	$\overline{EN}$	Digital Input. Switch enable control line.
7	VSS	Negative Power Supply Pin in Dual-Supply Applications. For

		single-supply applications, it should be tied to GND.
8	GND	Ground (0 V) Reference.
9	A2	Digital Input. Channel selection control line A2.
10	A1	Digital Input. Channel selection control line A1.
11	A0	Digital Input. Channel selection control line A0.
12	S1A	Source Pin S1A. May be an input or an output.
13	S1B	Source Pin S1B. May be an input or an output.
14	D1	Drain Pin D1. May be an input or an output.
15	D2	Drain Pin D2. May be an input or an output.
16	V_{DD}	Positive Power Supply Input.

Table 1. Pin description（CDG734）

Pin No.	Pin Name	Description
1	IN1	Logic Control Input for Switch S1→D1.
2	S1A	Source Pin S1A. May be an input or an output.
3	D1	Drain Pin D1. May be an input or an output.
4	S1B	Source Pin S1B. May be an input or an output.
5	VSS	Negative Power Supply Pin in Dual-Supply Applications. For single-supply applications, it should be tied to GND.
6	GND	Ground (0 V) Reference.
7	S2B	Source Pin S2B. May be an input or an output.
8	D2	Drain Pin D2. May be an input or an output.
9	S2A	Source Pin S2A. May be an input or an output.
10	IN2	Logic Control Input for Switch S2→D2.
11	IN3	Logic Control Input for Switch S3→D3.
12	S3A	Source Pin S3A. May be an input or an output.
13	D3	Drain Pin D3. May be an input or an output.
14	S3B	Source Pin S3B. May be an input or an output.
15	NC	Drain Pin D2. May be an input or an output.
16	V_{DD}	Positive Power Supply Input.
17	S4B	Source Pin S4B. May be an input or an output.
18	D4	Drain Pin D4. May be an input or an output.
19	S4A	Source Pin S4A. May be an input or an output.
20	IN4	Logic Control Input for Switch S4→D4.

Functional Block diagram

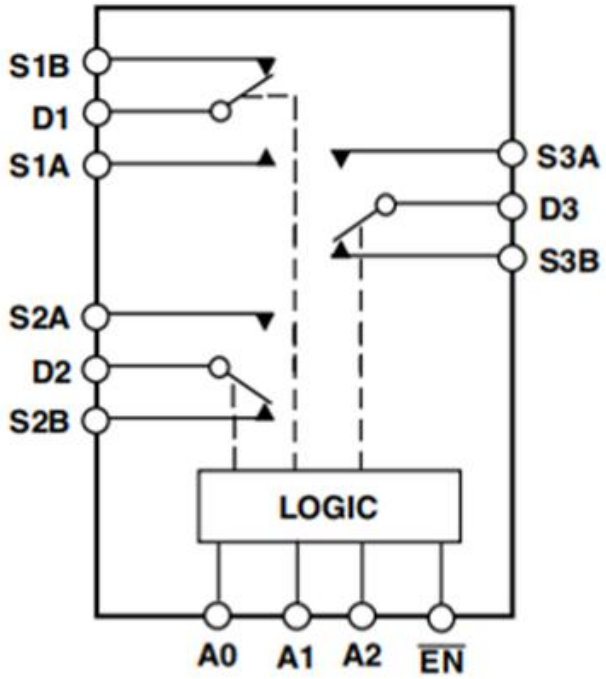


Figure 2. CDG733

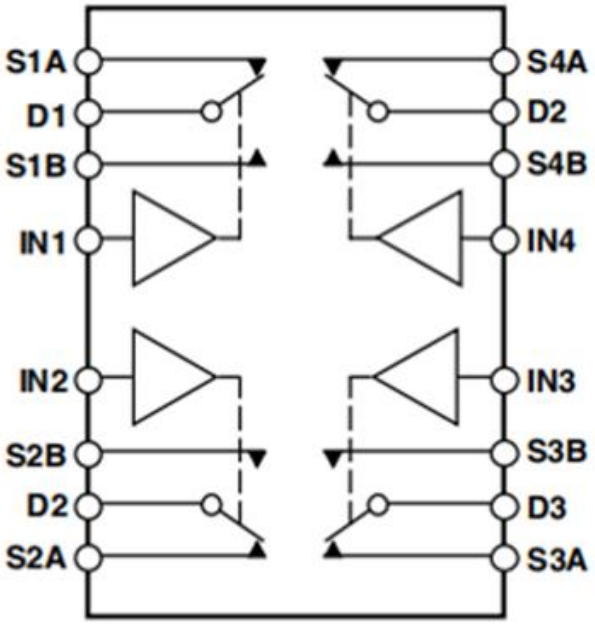


Figure 3. CDG734

Absolute Maximum Ratings

Parameter	Rating
VDD to VSS	+7 V
VDD to GND	−0.3 V to +7 V
Analog, Digital Inputs	−0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA
Continuous Current, Each S	30mA
Continuous Current D, CDG729	80mA
Continuous Current D, CDG728	120mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP θJA Thermal Impedance	150.4°C/W
20-Lead TSSOP θJA Thermal Impedance	143°C/W

Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature(15 sec)	235°C
ESD	2kV

Electrical Characteristics

VDD = +5 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	2.5	4.5	--	--	5.0	V_S=0V to V_{DD}, I_S=10mA;See Figure 8	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	--	0.4	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	0.5	--	--	--	1.2	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 10	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±0.5	V_S=V_D=1V, or 4.5V;See Figure 9	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	19	--	--	--	34	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{OFF}	--	7	--	--	--	12	R_L=300Ω,C_L=35pF,V_S=3V	ns
CDG733 t_{ON}($\overline{EN}$)	--	20	--	--	--	40	R_L = 300Ω, C_L = 35 pF;V_S=3V	ns
CDG733 t_{OFF}($\overline{EN}$)	--	7	--	--	--	12	R_L = 300 Ω, C_L = 35 pF;V_S = 3 V	ns
Break-Before-Make Time Delay, t_D	13		--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=3V;	ns
Charge Injection	--	±3	--				V_S=2V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-72	--				R_L=50Ω, C_L=5pF, f=1MHz	dB

Channel-to-Channel Crosstalk	--	-67	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB
Bandwidth −3 dB	--	160	--				R_L=50Ω, C_L=5pF;	MHz
C_S (OFF)	--	11	--					pF
C_D, C_S (On)	--	34	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+5.5V, Digital inputs=0V or 5V	μA

VDD = +3 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	6	11	--	--	12	V_S=0V to V_{DD}, I_S=10mA;See Figure 8	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	0.1	0.4	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	--	--	--	3	--	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+3.3V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=3V/1V, V_D=1V/3V;See Figure 10	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±0.5	V_S=V_D=1V, or 3V;See Figure 9	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.0	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	28	--	--	--	55	R_L=300Ω,C_L=35pF,V_S=2V	ns
t_{OFF}	--	9	--	--	--	16	R_L=300Ω,C_L=35pF,V_S=2V	ns
CDG733 t_{ON}($\overline{EN}$)	--	29	--	--	--	60	R_L = 300Ω, C_L = 35 pF;V_S=3V	ns
CDG733 t_{OFF}($\overline{EN}$)	--	9	--	--	--	16	R_L = 300 Ω, C_L = 35 pF;V_S = 3 V	ns
Break-Before-Make Time Delay, t_D	--	22	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=2V	ns

Charge Injection	--	±3	--				V_S=1.5V; R_S=0Ω, C_L=1nF	pC
Off Isolation	--	-72	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-67	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Bandwidth −3 dB	--	160	--				R_L=50Ω, C_L=5pF	MHz
C_S (OFF)	--	11	--					pF
C_D, C_S (On)	--	34	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+3.3V, Digital inputs=0V or 3V	μA

Typical Characteristics

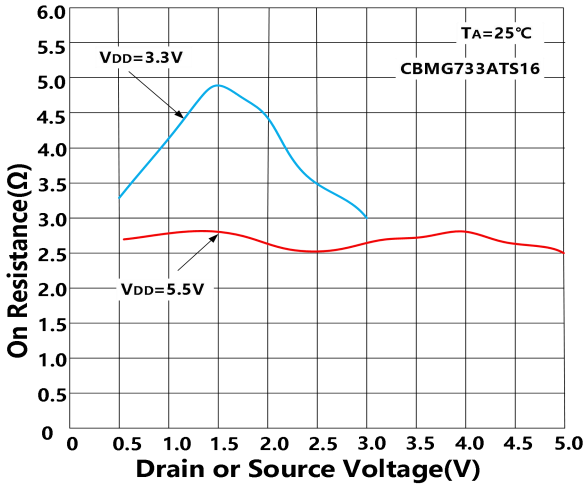


Figure 5.On Resistance vs. V_D (V_S)-(CDG733)

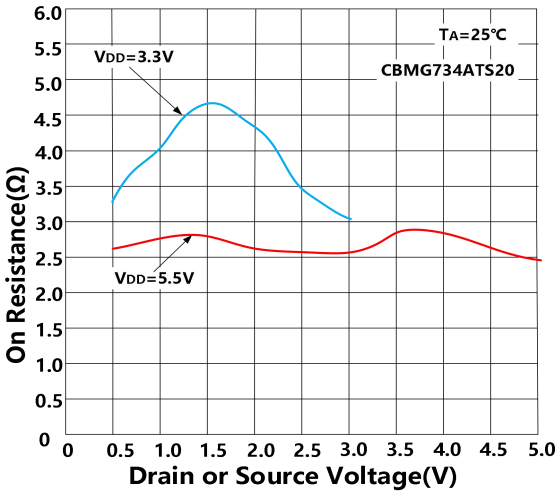
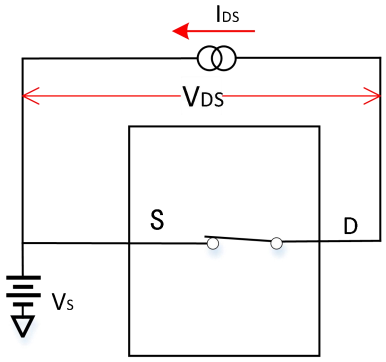


Figure 6.On Resistance vs. V_D (V_S)-(CDG734)

Test Circuit



RON=V_{DS}/I_{DS}

Figure 7. On Resistance

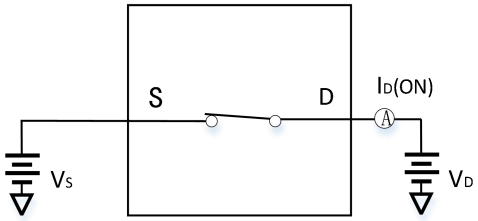


Figure 8. On Leakage

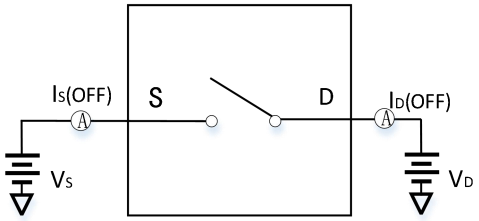


Figure 9. Off Leakage

Chinese version:CDG733_CDG734

Package Outline Dimensions

TSSOP-16

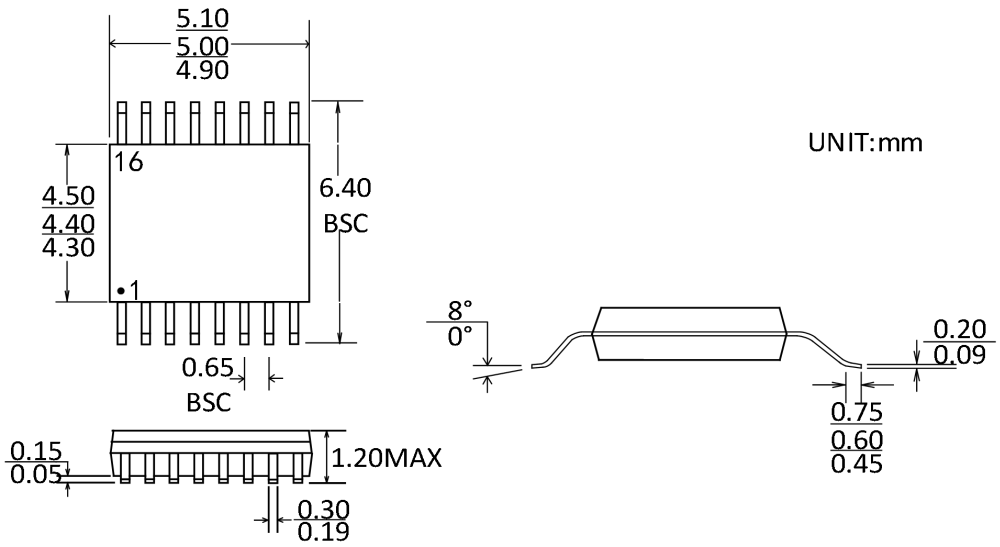


Figure 10. 16-Lead Outline Package [TSSOP]

TSSOP-20

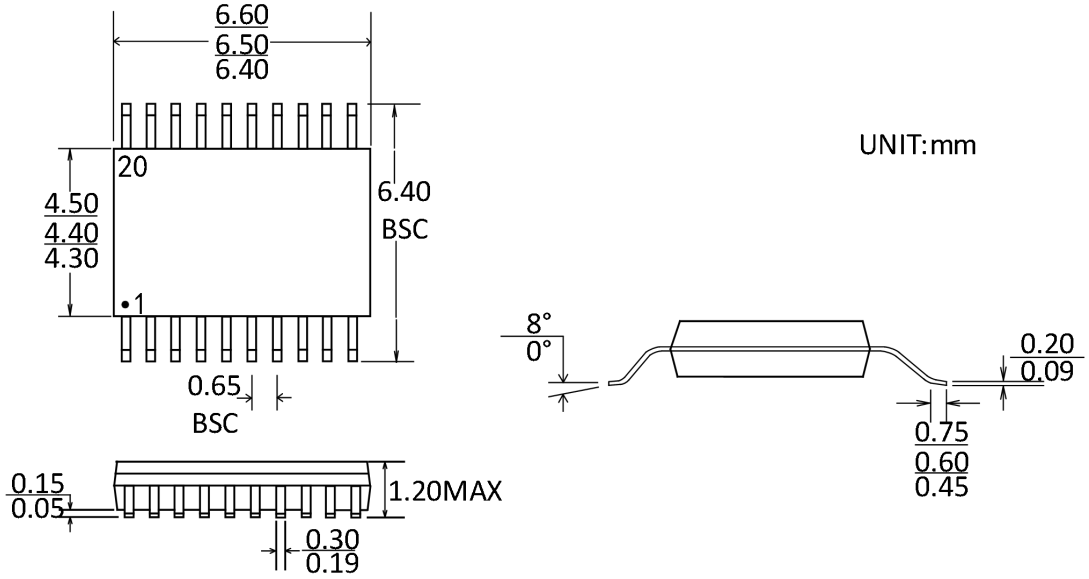


Figure 11. 20-Lead Outline Package [TSSOP]

Chinese version:CDG733 CDG734

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDG733ATS16	-40℃~85℃	TSSOP-16	Tape and Reel, 3000
CDG734ATS20	-40℃~85℃	TSSOP-20	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.18	Initial version	Regular update	WW	LYL	