CoreadDvices
承芯微电子

CDG736

Dual SPDT Switch

Version: Rev 1.0.0 Date: 2025-6-18

Features

- 1.8 V to 5.5 V single supply
- Low on resistance (2Ω Typ)
- Low on resistance flatness
- −3 dB bandwidth > 200 MHz
- Rail-to-rail operation
- 10-lead MSOP packages
- Fast switching times: t_{ON} = 16 ns t_{OFF} = 8 ns
- Typical power consumption: (< 0.01 μW)
- TTL/CMOS compatible

Application

- Cell phones
- Communication systems
- Sample-and-hold systems
- Audio signal routing
- Audio and video switching
- Battery-powered systems
- USB 1.1 signal switching circuits
- Mechanical reed relay replacement

Description

The CDG736 is a monolithic device comprising two independ- ently selectable CMOS single pole, double throw (SPDT) switches. These switches are designed using a submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents, and wide input signal bandwidth.

The on resistance profile is very flat over the full analog signal range. This ensures excellent linearity and low distortion when switching audio signals. Fast switching speed also makes the part suitable for video signal switching.

The CDG736 operates from a single 1.8 V to 5.5 V supply, making it ideally suited to portable and battery-powered instruments.

Each switch conducts equally well in both directions when on, and each has an input signal range that extends to the power supplies. The CDG736 exhibits break-before-make switching action. The CDG736 is available in a 10-lead MSOP package.

Contents

Product Highlights

1. 1.8V to 5.5V Single-Supply Operation. The CDG736 offers high performance, including low on resistance and fast switching times. It is fully specified and guaranteed with 3V and 5V supply rails.

2. Very Low R_{ON} (4.5Ω Maximum at 5V, 8Ω Maximum at 3V). At a supply voltage of 1.8 V, RON is typically 35Ω over the temperature range.

3. Low On Resistance Flatness.

4. −3dB Bandwidth > 200 MHz.

5. Low Power Dissipation. CMOS construction ensures low power dissipation.

6. Fast t_{ON}/t_{OFF}.

7. Break-Before-Make Switching Action.

8. 10-Lead MSOP Package.

Pin Configurations

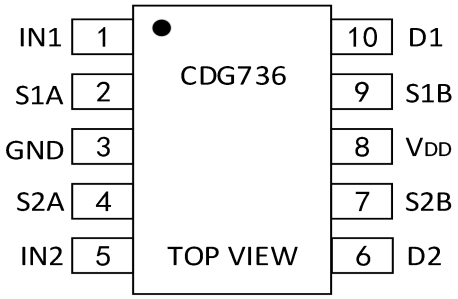


Figure 1. MSOP10 Pin Configuration

Pin description

Pin No.	Pin Name	Description
1	IN1	Logic Control Input.
2	S1A	Source Terminal. May be an input or output.
3	GND	Ground (0 V) Reference.
4	S2A	Source Terminal. May be an input or output.
5	IN2	Logic Control Input.
6	D2	Source Terminal. May be an input or output.
7	S2B	Source Terminal. May be an input or output.
8	V_{DD}	Most Positive Power Supply Potential.
9	S1B	Source Terminal. May be an input or output.
10	D1	Drain Terminal. May be an input or output.

Functional Block diagram

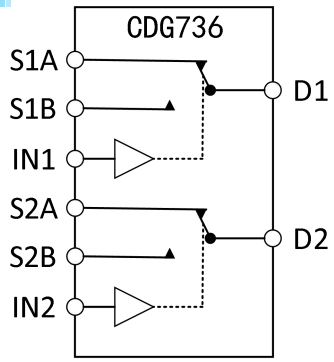


Figure 2. Switches shown for a logic "1" input

Truth Table

Logic	Switch A	Switch B
0	Off	On
1	On	Off

Absolute Maximum Ratings

Parameter	Rating
V_{DD} to GND	−0.3 V to +6 V
Analog, Digital Inputs1	−0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA
Continuous Current, S or D	30mA

Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP Package, Power Dissipation	315mW
θ_{JA} Thermal Impedance	205°C/W
Lead Temperature, Soldering Vapor Phase(10 sec)	300°C
IR Reflow, Peak Temperature (<20sec)	235°C
ESD	2 kV

Electrical Characteristics

VDD = +5 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	2.5	4	--	--	4.5	V_S=0V to V_{DD}, I_S=−10mA;See Figure 4	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	0.1	--	--	--	0.4	V_S=0 V to V_{DD}, I_S=−10mA	Ω
On Resistance Flatness ($R_{FLAT(ON)}$)	--	0.5	--	--	--	1.2	V_S=0 V to V_{DD}, I_S=−10mA	Ω
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	--	--	--	±0.2	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 6	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	--	--	--	±0.2	V_S=V_D=1V, or 4.5V;See Figure 5	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	12	--	--	--	16	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{OFF}	--	5	--	--	--	8	R_L=300Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D	--	7	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=3V;	ns

Off Isolation	--	-62	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-82	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-62	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
	--	-82	--				R_L=50Ω, C_L=5pF, f=1MHz;	
Bandwidth −3 dB	--	200	--				R_L=50Ω, C_L=5pF;	MHz
C_S	--	9	--					pF
C_D, C_S (On)	--	32	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+5.5V, Digital inputs=0V or 5V	μA

VDD = +3 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25℃			-40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	5	--	--	5.5	8	V_S=0V to V_{DD}, I_S=−10mA;See Figure 4	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	0.1	--	--	--	0.4	V_S=0 V to V_{DD}, I_S=−10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	--	--	--	2.5	--	V_S=0 V to V_{DD}, I_S=−10mA	Ω
Leakage Currents							V_{DD}=+3.3V	
Source Off Leakage I_S (Off)	--	± 0.01	--	--	--	--	V_S=3V/1V, V_D=1V/3V;See Figure 6	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	--	--	--	--	V_S=V_D=1V, or 3V;See Figure 5	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.0	--	--		V
Input Low Voltage, V_{INL}				--	--	0.4		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	14	--	--	--	20	R_L=300Ω,C_L=35pF,V_S=2V	ns
t_{OFF}	--	6	--	--	--	10	R_L=300Ω,C_L=35pF,V_S=2V	ns
Break-Before-Make Time Delay, t_D (CDG713 Only)	--	7	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=2V;	ns

Chinese version:CDG736

Off Isolation	--	-62	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-82	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-62	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
	--	-82	--				R_L=50Ω, C_L=5pF, f=1MHz;	
Bandwidth −3 dB	--	200	--				R_L=50Ω, C_L=5pF;	MHz
C_S	--	9	--					pF
C_D, C_S (On)	--	32	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+3.3V, Digital inputs=0V or 3V	μA

Typical Characteristics

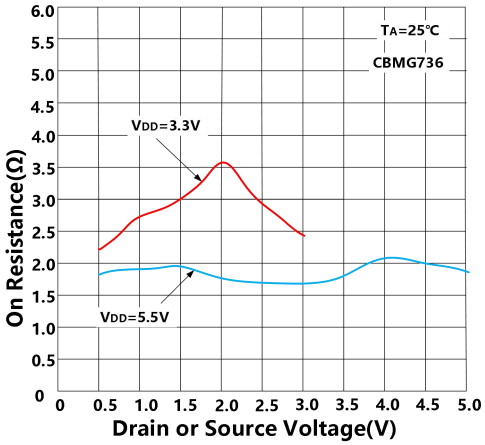
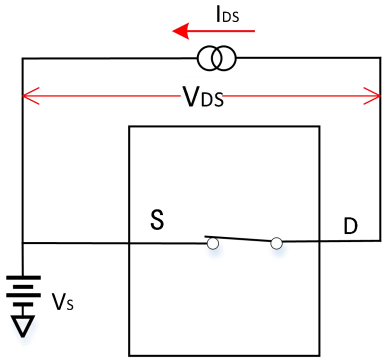


Figure 3.On Resistance vs. V_D (V_S)

Test Circuit



RON=V_{DS}/I_{DS}

Figure 4. On Resistance

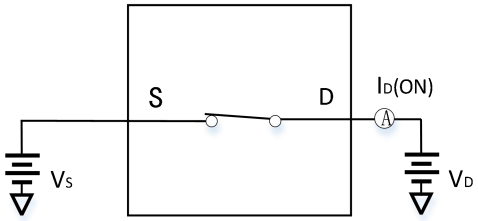


Figure 5. On Leakage

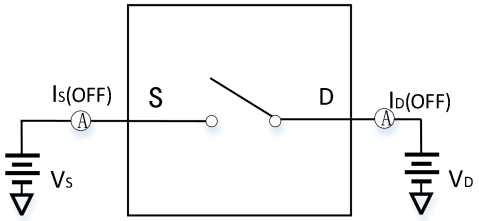


Figure 6. Off Leakage

Package Outline Dimensions

MSOP-10

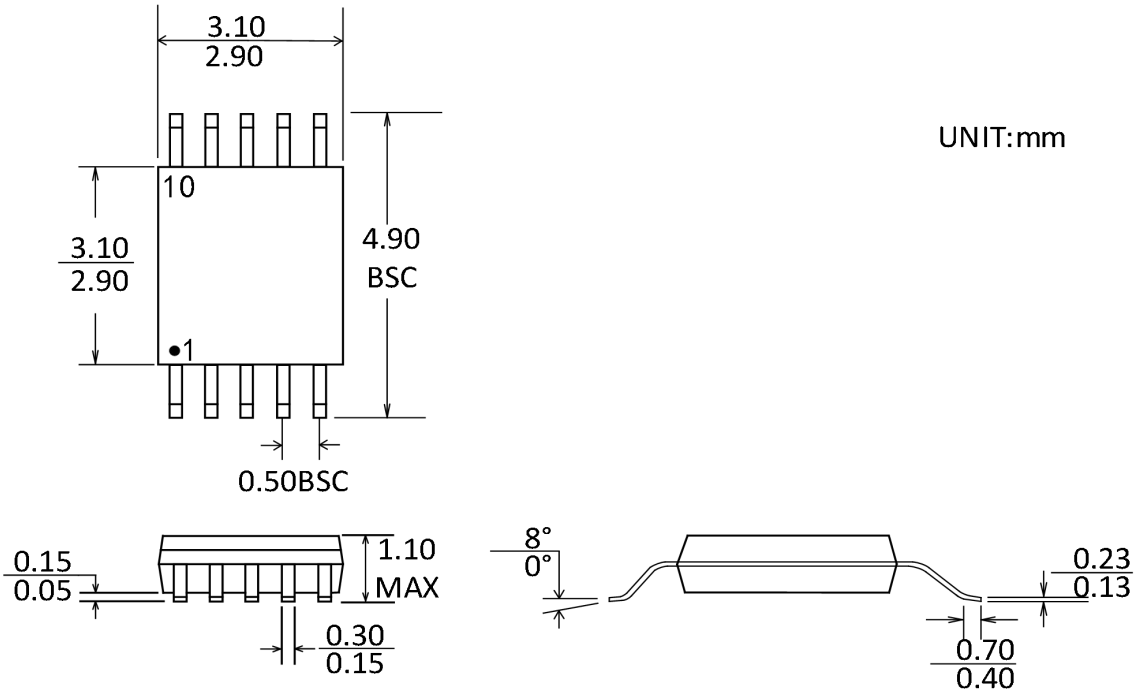


Figure 7. 10-Lead Mini Small Outline Package [MSOP]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDG736AMS10	-40℃~125℃	MSOP-10	Tape and Reel,3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.18	Initial version	Regular update	WW	LYL	