CoreadDvices
承芯微电子

CDG738_CDG739_

3-Wire Serially-Controlled, Matrix Switches

Version: Rev 1.0.0 Date: 2025-6-18

Features

- 3-wire serial interface
- 2.7 V to 5.5 V single supply
- 2.5 Ω on resistance
- 0.75 Ω on-resistance flatness
- 100 pA leakage currents
- Single 8-to-1 multiplexer CDG738
- Dual 4-to-1 multiplexer CDG739
- Power-on reset
- TTL/CMOS-compatible
- 16-lead TSSOP

Application

- Data acquisition systems
- Communication systems
- Relay replacement
- Audio and video switching

Description

The CDG738 and CDG739 are CMOS analog matrix switches with a serially-controlled 3-wire interface. The CDG738 is an 8-channel matrix switch, while the CDG739 is a dual 4-channel matrix switch. On resistance is closely matched between switches and very flat over the full signal range. The CDG738 and CDG739 utilize a 3-wire serial interface that is compatible with SPI™, QSPI™, MICROWIRE®, and some DSP interface standards. The output of the input shift register, DOUT, enables a number of these parts to be daisy-chained. On power-up, the internal input shift register contains all zeros and all switches are in the off state.

Each switch conducts equally well in both directions when on, making these parts suitable for both multiplexing and demulti-plexing applications. As each switch is turned on or off by a separate bit, these parts can also be configured as a type of switch array, where any, all, or none of the eight switches may be closed at any time. The input signal range extends to the supply rails.

Contents

Product Highlights

1. 3-Wire Serial Interface.

2. Single Supply Operation. The ADG738/ADG739 are fully specified and guaranteed with 3 V and 5 V supply rails.

3. Low On Resistance, 2.5 Ω typical.

4. Any configuration of switches may be on or off at any one time.

5. Guaranteed Break-Before-Make Switching Action.

6. Small 16-lead TSSOP Package.

Pin Configurations

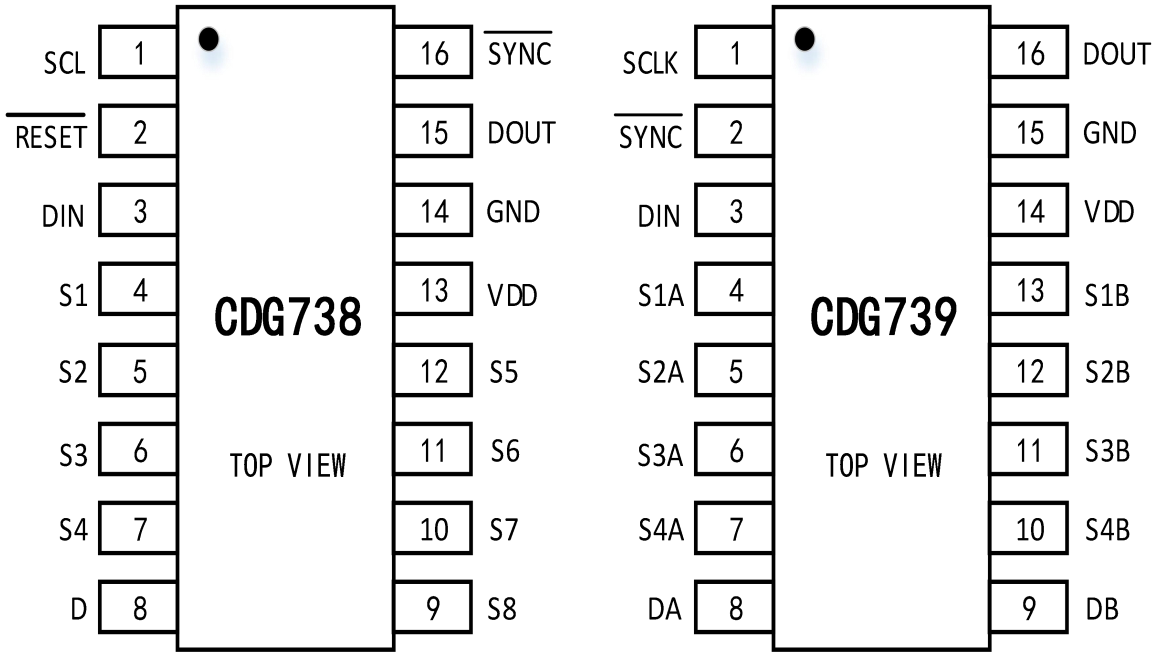


Figure 1. TSSOP16 Pin Configuration

Pin description

CDG738

CDG738	Pin Name	Description
1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz.
2	$\overline{\text{RESET}}$	Active Low Control Input. This pin clears the input register and turns all switches to the off condition.
3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4,5,6,7	S1,S2,S3,S4	Source. May be an input or output.
8	D	Drain. May be an input or output.
9,10,11,12	S8,S7,S6,S5	Source. May be an input or output
13	V_{DD}	Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
14	GND	Ground (0 V) Reference.
15	DOUT	Data Output. This allows a number a parts to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. This is an open drain output, which should be pulled to the supply with an external resistor.
16	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When SYNC goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clocks. Taking SYNC high updates the switch conditions.

Pin description

CDG739

CDG739	Pin Name	Description
1	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accommodate serial input rates of up to 30 MHz.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When SYNC goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. Data is transferred on the falling edges of the following clocks. Taking SYNC high updates the switch conditions.

3	DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
4,5,6,7	S1A,S2A,S3A, S4A	Source. May be an input or output.
8,9	DA,DB	Drain. May be an input or output.
10,11,12,13	S4B,S3B,S2B,S 1B	Source. May be an input or output
14	V_{DD}	Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V.
15	GND	Ground (0 V) Reference.
16	DOUT	Data Output. This allows a number a parts to be daisy-chained. Data is clocked out of the input shift register on the rising edge of SCLK. This is an open drain output, which should be pulled to the supply with an external resistor.

Functional Block diagram

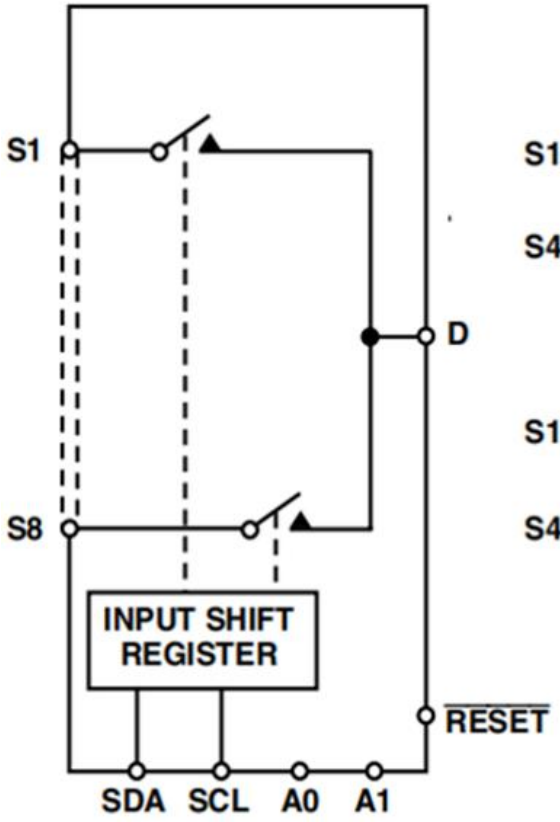


Figure 2. CDG738

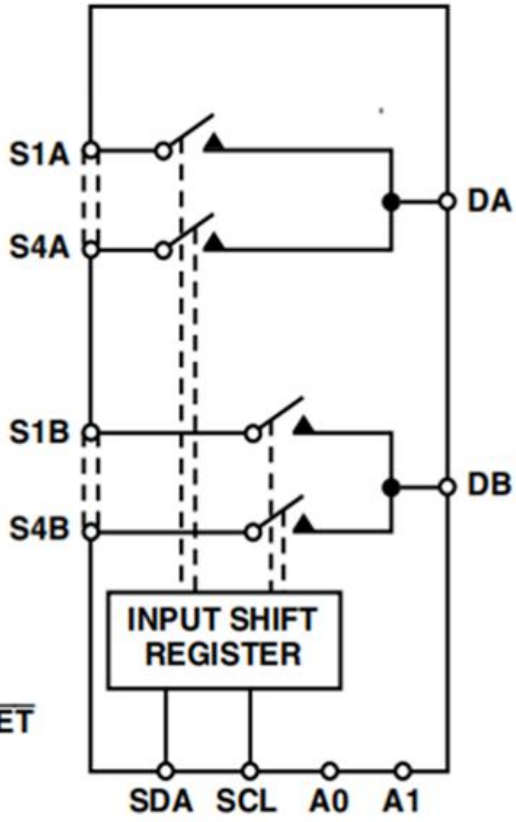


Figure 3. CDG739

Absolute Maximum Ratings

Parameter	Rating
VDD to GND	−0.3 V to +7 V
Analog, Digital Inputs	−0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA
Continuous Current, Each S	30mA
Continuous Current D, CDG739	80mA
Continuous Current D, CDG738	120mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature, Soldering	As per JEDEC J-STD-020
ESD	2kV

Electrical Characteristics

V_{DD} = +5 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	2.5	4.5	--	--	5	V_S=0V to V_{DD}, I_S=10mA;See Figure 6	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	0.4	0.8	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	0.75	--	--	--	1.2	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=1V/4.5V, V_D=4.5V/1V;See Figure 8	nA
Drain Off Leakage I_D (Off)	--	± 0.01	±0.1	--	--	±1	V_S=1V/4.5V, V_D=4.5V/1V;See	nA

							Figure 8	
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±1	V_S=V_D=1V, or 4.5V;See Figure 7	nA
DIGITAL Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Digital Input Capacitance, C_{IN}	--	3	--	--	--	--		pF
Logic OUTPUT, SDA								
Output Voltage Low, V_{OL}	--	--	--	--	--	0.4	I_{SINK} = 6 mA	V
Dynamic Characteristics								
t_{on}	--	20	--	--	--	32	R_L=300 Ω,C_L=35pF,V_S=3V	ns
t_{OFF}	--	10	--	--	--	17	R_L=300 Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D	--	9	--	1	--	--	R_L=30 Ω,C_L=35pF,V_S=3V;	ns
Charge Injection,Q_{INJ}	--	±3	--				V_S=2.5V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-55	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-75	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-55	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
	--	-75	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB
Bandwidth −3 dB(CDG738)	--	65	--				R_L=50Ω, C_L=5pF;	MHz
Bandwidth −3 dB(CDG739)	--	100	--				R_L=50Ω, C_L=5pF;	MHz
C_S (OFF)	--	13	--					pF
C_D(OFF)-CDG738	--	85	--					pF
C_D(OFF)-CDG739	--	42	--					pF
C_D, C_S (On)-CDG728	--	96	--					pF
C_D, C_S (On)-CDG729	--	48	--					pF
Power Requirements								
I_{DD}	--	10	--	--	--	20	V_{DD}=+5.5V, Digital inputs=0V or 5V	μA

V_{DD} = +3 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			-40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	6	11	--	--	12	V_S=0V to V_{DD}, I_S=10mA;See Figure 6	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	--	--	--	0.4	1.2	V_S=0 V to V_{DD}, I_S=10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	3.5	--	--	--	--	V_S=0 V to V_{DD}, I_S=10mA	Ω
Leakage Currents							V_{DD}=+3.3V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.3	V_S=1V/3V, V_D=3V/1V;See Figure 8	nA
Drain Off Leakage I_D (Off)	--	± 0.01	±0.1	--	--	±1	V_S=1V/3V, V_D=3V/1V;See Figure 8	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±1	V_S=V_D=1V, or 3V;See Figure 7	nA
DIGITAL Input								
Input High Voltage, V_{INH}				2.0	--	--		V
Input Low Voltage, V_{INL}				--	--	0.4		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Digital Input Capacitance, C_{IN}	--	3	--	--	--	--		pF
LOGIC OUTPUT, (SDA)								
Output Voltage Low, V_{OL}	--	--	--	--	--	0.4	I_{SINK} = 6 mA	
Dynamic Characteristics								
t_{on}	--	40	--	--	--	70	R_L=300 Ω,C_L=35pF,V_S=3V	ns
t_{OFF}	--	14	--	--	--	25	R_L=300 Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D	--	12	--	1	--	--	R_L=30 Ω,C_L=35pF,V_S=3V;	ns
Charge Injection,Q_{INJ}	--	±3	--				V_S=2V; R_S=0Ω, C_L=1nF;	pC

Off Isolation	--	-55	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-75	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-55	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
	--	-75	--				R_L=50Ω, C_L=5pF, f=1MHz;	dB
Bandwidth −3 dB(CDG738)	--	65	--				R_L=50Ω, C_L=5pF;	MHz
Bandwidth −3 dB(CDG739)	--	100	--					
C_S (OFF)	--	13	--					pF
C_D (OFF)-CDG738	--	85	--					pF
C_D (OFF)-CDG739		42						
C_D, C_S (On)-CDG738	--	96	--					pF
C_D, C_S (On)-CDG739	--	48	--					pF
Power Requirements								
I_{DD}	--	10	--	--	--	20	V_{DD}=+3.3V, Digital inputs=0V or 3.3V	μA

Typical Characteristics

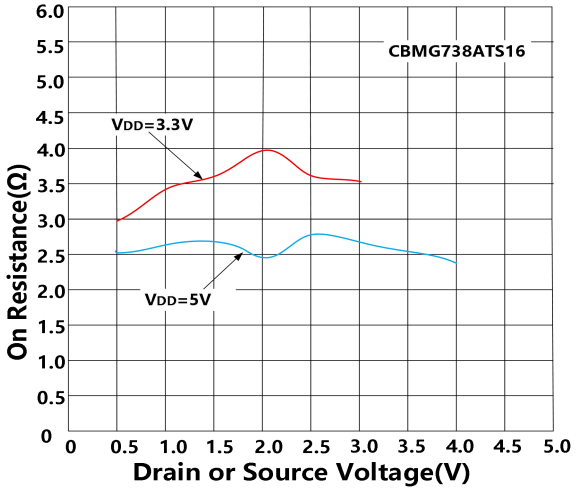


Figure 4.On Resistance vs. V_D (V_S)-(CDG738)

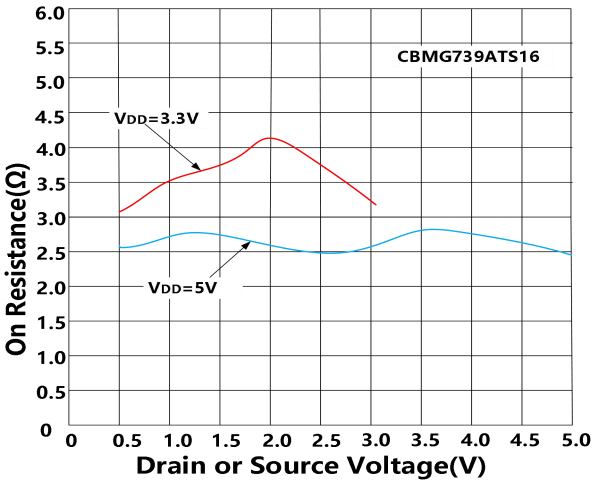
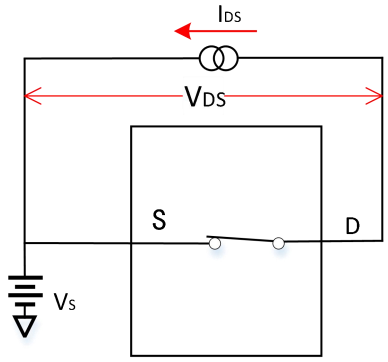


Figure 5.On Resistance vs. V_D (V_S)-(CDG739)

Test Circuit



RON=V_{DS}/I_{DS}

Figure 6. On Resistance

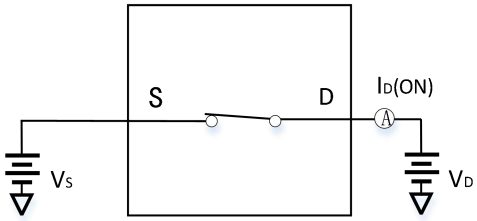


Figure 7. On Leakage

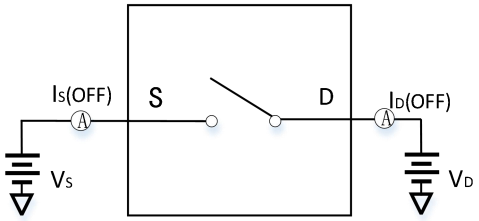


Figure 8. Off Leakage

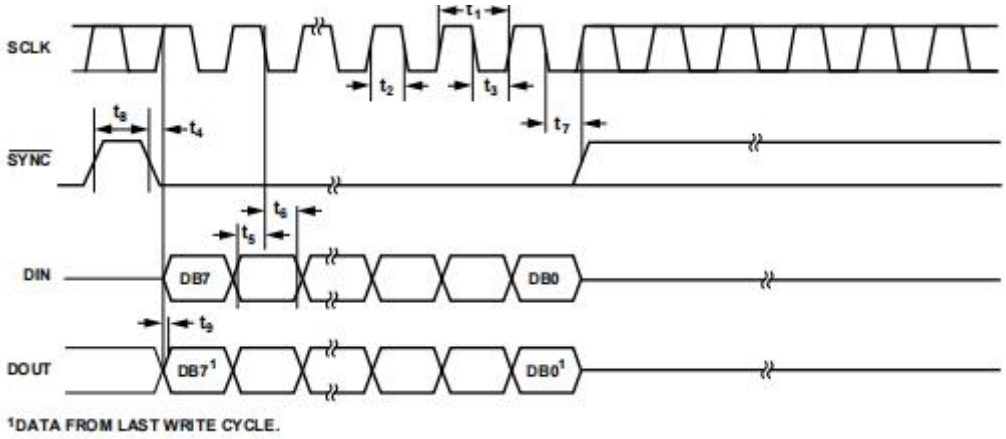


Figure 9. 3-Wire Serial Interface Timing Diagram

Package Outline Dimensions

TSSOP-16

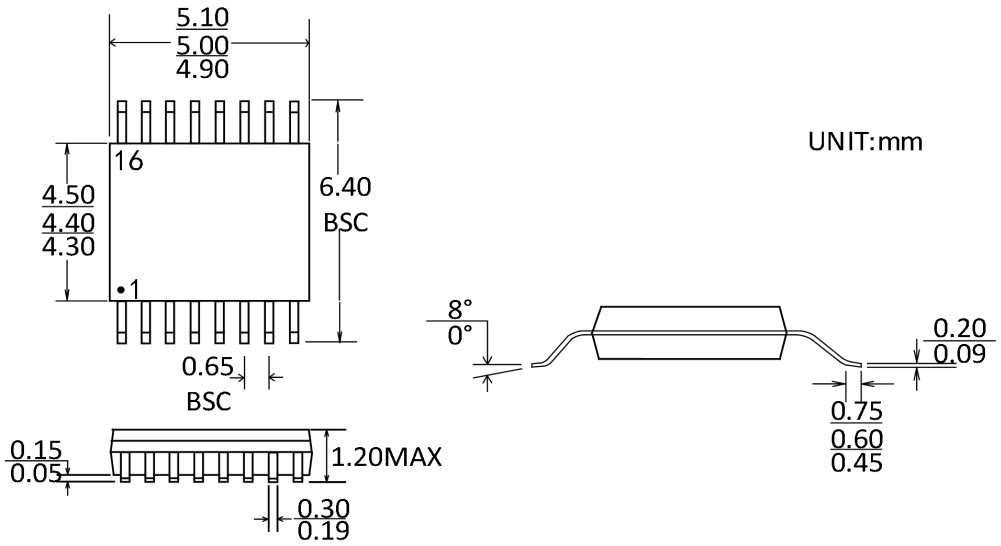


Figure 10. 16-Lead Outline Package [TSSOP]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDG738ATS16	-40℃~85℃	TSSOP-16	Tape and Reel, 3000
CDG739ATS16	-40℃~85℃	TSSOP-16	Tape and Reel, 3000