CoreadDvices
承芯微电子

CDG781_CDG782_CDG783

Quad, SPST Switches

Version: Rev 1.0.0 Date: 2025-6-18

Features

- 1.8 V to 5.5 V Single Supply
- Low On Resistance (2.5Ω Typ)
- Low On-Resistance Flatness (0.5Ω)
- –3 dB Bandwidth > 200 MHz
- Rail-to-Rail Operation
- 20-Lead 4 mm x 4 mm Chip Scale Package
- Fast Switching Times

  t_{ON}=16 ns

  t_{OFF}=10 ns
- Typical Power Consumption (< 0.01μW)
- TTL/CMOS Compatible
- For Functionally Equivalent Devices in 16-Lead and SOIC Packages, See CDG711/CDG712/CDG713 TSSOP

Application

- Cell phones
- Video switching
- Communication systems
- Battery-powered systems
- USB 1.1 signal switching circuits
- Mechanical reed relay replacement

Description

The CDG781, CDG782, and CDG783 are monolithic CMOS devices containing four independently selectable switches. These switches are designed on an advanced submicron process that provides low power dissipation and high switching speed, low on resistance, low leakage currents and high bandwidth. They are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery powered instruments and with the new generation of DACs and ADCs from Analog Devices. Fast switching times and high bandwidth make the part suitable for video signal switching. The CDG781, CDG782, and CDG783 contain four independent single-pole/single throw (SPST) switches. The CDG781 and CDG782 differ only in that the digital control logic is inverted. The CDG781 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the CDG782. The CDG783 contains two switches whose digital control logic is similar to the CDG781, while the logic is inverted on the other two switches. Each switch conducts equally well in both directions when ON. The CDG783 exhibits break-before-make switching action.
The CDG781/CDG782/CDG783 are available in 20-lead chip scale packages.

Contents

Product Highlights

1. 20-Lead 4mm X 4mm Chip Scale Package (QFN).

2. 1.8 V to 5.5 V Single Supply Operation. The CDG781, CDG782, and CDG783 offer high performance and are fully specified and guaranteed with 3 V and 5 V supply rails.

3. Very Low R_{ON} (4.5 Ω max at 5 V, 8 Ω max at 3 V). At supply voltage of 1.8 V, RON is typically 35 Ω over the temperature range.

4. Low On-Resistance Flatness.

5. –3 dB Bandwidth >200 MHz.

6. Low Power Dissipation. CMOS construction ensures low power dissipation.

7. Fast t_{ON}/t_{OFF}.

8. Break-Before-Make Switching. This prevents channel shorting when the switches are configured as a multiplexer (CDG783 only).

Pin Configurations

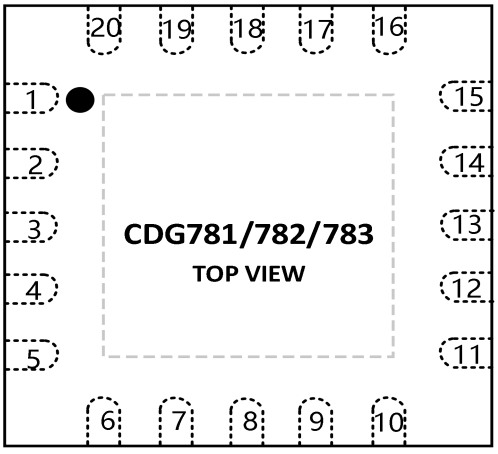


Figure 1. QFN20 Pin Configuration

Pin description

Pin No.	Pin Name	Description
1	D1	Drain Pin 1. May be an input or an output.
2	S1	Source Pin 1. May be an input or an output.
3	GND	Ground (0 V) Reference.
4	S4	Source Pin 4. May be an input or an output.
5	D5	Drain Pin 5. May be an input or an output.
6	NC	No Connect
7	IN4	Logic Control Input for Switch S4→D4.
8	NC	Positive Power Supply Input.
9	IN3	Logic Control Input for Switch S3→D3.
10	NC	No Connect
11	D3	Drain Pin 3. May be an input or an output.
12	S3	Source Pin 3. May be an input or an output.
13	V_{DD}	Positive Power Supply Input.
14	S2	Source Pin 2. May be an input or an output.
15	D2	Drain Pin 2. May be an input or an output.
16	NC	No Connect
17	IN2	Logic Control Input for Switch S2→D2.
18	NC	No Connect
19	IN1	Logic Control Input for Switch S1→D1.
20	NC	No Connect

Functional Block diagram

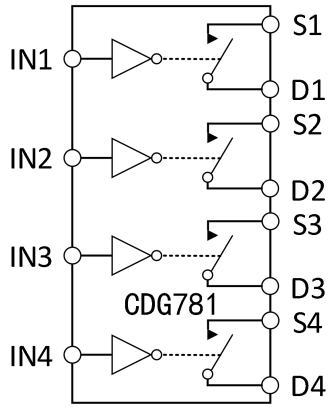


Figure 2. CDG721

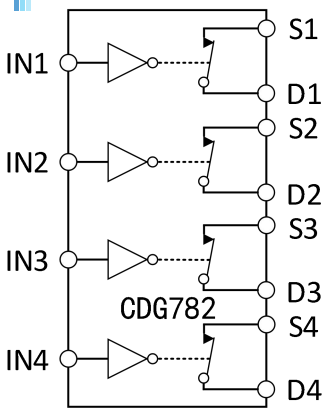


Figure 3. CDG721

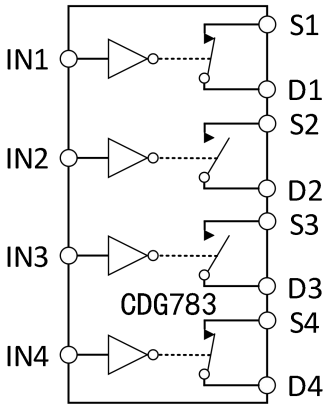


Figure 4. CDG723

Switches shown for a logic "0" input

Truth Table(CDG781/CDG782)

CDG711 In	CDG712 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table(CDG783)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs1	−0.3 V to VDD + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA
Continuous Current, S or D	30mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
QFN Package	
θ_{JA} Thermal Impedance	32°C/W
Lead Temperature, Soldering Vapor Phase(60 sec)	300°C
IR Reflow, Peak Temperature (<20sec)	235°C
ESD	2kV

Electrical Characteristics

VDD = +5 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			-40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	2.5	4	--	--	4.5	V_S=0V to V_{DD}, I_S=−10mA;See Figure 8	Ω

On Resistance Match Between Channels (ΔR_{ON})				--	0.05	0.3	V_S=0 V to V_{DD}, I_S=−10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	0.5	--	--	--	1.0	V_S=0 V to V_{DD}, I_S=−10mA	Ω
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.2	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 10	nA
Drain Off Leakage ID (Off)	--	± 0.01	±0.1	--	--	±0.2	V_S=4.5V/1V, V_D=1V/4.5V;See Figure 10	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±0.2	V_S=V_D=1V, or 4.5V;See Figure 9	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	11	--	--	--	16	R_L=300Ω,C_L=35pF,V_S=3V	ns
t_{OFF}	--	6	--	--	--	10	R_L=300Ω,C_L=35pF,V_S=3V	ns
Break-Before-Make Time Delay, t_D (CDG713 Only)	--	6	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=3V;	ns
Charge Injection	--	3	--				V_S=2V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-58	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-78	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-90	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
Bandwidth −3 dB	--	200	--				R_L=50Ω, C_L=5pF;	MHz
C_S	--	10	--					pF
C_D	--	10	--					pF
C_D, C_S (On)	--	22	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+5.5V, Digital inputs=0V or 5V	μA

VDD = +3 V±10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		

Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	5	--	--	5.5	8	V_S=0V to V_{DD}, I_S=−10mA;See Figure 8	Ω
On Resistance Match Between Channels (ΔR_{ON})	--	0.1	--	--	--	--	V_S=0 V to V_{DD}, I_S=−10mA	Ω
On Resistance Flatness (RFLAT(ON))	--	--	--	--	2.5	--	V_S=0 V to V_{DD}, I_S=−10mA	Ω
Leakage Currents							V_{DD}=+3.3V	
Source Off Leakage I_S (Off)	--	± 0.01	±0.1	--	--	±0.2	V_S=3V/1V, V_D=1V/3V;See Figure 10	nA
Drain Off Leakage ID (Off)	--	± 0.01	±0.1	--	--	±0.2	V_S=3V/1V, V_D=1V/3V;See Figure 10	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	±0.1	--	--	±0.2	V_S=V_D=1V, or 3V;See Figure 9	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.0	--	--		V
Input Low Voltage, V_{INL}				--	--	0.4		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	13	--	--	--	20	R_L=300Ω,C_L=35pF,V_S=2V	ns
t_{OFF}	--	7	--	--	--	12	R_L=300Ω,C_L=35pF,V_S=2V	ns
Break-Before-Make Time Delay, t_D (CDG713 Only)	--	7	--	1	--	--	R_L=300 Ω,C_L=35pF,V_{S1}=V_{S2}=2V;	ns
Charge Injection	--	3	--				V_S=1.5V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-58	--				R_L=50Ω, C_L=5pF, f=10MHz	dB
	--	-78	--				R_L=50Ω, C_L=5pF, f=1MHz	dB
Channel-to-Channel Crosstalk	--	-90	--				R_L=50Ω, C_L=5pF, f=10MHz;	dB
Bandwidth −3 dB	--	200	--				R_L=50Ω, C_L=5pF;	MHz
C_S	--	10	--					pF
C_D	--	10	--					pF
C_D, C_S (On)	--	22	--					pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+3.3V, Digital inputs=0V or 3V	μA

Typical Characteristics

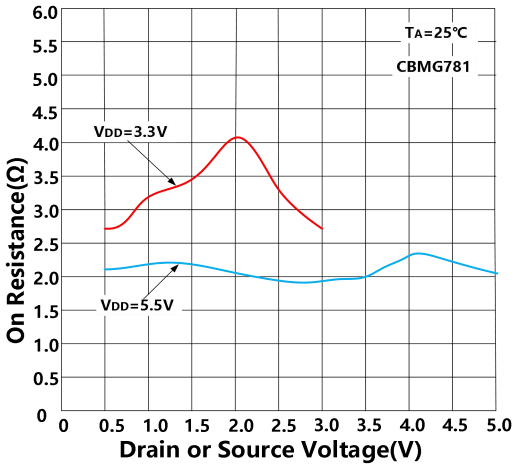


Figure 5.On Resistance vs. V_D (V_S)-(CDG781)

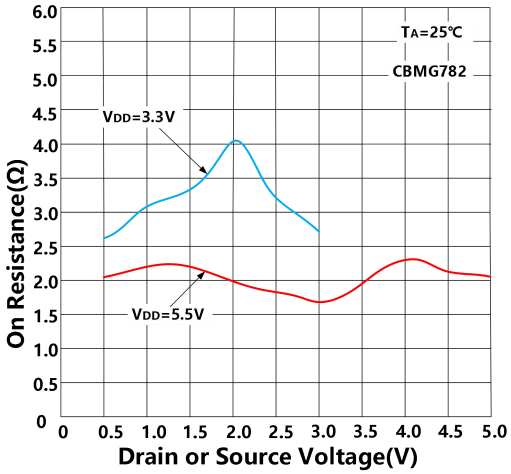


Figure 6.On Resistance vs. V_D (V_S)-(CDG782)

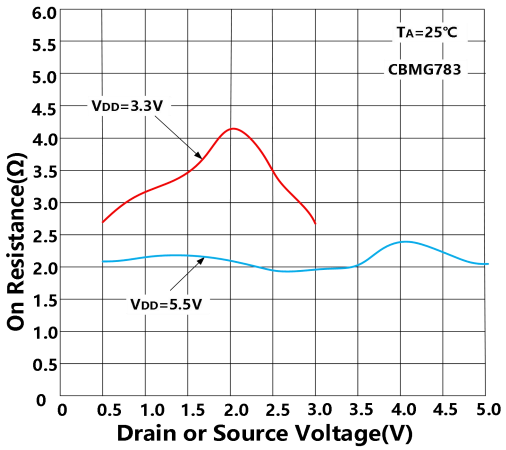
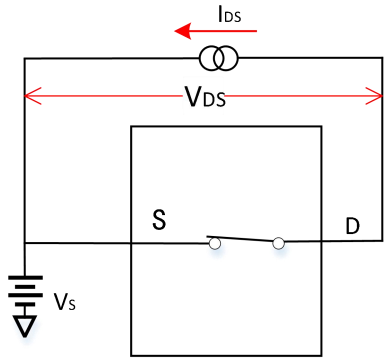


Figure 7.On Resistance vs. V_D (V_S)-(CDG783)

Chinese version:CDG781_CDG782_CDG783

Test Circuit



RON=V_{DS}/I_{DS}

Figure 8. On Resistance

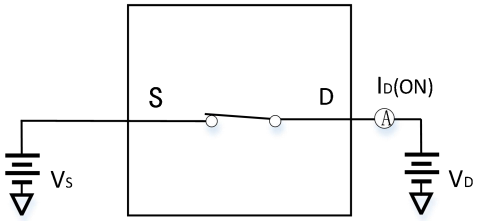


Figure 9. On Leakage

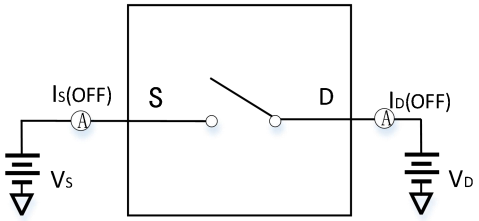


Figure 10. Off Leakage

Chinese version:CDG781_CDG782_CDG783

Package Outline Dimensions

QFN20

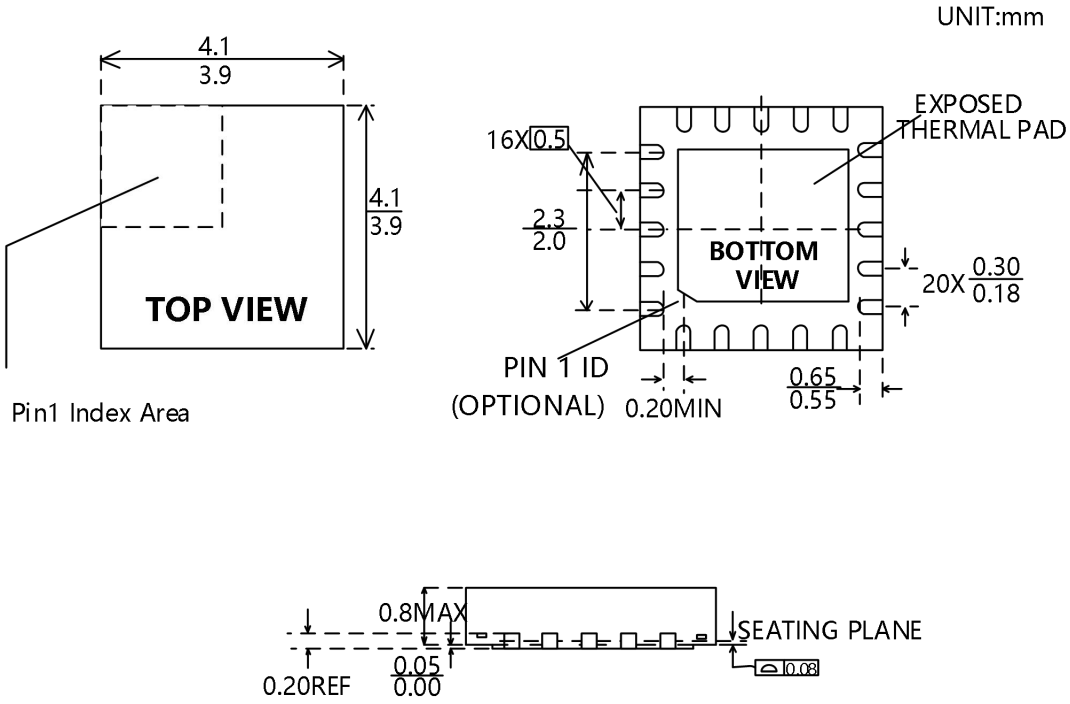


Figure 11. 20-Lead Lead Frame Chip Scale Package(QFN)

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDG781AQF20	-40℃~85℃	QFN-20	Tape and Reel, 3000
CDG782AQF20	-40℃~85℃	QFN-20	Tape and Reel, 3000
CDG783AQF20	-40℃~85℃	QFN-20	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.18	Initial version	Regular update	WW	LYL	