CoreadDvices
承芯微电子

CD1302

Trickle-Charge Timekeeping Chip

Version: Rev 1.0.0 Date: 2025-6-25

Features

- Completely Manages All Timekeeping Functions.Real-Time Clock Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
  31 x 8 Battery-Backed General-Purpose RAM
- Simple Serial Port Interfaces to Most Microcontrollers.Simple 3-Wire Interface
TTL-Compatible (V_{CC} = 5V)
- Low Power Operation Extends Battery Backup Run Time 2.0V to 5.5V Full Operation
- Uses Less Than 300nA at 2.0V
- 8-Pin SOP Package
- Optional Industrial Temperature Range: -40°C to +85°C Supports Operation in a Wide Range of Applications

Application

- Computers
- Communication equipment
- Industrial control systems, and embedded systems

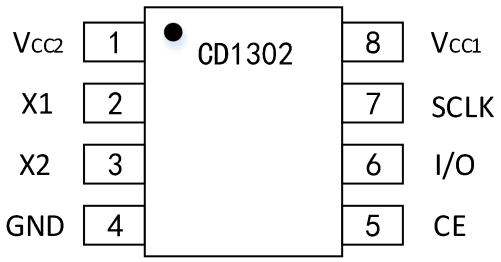
Description

The CD1302 trickle-charge timekeeping chip contains a real-time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Interfacing the CD1302 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: CE, I/O (data line), and SCLK (serial clock). Data can be transferred to and from the clock/RAM 1 byte at a time or in a burst of up to 31 bytes. The CD1302 is designed to operate on very low power and retain data and clock information on less than 1μW. The CD1302 has the additional features of dual power pins for primary and backup power supplies, programmable trickle charger for VCC1, and seven additional bytes of scratchpad memory.

Contents

Chinese version:CD1302

Pin Configurations

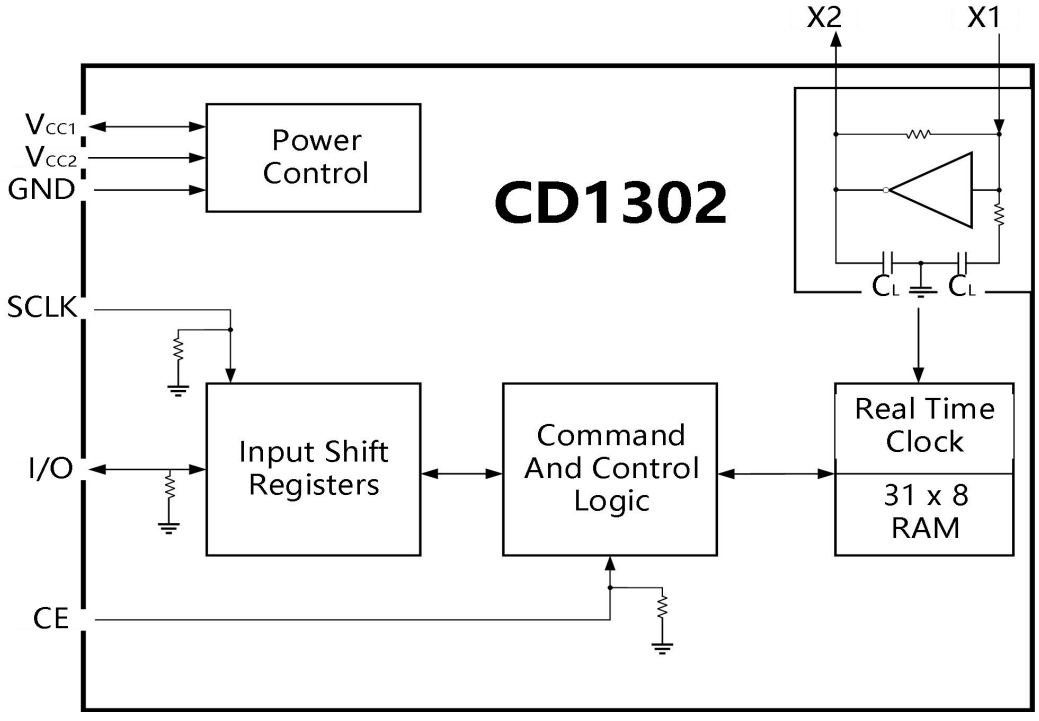


Pin Description

Pin	Symbol	I/O	Pin Description
1	V_{CC2}	In	Primary Power-Supply Pin in Dual Supply Configuration. V_{CC1} is connected to a backup source to maintain the time and date in the absence of primary power. The CD1302 operates from the larger of V_{CC1} or V_{CC2}. When V_{CC2} is greater than V_{CC1} + 0.2V, V_{CC2} powers the CD1302. When V_{CC2} is less than V_{CC1}, V_{CC1} powers the CD1302.
2	X1	In	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. For more information on crystal selection and crystal layout considerations, refer to Application Note 58: Crystal Considerations for Dallas Real-Time Clocks. The CD1302 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
3	X2	In	
4	GND	In	Ground pin
5	CE	In/Out	Input. CE signal must be asserted high during a read or a write. This pin has an internal 40kΩ (typ) pulldown resistor to ground. Note: Previous data sheet revisions referred to CE as RST. The functionality of the pin has not changed.
6	I/O	In	Input/Push-Pull Output. The I/O pin is the bidirectional data

			pin for the 3-wire interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
7	SCLK	Out	Input. SCLK is used to synchronize data movement on the serial interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
8	V_{CC1}	In	Low-Power Operation in Single Supply and Battery-Operated Systems and LowPower Battery Backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin. UL recognized to ensure against reverse charging current when used with a lithium battery.

Functional Block diagram



Operating Temperatures Range

Operating temperatures range of the microcircuit CD1302: T_A = - 40 ~ + 85℃.

RECOMMENDED DC OPERATING CONDITION and ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Recommended Operating Condition		Absolute Maximum Rating		Unit
		min	max	min	max	
Supply voltage V_{CC1},V_{CC2}	V_{CC1},V_{CC2}	2.0	5.5	-0.5	7.0	V
Low level input voltage	V_{IL}(V_{CC}=2V)	-0.3	0.3	--	--	--
	V_{IL}(V_{CC}=5V)	-0.3	0.8	--	--	--
High level input voltage	V_{IH}	2.0	V_{CC}+0.3	--	--	--
Storage temperature	T_S	--	--	-55	+125	℃
Soldering Temperature(leads, 10 seconds)	S_T	--	--	--	260	℃
Operating Temperature Range, Industrial	O_{TR}	--	--	-40	85	℃

DC Electrical Characteristics

(Unless otherwise specified,T_A=–40~+85℃)

Parameter	Symbol	Conditions				Unit
			Min		Max	
Input leakage current	I_{LI}	CE, SCLK, and I/O all have 40kΩ pulldown resistors to ground.T_A=25℃	--	86	500	μA
In / Out leakage current,	I_{LO}		--	86	500	
Logic 1 Output (I_{OH} = -0.4mA)	V_{OH}(V_{CC}=2V)	All voltages are referenced to ground.	1.6	--	--	V
Logic 1 Output (I_{OH} = -1.0mA)	V_{OH}(V_{CC}=5V)		2.4	--	--	
Logic 0 Output (I_{OL} = 1.5mA)	V_{OL}(V_{CC}=2V)	All voltages are referenced to ground.	--	--	0.4	V
Logic 0 Output (I_{OL} = 4.0mA)	V_{OL}(V_{CC}=5V)		--	--	0.4	

Active Supply Current (Oscillator Enabled)	$I_{CC1A}(V_{CC1}=2V)$	CH=0,V_{CC2} = 0V. I_{CC1A} and I_{CC2A} are specified with the I/O pin open, CE high, SCLK = 2MHz at V_{CC} = 5V; SCLK = 500kHz, V_{CC} = 2.0V.	--	--	0.4	mA
	$I_{CC1A}(V_{CC1}=5V)$		--	--	1.2	
Timekeeping Current (Oscillator Enabled)	$I_{CC1T}(V_{CC1}=2V)$	T_A=25℃.CH=0,V_{CC2} = 0V. I_{CC1T} and I_{CC2T} are specified with I/O open, CE and SCLK set to a logic 0.	--	0.2	0.3	μA
	$I_{CC1T}(V_{CC1}=5V)$		--	0.45	1	
Standby Current (Oscillator Disabled)	$I_{CC1S}(V_{CC1}=2V)$	CH=1,I_{CC1S} and I_{CC2S} are specified with CE, I/O, and SCLK open. V_{CC2} = 0V. T_A=25℃	--	1	100	nA
	$I_{CC1S}(V_{CC1}=5V)$		--	1	100	
	IND		--	5	200	
Active Supply Current (Oscillator Enabled)	$I_{CC2A}(V_{CC1}=2V)$	CH=0,V_{CC2} = 0V. I_{CC1A} and I_{CC2A} are specified with the I/O pin open, CE high, SCLK = 2MHz at V_{CC} = 5V; SCLK = 500kHz, V_{CC} = 2.0V.	--		0.425	mA
	$I_{CC2A}(V_{CC1}=5V)$		--	--	1.28	
Timekeeping Current (Oscillator Enabled)	$I_{CC2T}(V_{CC1}=2V)$	CH=0,V_{CC1} = 0V. I_{CC1T} and I_{CC2T} are specified with I/O open, CE and SCLK set to a logic 0.	--	--	25.3	μA
	$I_{CC2T}(V_{CC1}=5V)$		--	--	81	
Standby Current (Oscillator Disabled)	$I_{CC2S}(V_{CC1}=2V)$	CH=1,V_{CC1} = 0V. I_{CC1S} and I_{CC2S} are specified with CE, I/O, and SCLK open.	--	--	25	μA
	$I_{CC2S}(V_{CC1}=5V)$	--	--	--	80	
Trickle-Charge Resistors	R1	--	--	2	--	kΩ
	R2	--	--	4	--	
	R3	--	--	8	--	
Trickle-Charge Diode Voltage Drop	V_{TD}	--	--	0.7	--	V

Capacitance(T_A=25℃)

Parameter	Symbol	Min	Typ	Max	Units

Input Capacitance	C_I	--	10	--	pF
I/O Capacitance	$C_{I/O}$	--	15	--	pF

AC Electrical Characteristics

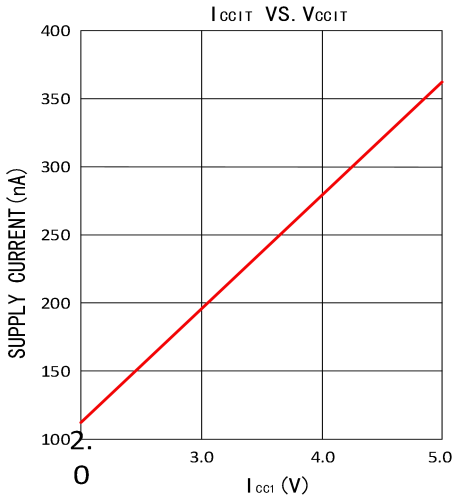
(T_A = 0°C to +70°C or T_A = -40°C to +85°C.)

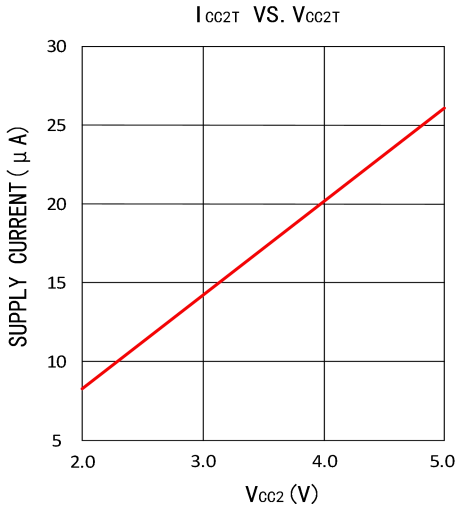
Parameter	Symbol		Conditions	Min	Max	Unit
Data to CLK Setup	t_{DC}	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.	200	--	ns
		V_{CC}=5V		50	--	ns
CLK to Data Hold	t_{CDH}	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.	280	--	ns
		V_{CC}=5V		70	--	ns
CLK to Data Delay	t_{CDD}	VCC=2V	Measured at VIH = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.Measured at V_{OH} = 2.4V or V_{OL} = 0.4V. Load capacitance = 50pF.	--	800	ns
		V_{CC}=5V		--	200	ns
CLK Low Time	t_{CL}	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.	1000	--	ns
		V_{CC}=5V		250	--	ns
CLK High Time	t_{CH}	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.	1000	--	ns
		V_{CC}=5V		250	--	ns
CLK Frequency	t_{CLK}	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.	--	0.5	MHz
		V_{CC}=5V		DC	2	
CLK Rise and Fall	t_R, t_F	V_{CC}=2V		--	2000	ns
		V_{CC}=5V		--	500	
CE to CLK Setup	t_{CC}	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.	4	--	μs
		V_{CC}=5V		1	--	
CLK to CE Hold	t_{CCH}	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum	240	--	ns

		V_{CC}=5V	rise and fall time.	60	--	
CE Inactive Time	t_{CWH}	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.	4	--	μs
		V_{CC}=5V		1	--	
CE to I/O High Impedance	tCDZ	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.	--	280	ns
		V_{CC}=5V		--	70	ns
SCLK to I/O High Impedance	t_{CCZ}	V_{CC}=2V	Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.	--	280	ns
		V_{CC}=5V		--	70	ns

Typical Operation Characteristics

(V_{CC}=5.0V,T_A=+25℃,unless otherwise noted)





Application Note

OSCILLATOR CIRCUIT

The CD1302 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 1 shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.

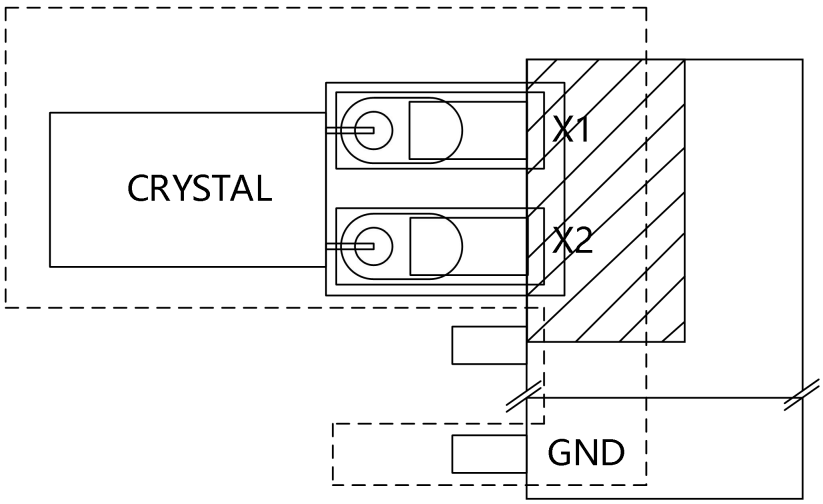
CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast. Figure 2 shows a typical PC board layout for isolating the crystal and oscillator from noise.

Table 1. Crystal Specifications*

Parameter	Symbol				Unit
		Min		Max	
Nominal Frequency	f_O	--	32.768	--	kHz
Series Resistance	ESR	--	--	45	kΩ
Load Capacitance	C_L	--	6	--	pF

Figure 2. Typical PC Board Layout for Crystal



COMMAND BYTE

Figure 3 shows the command byte. A command byte initiates each data transfer. The MSB (bit 7) must be a logic 1. If it is 0, writes to the CD1302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 to 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

Figure 3. Address/Command Byte

7	6	5	4	3	2	1	0
1	RAM	A4	A3	A2	A1	A0	RD
	CK						WR

CE AND CLOCK CONTROL

Driving the CE input high initiates all data transfers. The CE input serves two functions. First, CE turns on the control logic that allows access to the shift register for the address/command sequence. Second, the CE signal provides a method of terminating either single-byte or multiple-byte CE data transfer.

A clock cycle is a sequence of a rising edge followed by a falling edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the CE input is low, all data transfer terminates and the I/O pin goes to a high-impedance state. Figure 4 shows data transfer. At power-up, CE must be a logic 0 until VCC > 2.0V. Also, SCLK must be at a logic 0 when CE is driven to a logic 1 state.

DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as CE remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri-stated upon each rising edge of SCLK. Data is output starting with bit 0.

BURST MODE

Burst mode can be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits 1 through 5 = logic 1). As before, bit 6 specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit 0 of address 0. When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. However, when writing to RAM in burst mode it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 31 bytes are written or not.

CLOCK/CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. Table 3 illustrates the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format.

The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.). Illogical time and date entries result in undefined operation. When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update.

When reading the time and date registers, the user buffers are synchronized to the internal registers the rising edge of CE.

The countdown chain is reset whenever the seconds register is written. Write transfers occur on the falling edge of CE. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within 1 second.

The CD1302 can be run in either 12-hour or 24-hour mode. Bit 7 of the hours register is defined as the 12- or 24- hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours). The hours data must be re-initialized whenever the 12/24 bit is changed.

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt (CH) flag. When this bit is set to logic 1, the clock oscillator is stopped and the CD1302 is placed into a low-power standby mode with a current drain of less than 100nA. When this bit is written to logic 0, the clock will start. The initial power-on state is not defined.

WRITE-PROTECT BIT

Bit 7 of the control register is the write-protect bit. The first seven bits (bits 0 to 6) are forced to 0 and always read 0 when read. Before any write operation to the clock or RAM, bit 7 must be 0. When high, the write-protect bit prevents a write operation to any other register. The initial power-on state is not defined. Therefore, the WP bit should be cleared before attempting to write to the device.

TRICKLE-CHARGE REGISTER

This register controls the trickle-charge characteristics of the CD1302. The simplified schematic of Figure 5 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern of 1010 enables the

trickle charger. All other patterns will disable the trickle charger. The CD1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2 and 3) select whether one diode or two diodes are connected between V_{CC2} and V_{CC1}. If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independently of TCS. The RS bits (bits 0 and 1) select the resistor that is connected between V_{CC2} and V_{CC1}. The resistor and diodes are selected by the RS and DS bits as shown in Table 2.

Table 2. Trickle Charger Resistor and Diode Select

TCS BIT7	TCS BIT6	TCS BIT5	TCS BIT4	TCS BIT3	TCS BIT2	TCS BIT1	TCS BIT0	Function
X	X	X	X	X	X	0	0	Disabled
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
1	0	1	0	0	1	0	1	1 Diode, 2kΩ
1	0	1	0	0	1	1	0	1 Diode, 4kΩ
1	0	1	0	0	1	1	1	1 Diode, 8kΩ
1	0	1	0	1	0	0	1	2 Diode, 2kΩ
1	0	1	0	1	0	1	0	2 Diode, 4kΩ
1	0	1	0	1	0	1	1	2 Diode, 8kΩ
0	1	0	1	1	1	0	0	Initial power-on state

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to VCC2 and a super cap is

connected to VCC1. Also assume that the trickle charger has been enabled with one diode and resistor R1 between VCC2 and VCC1. The maximum current IMAX would therefore be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.7V) / 2k\Omega \approx 2.2mA$$

As the super cap charges, the voltage drop between VCC2 and VCC1 decreases and therefore the charge current decreases.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode, the first eight clock/calendar registers can be consecutively read or written (see Table 3) starting with bit 0 of address 0. If the write-protect bit is set high when a write clock/calendar burst mode is specified, no data transfer will occur to any of the eight clock/calendar registers (this includes the control register). The trickle charger is not accessible in burst mode.

At the beginning of a clock burst read, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

RAM

The static RAM is 31 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written (see Table 3) starting with bit 0 of address 0.

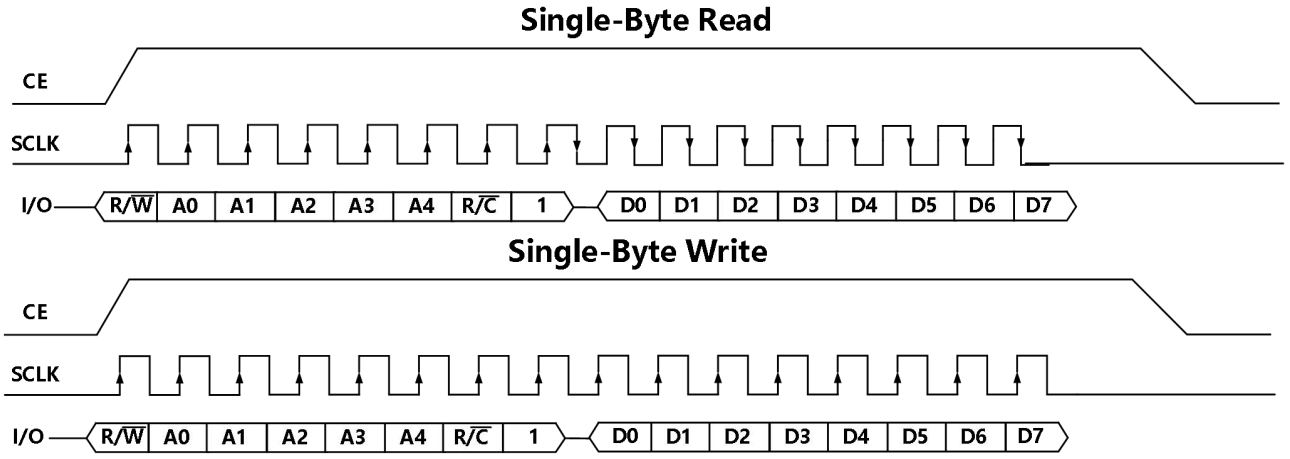
REGISTER SUMMARY

A register data format summary is shown in Table 3.

CRYSTAL SELECTION

A 32.768kHz crystal can be directly connected to the CD1302 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (C_L) of 6pF. For more information on crystal selection and crystal layout consideration, refer to *Application Note 58: Crystal Considerations for Dallas Real-Time Clocks*.

Figure 4. Data Transfer Summary



NOTE: IN BURST MODE, CE IS KEPT HIGH AND ADDITIONAL SCLK CYCLES ARE SENT UNTIL THE END OF THE BURST.

Table 3. Register Address/Definition

RTC

Read	Write	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Range
81h	80h	CH	10 Seconds			Seconds				00-59
83h	82h		10 Minutes			Minutes				00-59
85h	84h	12/24	0	10 AM/PM	Hour	Hour				1-12/0-23
87h	86h	0	0	10 Date		Date				1-31
89h	88h	0	0	0	10 Month	Month				1-12
8Bh	8Ah	0	0	0	0	0	Day			1-7
8Dh	8Ch	10 Year				Year				00-99
8Fh	8Eh	WP	0	0	0	0	0	0	0	--
91h	90h	TCS	TCS	TCS	TCS	DS	DS	RS	RS	--

CLOCK BURST

BFh	BEh

RAM

C1h			00-FFh
C3h			00-FFh

C5h			00-FFh
. . .	. . .		. . .
FDh	FCh		00-FFh

RAM BURST

FFh	FEh

Figure 5. Programmable Trickle Charger

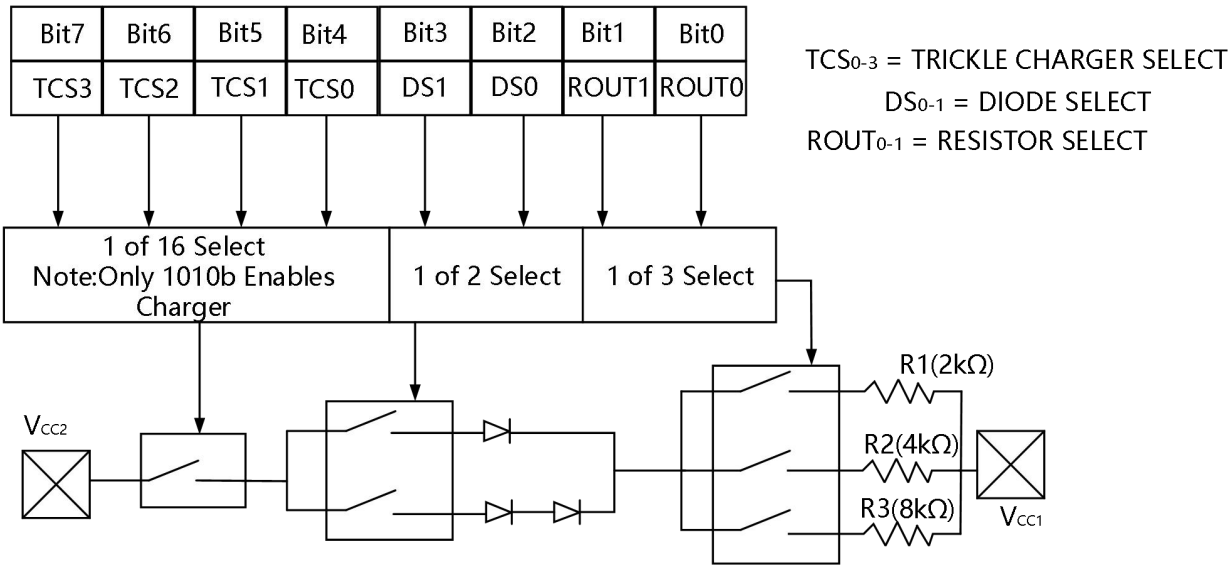


Figure 6. Timing Diagram: Read Data Transfer

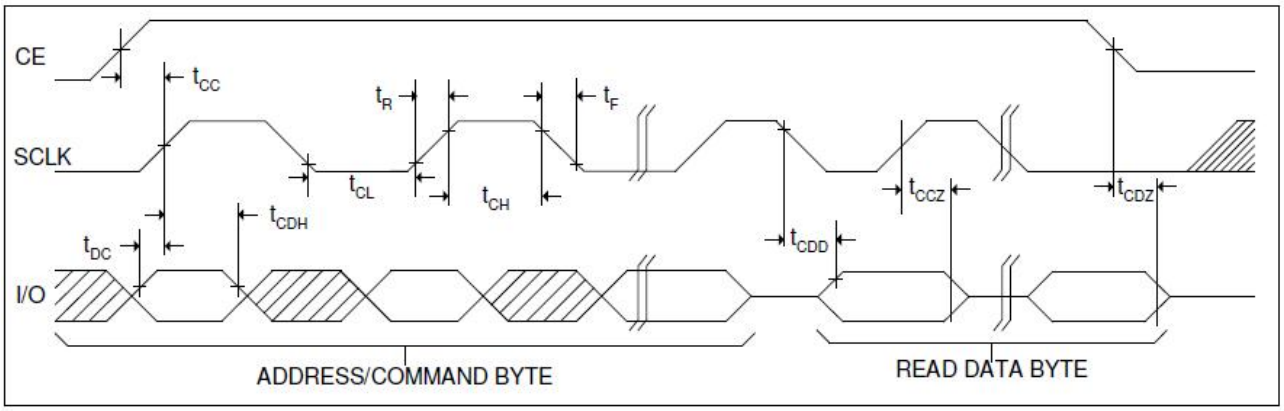
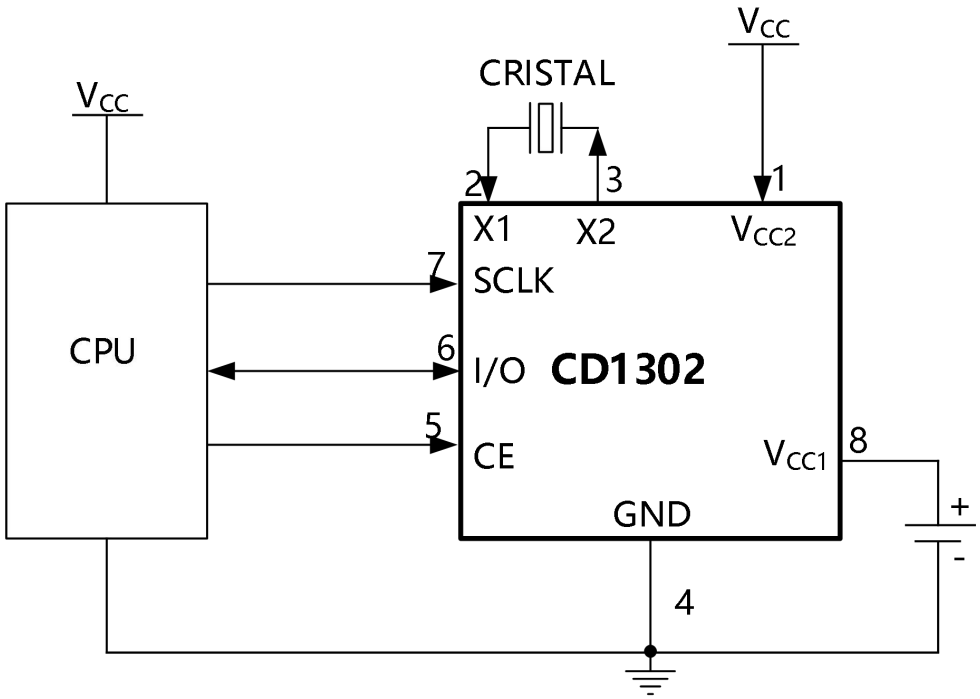


Figure 7. Timing Diagram: Write Data Transfer

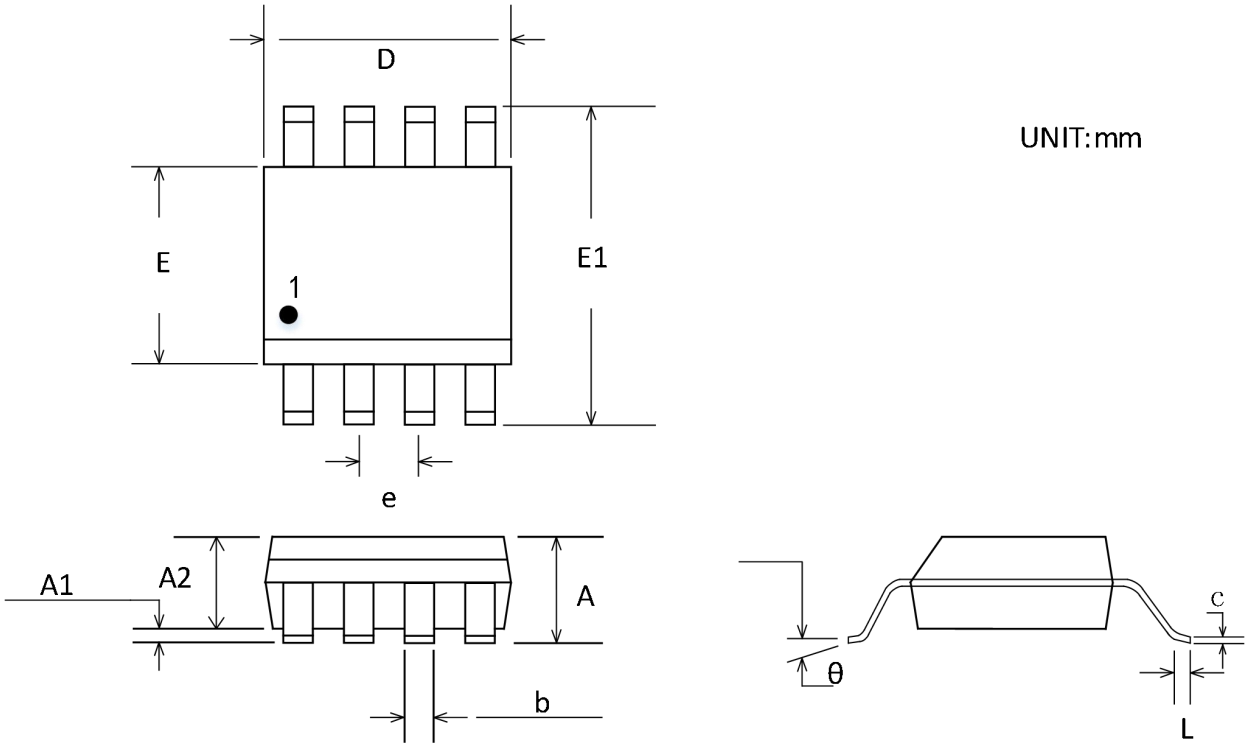
Typical Application Circuit



Chinese version:CD1302

Package Outline Dimensions

SOP-8



UNIT:mm

Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Chinese version:CD1302

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD1302AS8	-40℃ ~ 85℃	SOP-8	Tape and Reel, 2500
CD1302AS8-RL	-40℃ ~ 85℃	SOP-8	Tape and Reel, 3000
CD1302AS8-REEL	-40℃ ~ 85℃	SOP-8	Tape and Reel, 4000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.25	Initial version	Regular update	WW	LYL	

Chinese version:CD1302