CoreadDvices
承芯微电子

CD1307

64 x 8, Serial, I2C Real-Time Clock

Version: Rev 1.0.0 Date: 2025-6-18

Features

- Counts seconds, minutes, hours, days of the week, dates, months, and years, taking leap years into account (before the year 2100);
- Provides 56 bytes of random access memory with self - managed capabilities for date storage;
- Features an I2C interface, supporting a standard speed of 100KHz and a high speed of 400KHz;
- Offers a programmable rectangular output signal;
- Monitors the main power supply and backup power supply and enables automatic switching;
- Consumes less than 500nA of supply current in the battery backup power supply mode;
- Operates within a temperature range of -40°C to +85°C for industrial applications;

Application

- Computers
- Communication equipment
- Industrial control systems, and embedded systems

Description

The CD1307 is a binary-coded decimal (BCD) digital clock with a date function. It comes with an additional 56 bytes of self-managed static random access memory (SRAM) and features low power consumption. The memory space can be read from and written to via the I2C interface. The timing circuit is used to calculate the real-time in hours, minutes, and seconds, as well as the

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day of the week, date, month, and year. The last day of each month is automatically adjusted according to whether the month has 31 days or fewer, including leap year corrections. The clock can operate in either the 24-hour format or the 12-hour format with AM/PM indication.
The CD1307 has a built-in power control circuit. This circuit can detect a power supply interruption and automatically switch the device to the battery-powered mode.

Contents

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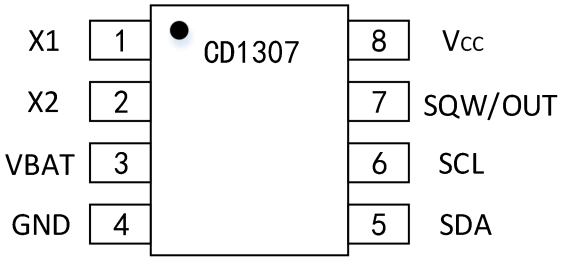
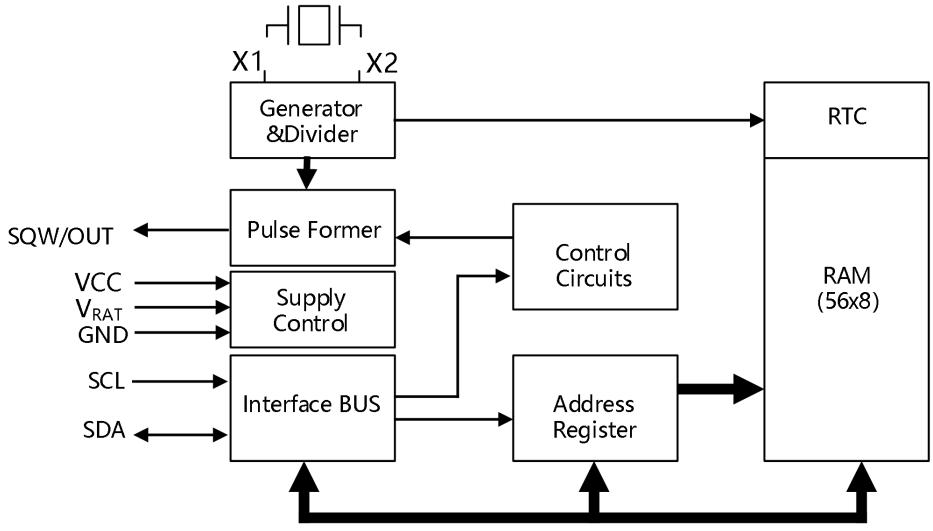
Pin Configurations



Pin Assignment

Pin	Symbol	I/O	Pin Description
1	X1	In	Pin for connection of the quartz resonator
2	X2	In	Pin for connection of the quartz resonator
3	VBAT	In	Pin for battery
4	GND	In	Ground pin
5	SDA	In/Out	Input / output of serial data
6	SCL	In	Input of the consecutive cycle signal
7	SQW/OUT	Out	Output of rectangular signal
8	V_{CC}	In	Power supply pin

Functional Block diagram



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Operating Temperatures Range

Operating temperatures range of the microcircuit CD1307: T_A = - 40 ~ + 85℃.

RECOMMENDED DC OPERATING CONDITION and ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Recommended Operating Condition		Absolute Maximum Rating		Unit
		min	max	min	max	
Supply voltage	V_{CC}	4.5	5.5	-0.5	7.0	V
Battery voltage	V_{BAT}	2.0	3.5	-0.5	7.0	V
Low level input voltage	V_{IL}	-0.3	0.8	-0.5	7.0	V
High level input voltage	V_{IH}	2.2	V_{CC}+0.3	-0.5	7.0	V
Storage temperature	T_S	-	-	-55	+125	℃

DC Electrical Characteristics

(T_A=–40~+85℃, V_{CC}= 4.5–5.5V)

Parameter	Symbol	Mode			Unit
			Min	Max	
Input leakage current, (SCL only)	I_{LI}		-	1	uA
In / Out leakage current, (SDA and SQW/OUT)	I_{LO}		-	1	uA
Low level output voltage	V_{LO} 1)	V_{CC} = 4.5 V	-	0.4	V
Consumption current in the data transfer mode	I_{CCA}	F_{SCL} = 100 kHz	-	1500	µA
Consumption current in the static mode	I_{CCS}	V_{CC} = 5 V and SDA, SCL = 5 V	-	200	µA
Consumption current in the battery mode (SQW/OUT OFF., 32 kHz – ON)	I_{BAT1}	V_{CC} = 0 V, V_{BAT} = 3 V	-	0.5	µA
Consumption current in the battery mode (SQW/OUT – ON, 32 kHz – ON)	I_{BAT2}	V_{CC} = 0 V, V_{BAT} = 3 V	-	0.8	µA

Low level voltage is determined under the load current of 5mA; VOL = GND under the capacitance load

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AC Electrical Characteristics

(T_A=−40~+85℃,V_{CC}=4.5–5.5V)

Parameter	Symbol	Mode			Unit
			Min	Max	
Cycle frequency SCL	F_{SCL}	-	0	100	kHz
Time of the bus vacant status between the statuses of STOP and START	T_{BUF}	-	4.7	-	μs
Hold time (repeated) of START status	$T_{HD:STA}$ [1])	-	4.0	-	μs
Duration of the low status of the cycle pulse SCL	T_{LOW}	-	4.7	-	μs
Duration of the cycle pulse high status SCL	T_{HIGH}	-	4.0	-	μs
Pre-set time for the repeated status START	$T_{SU:STA}$	-	4.7	-	μs
Data hold time	2) $T_{HD:DAT}$	-	0	-	μs
Data pre-set time	$T_{SU:DAT}$	-	250	-	ns
Rise time of signals SDA and SCL	T_R	-	-	1000	ns
Drop time of signals SDA and SCL	T_F	-	-	300	ns
Pre-set time for the status STOP	$T_{SU:STO}$	-	4.7	-	ns
TotaL capacitance load per each bus line	C_B	-	-	400	pF
IN / OUT capacitance	$C_{I/O}$	-	10	10	pF
Load capacitance of the quartz resonator	CLX	-	12.5	12.5	pF

After this time interval the first time cycle signal is formed;

Device should internally ensure the hold time, at least, 300 nsec for the signal SDA (relative to VIHMIN of signal SCL) in order to overlap the indeterminancy area of the fall signal of SCL.

maximum value $t_{HD:DAT}$ should be definite in that case, if the device does not increase duration of

the low status (t_{LOW}) of signal SCL.

Typical Operation Characteristics

(V_{CC}=5.0V,T_A=+25℃,unless otherwise noted)

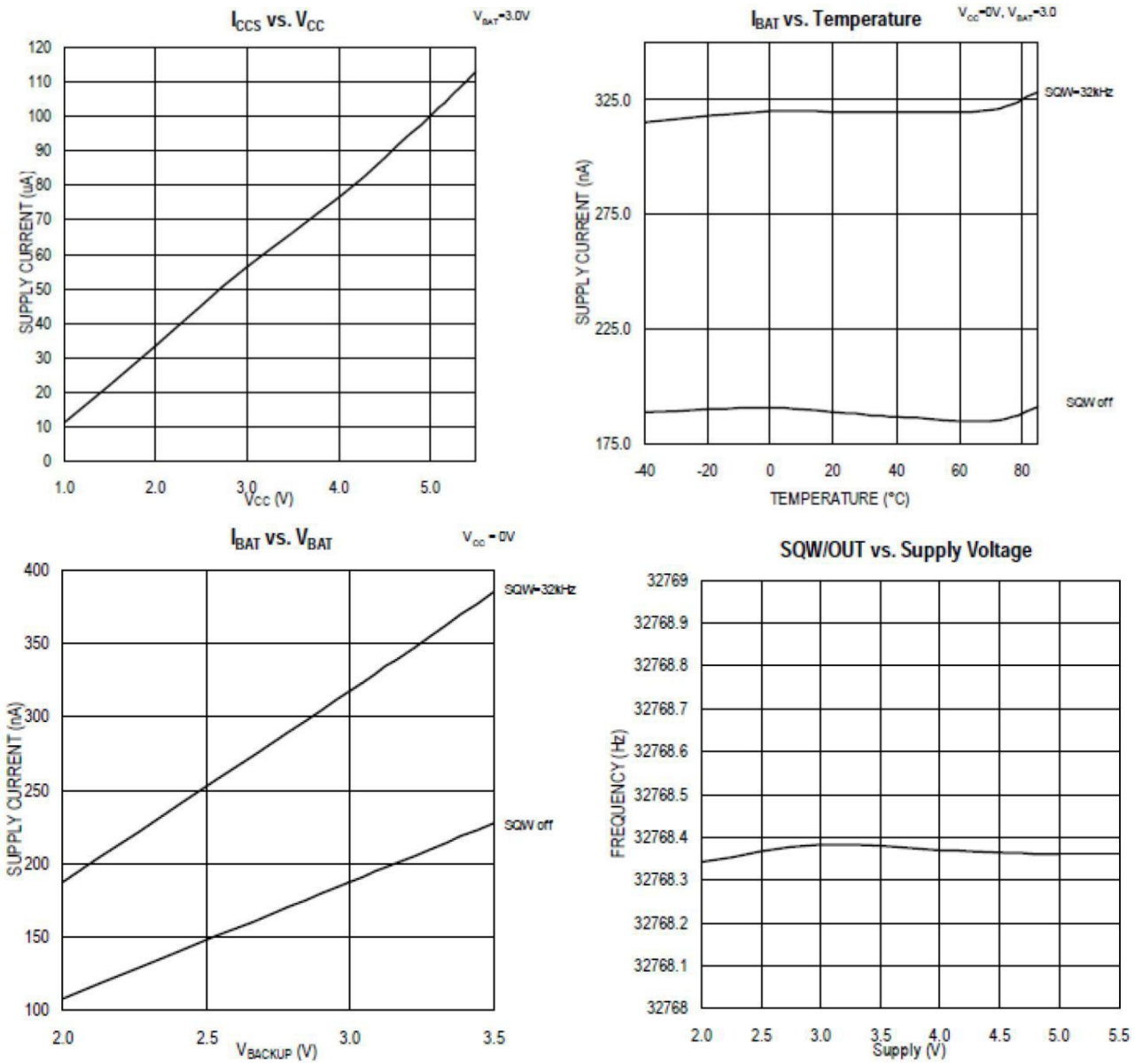
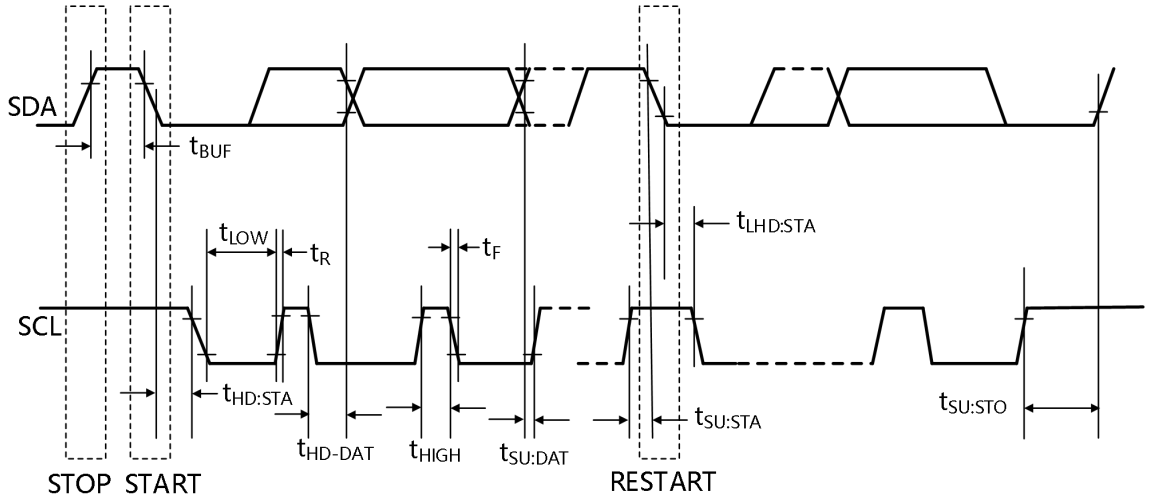


Figure 9. Inverting Regulator Ground Referenced Shutdown

Timing Chart



Functioning

CD1307 operates as the driven device on the serial bus. For access to it it is required to set the status START and to send after the register address the device identification code. It is possi-ble to address the next register consequently, until the status STOP is set. When V_{CC} drops below 1.25 x V_{BAT}, the access in progress to the device is ceased and the address counter is reset. At this time the device does not recognize the input data, excluding the erroneous information writing. When V_{CC} drops below V_{BAT}, the device switches over to the battery mode, consuming low power. When switching on the power supply V_{CC} above V_{BAT} + 0.2 V, the device switches over from the battery power supply to V_{CC}; and recognizes the input data, when VCC becomes above 1.25 x V_{BAT}.

Addresses Chart Of Rtc And Ram

00H	SECONDS
	MINUTES
	HOURS
	DAY
	DATE
	MONTH

Addresses chart of the registers RTC and RAM is indicated in the Figure. Hour registers of the real time are positioned at the addresses 00h – 07h. RAM registers are positioned at the ad-dresses of 08h –

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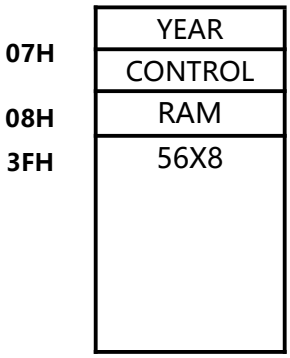

3Fh. In the mode of the multi-byte access, when reaching by the pointer of the address 3Fh, the end of the RAM address space, there happens transition to the register with the address 00h, beginning of the hours area.

Oscillator Circuit

CD1307 uses an external 32.768kHz crystal. The oscillator circuit does not require any exter-nal resistors or capacitors to operate. Table specifies several crystal parameters for the external crystal.

Crystal Specifications*

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_o		32.768		kHz
Series Resistance	ESR			45	kΩ
Load Capacitance	C_L		12.5		pF

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by tempera-ture shifts. External circuit noise coupled into the oscillator.

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Oscillator Circuit Showing Internal Bias Network

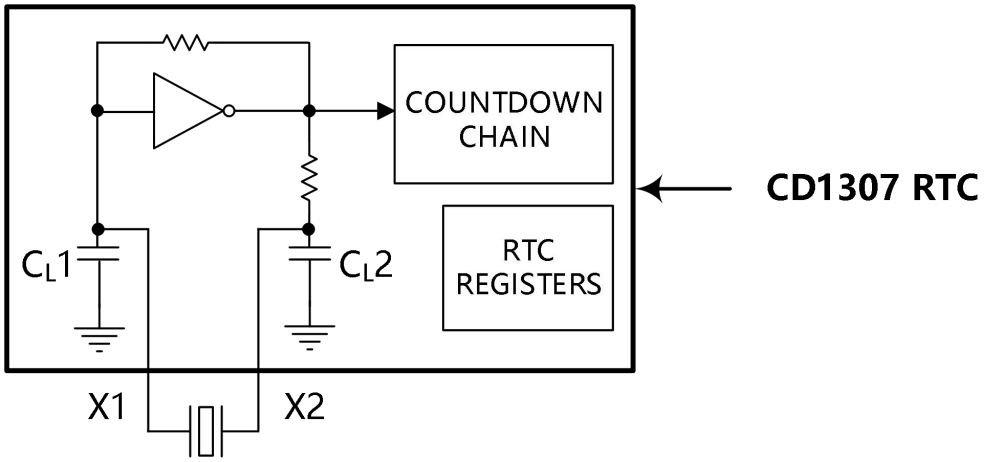
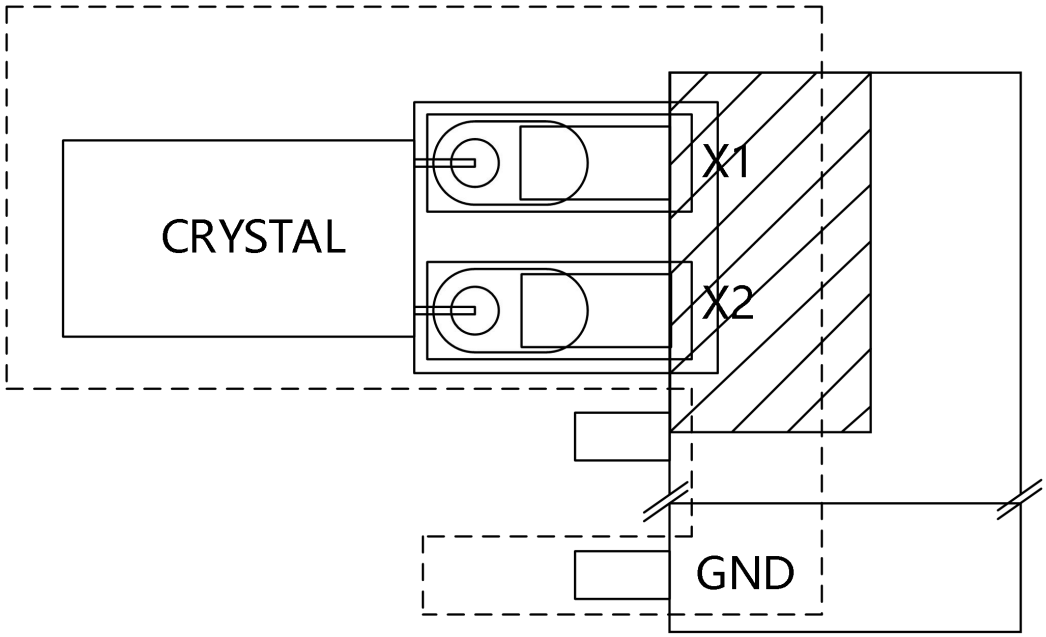


Figure shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.

Recommended Layout For Crystal



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Hours And Calendar

Information on the time and date is obtained by means of reading the appropriate register bytes. Hour registers of the real time are indicated in the Figure. Pre-setting and time and calendar initialization are performed by means of writing the appropriate bytes. Information, contained in the time and calendar registers, represents the binary-decimal code. Bit 7 of register 0 represents the hour stop bit (CH). When this bit is set to “1”, the generator is off.

When switching on the power supply, the initial status of all registers is not determined. It is necessary to enable the generator (bit CH = 0) when setting the initial configurations.

CD1307 operates in the 12-hour or in the 24-hour format. The bit 6 of the watch register de-termines the operational mode. 12-hour mode corresponds to the high level. In the 12-hour mode the bit 5 is the AM/PM bit. The high level corresponds to PM. In the 24-hour mode, the 5 is the second bit of tens of hours (20 -23 hours).

During application of the signal “START” to the two-wire bus there happens transfer of the real time to the auxiliary set of registers. The time data are read from these auxiliary registers, while the watch proceeds in operation. This eliminates the necessity of repeated reading in case of updating the basic registers in the access process.

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Registers RTC

	BIT7							BIT0	
00H	CH	2nd DIGIT of SECONDS			1st DIGIT of SECONDS				00-59
	X	2nd DIGIT of MINUTES			1st DIGIT of MINUTES				00-59
	X				1st DIGIT of HOURS				01-12 00-23
	X	X	X	X	X	DAY of WEEK			1-7
	X	X			1st DIGIT of DATE				01-28/29 01-30 01-31
	X	X	X		1st DIGIT of MONTH				01-12
					1st DIGIT of YEARS				00-99
07H	OUT	X	X	SQWE	X	X	RS1	RS0	

Control Register

Control register is used for control of pin SQW/OUT.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OUT	**X**	**X**	**SQWE**	**X**	**X**	**RS1**	**RS0**

OUT (output control): This bit presets the output logic level of the pin SQW/OUT, when the output of the rectangular signal is locked.

SQWE (rectangular signal enabling): This bit, pre-set to the logic “1”, activates the generator output. Frequency of the output rectangular signal is determined by the bits RS0 and RS1.

RS (frequency selection): These bits determine the frequency of the output rectangular signal, when the output of the rectangular signal is activated. The table indicates the frequencies, which can be selected by the bits RS.

RS1	RS0	Frequency SQW/OUT
0	0	1 Hz

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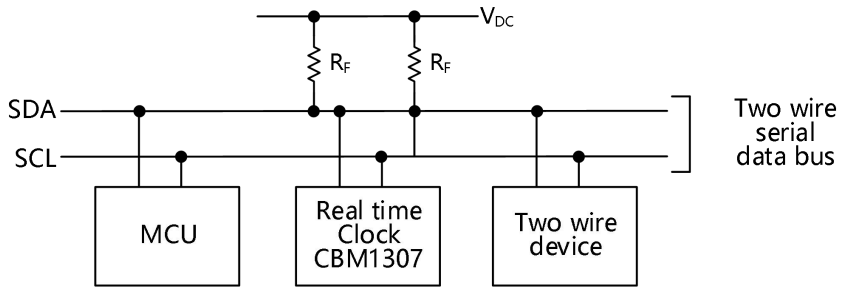
0	1	4,096 kHz
1	0	8,192 kHz
1	1	32,768 kHz

Two-Wire Serial Data Bus

CD1307 supports the bi-directional two-wire bus and the protocol of the data exchange. The bus can be controlled by the "master" device, which generates the cycle signal (SCL), controls ac-cess to the bus, generates the statuses START and STOP. Typical configuration of the bus with the two-wire protocol is indicated in Figure.



Data transfer can be initiated only when the bus is not occupied. In the process of the data transfer the data line should remain stable, while the line of the cycle signal is in the high status. Status alterations of the data line at that moment, when the cycle line is in the high status, will be regarded as the control signals.

In compliance with this the following conditions are determined:

Bus not occupied: both the data line and the cycle signal are in the HIGH status.

Data transfer start: Status alteration of the data line during transition from HIGH to LOW, while the cycle line is in the HIGH status, is determined as the status START.

Data transfer stop: Status alteration of the data line during transition from LOW to HIGH, while

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the cycle line is in the HIGH status, is determined as the status STOP.

Valid data: Data line status complies with the valid data, when after the status START the data line is stable during the HIGH status of the cycle signal. Data on the line should be altered at the time of the LOW status of the cycle signal. One cycle pulse per one data bit.

Each data transfer starts at the beginning of the status START and ceases at the beginning of the status STOP. Number of the data bytes, transferred between the statuses START and STOP is not limited and is determined by the «master» device. Information is transferred byte by byte, and each receipt is confirmed by the ninth byte. CD1307 operates in the normal mode only (100 kHz).

Confirmation of receipt: Each receiving device, when it being addressed, has to generate the recept confirmation after receiving each byte. «Master» device should generate the cycle pulses, which are allocated in compliance with the confirmation bits.

If the receipt confirmation signal is in the high status, then on arrival of the confirmation cycle pulse, the device, confirming the receipt, should switch over the SDA line to the low status. Of course, there should be considered the pre-set time and the hold time. The «master» device should signalize on completion of the data transfer to the "slave" device, ceasing generation of the confirmation bit on receiving the receipt confirmation from the "slave" cycle pulse. In this case, the «slave one should switch over the data line to the low status, in order to enable the «master» one generate the condition of STOP.

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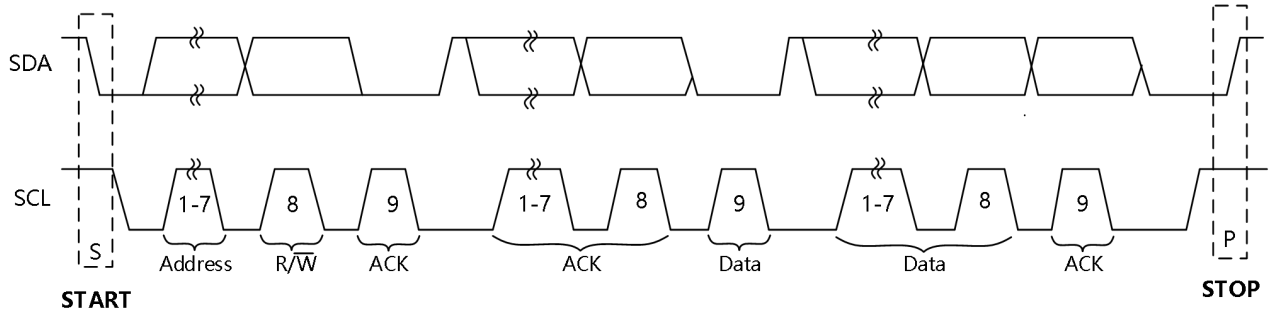
Data Transfer By The Serial Two-Wire Bus



Depending on the status of bit RF, there are possible two types of transfer:

1. Data are transferred from the «master» transmitter to the «slave» receiver.

The first byte, transmitted by the «master» one, is the address for the «slave» one. Then follows a sequence of the data bytes. The «slave» one returns the receipt confirmation bytes after each received byte. Order of the data transfer: the first is the most senior digit (MSB).

2. The data are transferred from the «slave» transmitter to the «master» receiver.

The first byte (address of «slave») is applied to the «master». Then the «master» returns the confirmation bit. This follows after the transfer by the «slave» of the data sequence. The «master» returns the receipt confirmation bit after each received byte, with the exception of the last byte. After receipt of the last byte the receipt confirmation bit is not returned.

The «master» device generates all cycle pulses and the statuses START and STOP. Transfer is completed at emergence of the status STOP or the repeated emergence of the status START. As the repeated status START is the beginning of the next serial transfer, the bus is not vacated.The data transfer order: the first is the most senior digit (MSB).

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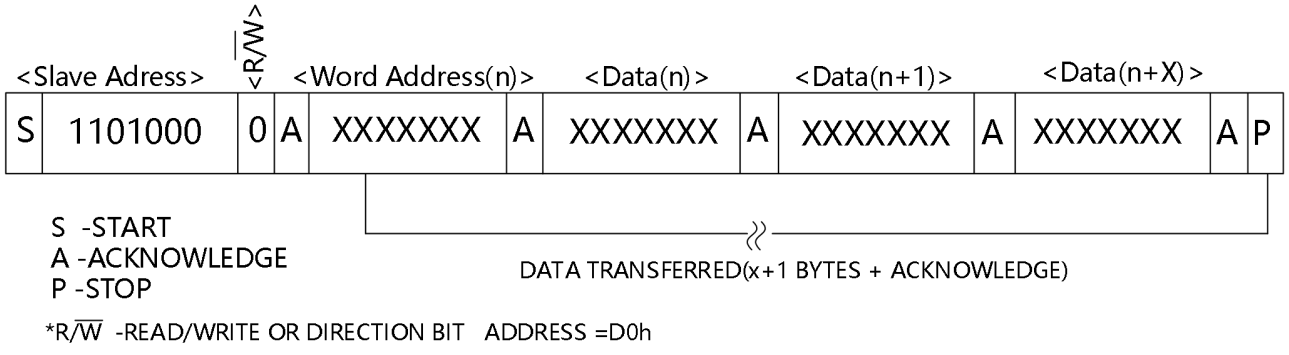
Two Following Modes

1. Mode of «slave» receiver (write mode of CD1307):

Serial data and cycles are received via SDA and SCL appropriately. After transfer of each byte the confirmation bit is sent. The statuses START and STOP are recognized as the beginning and the end of the serial transfer. The address recognition is performed by means of the hardware after receipt of the "slave" address and the direction bit. The address byte isthe first byte, received after occurrence of the START status, generated by the "master". The address byte contains the seven

address bits of CD1307, equal to 1101000, accompanied by the direction bit (R_F), which for write is equal to 0.After receipt and decoding of the address byte, DS1307 applies confirmation to the line SDA. After confirmation by CD1307 of the "slave" address and the write bit, the «master» sends the register address of CD1307. Thus the register indicator will be preset in CD1307. Then the «smart» shall start to send each data byte with the subsequent receipt confirmation of each byte. Upon completion of writing the "master" shall formulate the status STOP for termination of the data transfer.

Data Writing- Mode of << SLAVE>> Receiver

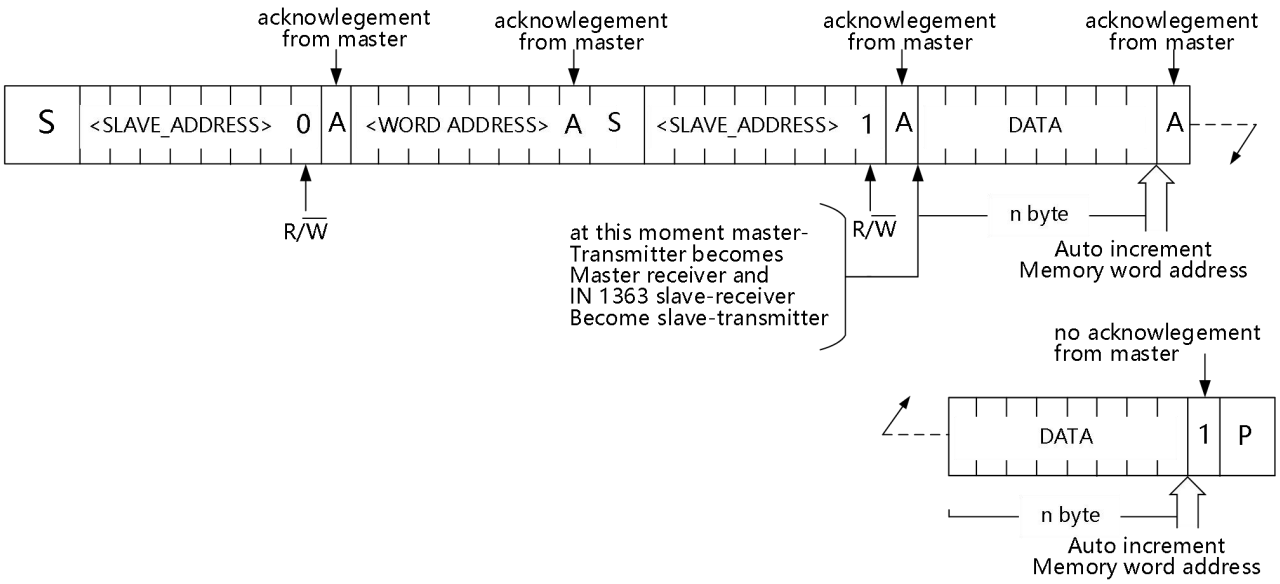


Data Writing- mode of 《SLAVE》 Receiver

2. Mode of《slave》Tranceiver (read-out mode from CD1307):

The first byte is received and processed as in the mode of the «slave» receiver. However, in this mode the direction bit will signify, that the transmission direction is changed. CD1307 sends the se-rial data by SDA, the cycle pulses - by SCL. statuses START and STOP are understood as the be-ginning and end of the consecutive transmission. The address byte is the first byte, received after occurrence of the status START, generated by the «master». The address byte contains the seven bits of the address CD1307, equal to 1101000, accompanied by the direction bit (R_F), which is equal to 1 for reading. After receipt and decoding of the address byte CD1307 receives confirmation from the line SDA. Then CD1307 starts to send the data from the address, which is indicated by the register indicator. If the register indicator is not written prior to initialization of the read mode, then the first read address is the last address , retained in the register indicator. CD1307 should send the bit of «non-confirmation», in order to complete the reading.

Data Reading – Mode of 《SLAVE》 Transmitter



Data reading – mode of «slave» transmitter

Application Note

CRYSTAL CONSIDERATIONS WITH REAL-TIME CLOCKS (RTCS)

This application note describes crystal selection and layout techniques for connecting a 32,768Hz crystal to a real-time (RTC). It also provides information about oscillator circuit-design criteria, system design, and manu-facturing issue.

OSCILLATOR BASICS

The oscillator used in RTCs is a CMOS inverter variation of a Pierce-type oscillator. Figure 1 shows a gen-eral configuration. These RTCs include integrated load capacitors (CL1 and CL2) and bias resistors. The Pierce oscillator utilizes a crystal operating in parallel-resonance mode. Crystals used in parallel-resonance mode will be specified for a certal frequency with a specific load capacitance. For the oscillator to run at the correct frequency, the oscillator circuit must load crystal with the correct capacitive load.

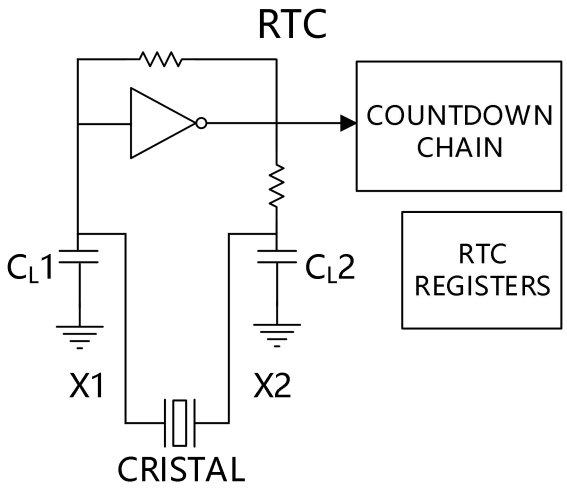


Figure 1. RTC oscillator with internal load capacitors and bias resistors.

ACCURACY

The frequency accuracy of a crystal-based oscillator circuit is mainly dependent upon the accuracy of the crystal and the accuracy of the match between the crystal and the oscillator capacitive load. If the capacitive load is less than the crystal was designed for, the oscillator runs fast. If the capacitive load is greater than what the crystal was designed for, the oscillator runs slow.

In addition to the errors from the crystal and the load match, crystals vary from their base frequency as the ambient temperature changes. RTCs use "tuning fork" crystals, which exhibit an error over temperature, as shown in Figure 2 . An error of 20ppm is equivalent to approximately 1 minute per month.

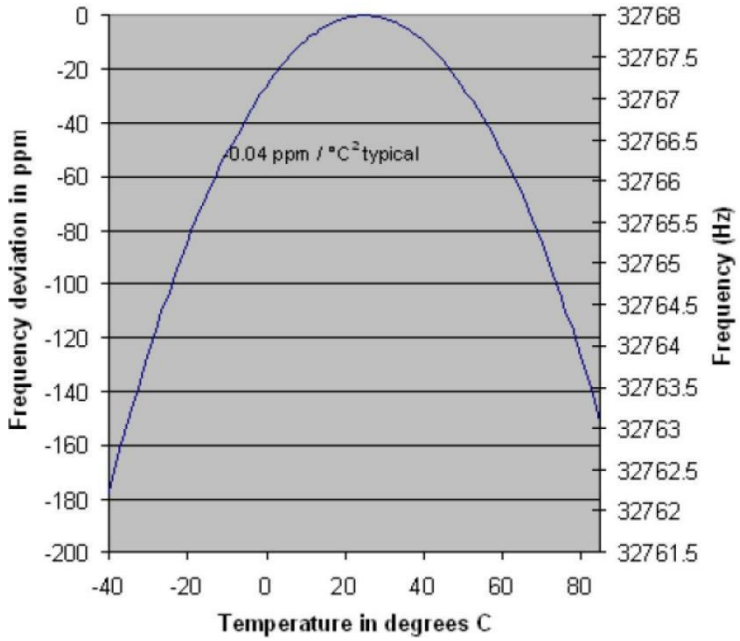


Figure 2. Crystal frequency vs. temperature.

Note: If better accuracy is required, a TCXO such as the DS32kHz can be used

CRYSTAL PARAMETERS

Figure 3 shows the equivalent circuit for a crystal. Near the resonate frequency the circuit consists of a se-ries circuit including motional inductance L1, motional resistance R1, and motional capacitance C1. The par-allel component C O is the shunt capacitance of the crystal.

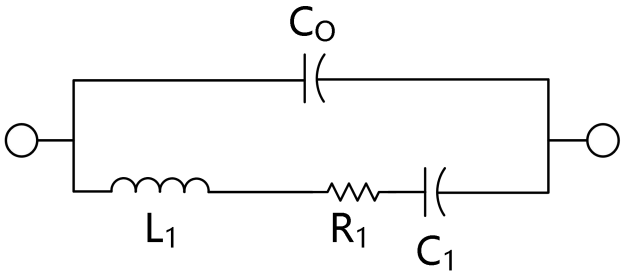


Figure 3. Crystal equivalent circuit.

The load capacitance CL is the capacitive load of the oscillating circuit as seen from the pins of the crystal. Figure 4 shows CL as a capacitance in parallel with the crystal. The load capacitors used in an oscillator circuit, CL1 and CL2, plus any stray capacitance in the circuit, combine to create the overall load capacitance. All RTCs have integrated CL1 and CL2 capacitors. Care should be taken to minimize stray capacitance in the PC board layout. The following formula shows the relationship between CL and load capacitor values:

$$CL = [\frac{(C_L1 \times C_2 2)}{(C_L1 + C_2 2)} + C_{STRAY}]$$

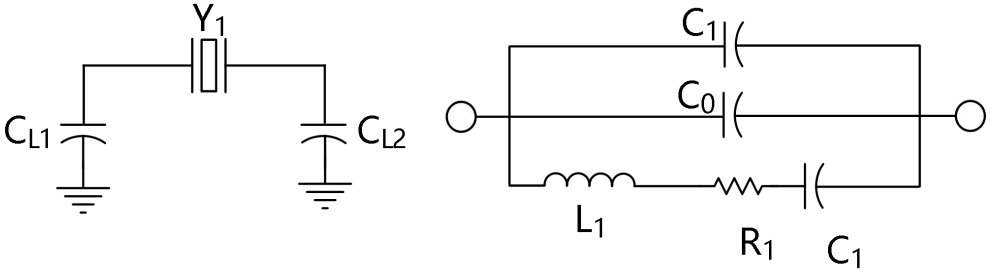


Figure 4. Crystal load capacitors and equivalent parallel load.

Most crystals allow a maximum drive level of 1μW. All RTCs run under 1μW. Drive level may be determined using the following formula:

$$P = 2R_1 \times [\pi \times 32768(C_0 + C_L)VRMS]2$$

where VRMS is the RMS value of the voltage across the crystal.

OSCILLATOR STARTUP TIME

Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within one second.

Table 1. Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Units
Nominal Frequency	F_O		32.768		kHz
Frequency Tolerance	delta F/ F_O		±20		ppm
Load Capacitance	C_L		6		pF
Temperature Turnover Point	T0	20	25	30	℃
Parabolic Curvature Constant	k			0.042	ppm/℃
Quality Factor	Q	40,000	70,000		
Series Resistance	ESR			45	kΩ
Shunt Capacitance	C0		1.1	1.8	pF
Capacitance Ratio	C0/C1		430	600	
Drive Level	D_L			1	μW

Note 1: Some devices allow higher ESR values, check the datasheet for specific requirements.

Table 2. Crystal Suppliers, cylinder-type (ESR=45kΩ)

Manufacturer	Part	Frequency Tolerance(ppm)	ESR(KΩ)	Drive Level max (μW)	CL-pF	Alternate CL?	Temp Range(℃)	Surface or Thru-Hole	Package Dimensions(mm)	Manufacturer Ordering Number
Citizen	CFS-145	±20	40	1.0	8.0	yes	-10 to +60	TH	1.5×5.1	
Citizen	CFS-206	±20	35	1.0	12.5	yes	-10 to +60	TH	2.1×6.2	

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Citizen	CMR-200T	±20	35	1.0	12.5 or 6.0	yes	-40 to +85	SMT	2.0×6.0	CMR200TB32.768KDZFTR or CMR200TB32.768KDZBTR
ECS, Inc.	ECS-3×8	±20	35	1.0	12.5	?	-40 to +60	TH	3.1×8.2	
ECS, Inc.	ECS-2×6	±20	35	1.0	12.5	?	-10 to +60	TH	2.1×6.2	
ECS, Inc.	ECS-1×5	±20	35	1.0	8	?	-10 to +60	TH	1.5×5.1	
KDS/Daiwa	DT-26	±20 or ±30	40	1.0	12.5	yes	-10 to +60	TH	2.0×6.0	1TB602G00
KDS/Daiwa	DT-38	±20 or ±30	30	1.0	12.5	yes	-10 to +60	TH	3.0×8.0	
Pletronics	W×15	±20	40	1.0	8.0	yes	-10 to +60	TH	1.5×5.1	WX15-32.768k-6pF
Pletronics	WX26	±20	40	1.0	12.5	6.0	-10 to +60	TH	2.1×6.2	WX26-32.768k-6pF
Fox	NC-38		35	1.0	12.5	6.0	-20 to +60	TH	3.0×8.3	
Seiko	C-001R	±20	45	1.0	12.5	6	-10 to +60	TH	3.1×8.0	
Seiko	C-2	±20	35	1.0	12.5	6	-10 to +60	TH	2.0×6.0	

Note: Cylinder-type dimensions are barrel diameter and length, and exclude leads.All dimensions approximate.

Table 3. Crystal Suppliers, Surface Mount

Manufacturer	Part	Frequency Tolerance(ppm)	ESR(KΩ)	Drive Level max (μW)	CL-pF	Alternate CL?	Temp Range(℃)	Dimensions(mm) approximate, including leads
Seiko	SP-T3	±10, ±20	55	1.0	12.5	yes	-40 to +85	7.3×4.3×1.8
Seiko	SP-T2	±20	50	1.0	12.5	yes	-40 to +85	8.7×3.7×2.5
EPSON	MC-3.6	±20	50	1.0	12.5	yes	-40 to +85	8.0×3.8×2.54
Citizen	CM200S	±20	50	1.0	12.5	yes	-40 to +85	8.0×3.8×2.5
KDS	DMX-26S	±30	50	1.0	12.5	yes	-40 to +85	8.0×3.8×2.4

POWER CONSUMPTION

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Many RTCs are designed to operate from a battery supply. In a typical application, a small lithium bat-tery can be used to run the oscillator and clock circuitry while the main supply is off. To maximize battery life, the oscillator must run using as little power as possible. To accomplish this, some design tradeoffs must be made.

NEGATIVE RESISTANCE

For typical high-frequency oscillator circuits, it is normal for the circuit to be designed with a 5 or 10X margin for the ESR. Low-frequency crystals typically have higher ESRs. An RTC oscillator may have less than a 2X margin for negative resistance. An oscillator circuit with a low margin normally consumes less cur-rent. As a result, an RTC oscillator often is sensitive to relatively small amounts of stray leakage, noise, or an increase in ESR. The CL of the oscillator circuit influences the power consumption. An RTC with 12.5pF in-ternal loads consumes more power than one that has 6pF loads. However, the oscillator with 12.5pF load capacitors is usually less susceptible to noise.

CRYSTAL LAYOUT GUIDELINES

Since the crystal inputs of RTCs have very high impedance (about 109), the leads to the crystal act like very good antenna, coupling high-frequency signals from the rest of the system. If a signal is coupled onto the crystal pins, it can either cancel out or add pulses. Since most of the signals on a board are at a much higher frequency than the 32.768kHz crystal, it is more likely to add pulses where none are wanted. These noise pulses get counted as extra clock "ticks" and make the clock appear to run fast.

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The following steps illustrate how to determine if noise is causing the RTC to run fast:

1. Power the system up and synchronize the RTC to a known accurate clock.

2. Turn the system power off.

3. Wait for a period of time (two hours, 24 hours, etc.). The longer the time period, the easier it is to measure the accuracy of the clock.

4. Turn the system on again, read clock, and compare to the known accurate clock.

5. Resynchronize the RTC to the known accurate clock.

6. Keep the system powered up and wait for a period of time equal to the period in Step 3.

7. Read the clock after waiting for the above period of time and compare it to the known accurate clock.

By using the above steps, the accuracy of the clock can be determined both when the system is pow-ered up and when the system is powered down. If the clock proves to be inaccurate when the system is powered up, but is accurate when the system is powered down, the problem is most likely due to noise from other signals in the system.

However, if the clock is inaccurate both when the system is powered up and when it is powered down, then the problem is not due to noise from the system. Since it is possible for noise to be coupled onto the crystal pins, care must be taken when placing the external crystal on a PC board layout. It is very important to follow a few basic layout guidelines concerning the placement of the crystal on the PC board layout to en-sure the extra clock ticks do not couple onto the crystal pins.

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1. It is important to place the crystal as close as possible to the X1 and X2 pins. Keeping the trace lengths between the crystal and RTC as small as possible reduces the probability of noise coupling by reducing the length of the antenna. Keeping the trace lengths small also decreases the amount of stray capacitance.

2. Keep the crystal bond pads and trace width to the X1 and X2 pins as small as possible. The larger these bond pads and traces are, the more likely it is that noise can couple from adjacent signals.

3. If possible, place a guard ring (connected to ground) around the crystal. This helps isolate the crystal from noise coupled from adjacent signals. See Figure 2 for an illustration of using a guard ring around a crystal.

4. Try to ensure that no signals on other PC board layers run directly below the crystal or below the traces to the X1 and X2 pins. The more the crystal is isolated from other signals on the board, the less likely it is that noise is coupled into the crystal. There should be a minimum of 0.200 inches be-tween any digital signal and any trace connected to X1 or X2. The RTC should be isolated from any component that generates electromagnetic radiation (EMR). This is true for discrete and module type RTCs.

5. It may also be helpful to place a local ground plane on the PC board layer immediately below the crystal. This helps to isolate the crystal from noise coupling from signals on other PC board layers. Note that the ground plane needs to be in the vicinity of the crystal only and not on the entire board. See Figure 5 for an illustration of a local ground plane. Note that the perimeter of the ground plane does not need to be larger than the outer perimeter of the guard ring.

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Note that care must be taken concerning the use of a local ground plane because of the stray capaci-tance that it introduces. The capacitance between the traces/pads and ground plane is added to the internal load capacitors (C_L1 and C_L2). Therefore, some factors must be taken into account when considering adding a local ground plane. For example, the capacitance due to the ground plane can be approximated by the following equation:

C=εA/t, where

ε=dielectric constant of the PC board

A=area of the traces/pads

t=thickness of the PC board layer

Therefore, to determine if a ground plane is appropriate for a given design, the above parameters must be taken into account to ensure that the capacitance from the local ground plane is not sufficiently large enough to slow down the clock.

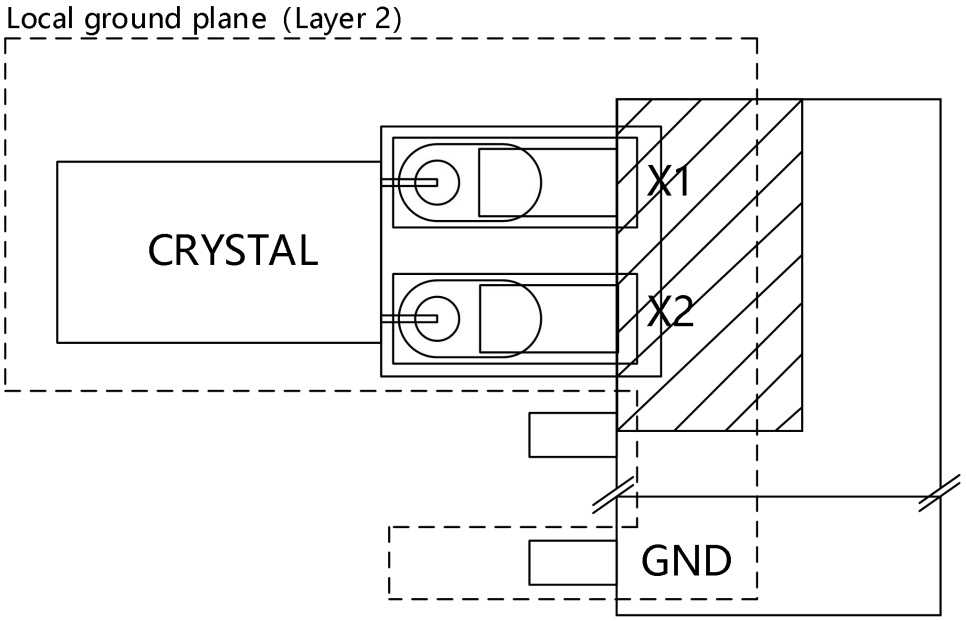

Figure 5. Recommended layout for crystal.

Checking For Oscillation

The first impulse that a designer has when checking for oscillator operation often is to connect an os-cilloscope probe to the oscillator input (X1) or output (X2) pin. Doing so is not recommended when using a Real-Time Clock. Since the oscillator is designed to run at low power (which extends operating time from a battery), loading the oscillator with an oscilloscope probe is likely to stop the oscillator. If the oscillator does not stop, the additional loading will reduce the signal amplitude, and may cause erratic operation, such as varying amplitude. Oscillation should therefore be verified indirectly.

Oscillation can be verified several ways. One method is to read the seconds register multiple times, looking for the data to increment. On RTCs with an OSF (Oscillator Stop Flag), clearing and then monitoring this bit will verify that the oscillator has started and is continuously running.

These methods won’ t work if the designer is troubleshooting a design and cannot communicate with the RTC. An alternate method is to check the square wave output on RTCs that have a square wave output. Check the datasheet to verify if the RTC must be written first to enable the oscillator and square wave output. Note that most RTC square wave out-puts are open-drain, and require a pull up resistor for operation. The square wave output can also be used to verify the accuracy of the RTC, however, a frequency counter with sufficient accuracy must be used.

Fast Clocks

The following are the most common scenarios that cause a crystal-based RTC to run fast.

1. Noise coupling into the crystal from adjacent signals. This problem has been extensively

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covered above. Noise coupling usually causes an RTC to be grossly inaccurate.

2. Wrong crystal. An RTC typically runs fast if a crystal with a specified load capacitance (CL) greater than the RTC-specified load capacitance is used. The severity of the inaccuracy is dependent on the value of the CL. For example, using a crystal with a CL of 12pF on an RTC designed with a 6pF CL causes the RTC to be about 3 to 4 minutes per month fast.

Slow Clocks

The following are the most common scenarios that cause a crystal-based RTC to run slow.

1. Overshoots on RTC input pins. It is possible to cause a RTC to run slow by periodically stopping the oscillator. This can be inadvertently accomplished by noisy input signals to the RTC. If an input sig-nal rises to a voltage that is greater than a diode drop (~0.3V) above VDD, the ESD protection diode for the input pin will forward bias, allowing the substrate to be flooded with current. This, in turn, stops the oscillator until the input signal voltage decreases to below a diode drop above VDD.

This mechanism can cause the oscillator to stop frequently if input signals are noisy. Therefore, care should be taken to ensure there is no overshoot on input signals.

Another situation that is common to overshoot problem is having an input to the RTC at 5V when the RTC is in battery-backup mode. This can be a problem in systems that systematically shut down cer-tain circuits but keep others powered up. It is very important to ensure there are no input signals to the RTC that are greater than the battery voltage (unless stated otherwise in the device data sheet) when the device is in battery-backup mode.

2. Wrong crystal. A RTC typically runs slow if a crystal with a specified CL is less than the CL of the

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RTC. The severity of the inaccuracy is dependent on the value of the CL.

3. Stray capacitance. Stray capacitance between the crystal pins and/or to ground can slow an RTC down. Therefore, care must be taken when designing the PC board layout to ensure the stray ca-pacitance is kept to a minimum.

4. Temperature. The further the operating temperature is from the crystal turnover temperature, the slower the crystal oscillates. See Figures 3 and 4.

Clock Does Not Run

The following are the most common scenarios that cause a RTC to not run.

1. The single most common problem when the clock does not run is that the CH (clock halt) or EOSC (enable oscillator) bit has not been set or cleared, as required. Many RTCs include a circuit that keeps the oscillator from running when power is first applied. This allows a system to wait for ship-ment to the customer, without drawing power from the backup battery. When the system is powered for the first time, the software/firmware must enable the oscillator and prompt the user for the correct time and date.

2. Surface mount crystals may have some N.C. (no connect) pins. Make sure that the correct pins from the crystal are connected to the X1 and X2 pins.

CRYSTAL MANUFACTURING ISSUES

Tuning fork crystals should not be exposed to ultrasonic cleaning. They are susceptible to damage from resonant vibration.

Crystals should not be exposed to temperatures above their maximum ratings. Exposure to excessive temperatures may damage the crystal, and usually increase the ESR. Crystal "cans"

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should not be soldered to a PC board. This is sometimes done to ground the case of the crystal. Soldering directly to the case of the crystal usually subjects the unit to excessive temperatures.

RTCs should generally be used in noncondensing environments. Moisture forming around the oscilla-tor conductors can cause leakage, which can cause the oscillator to stop. Conformal coatings can be used to protect the circuit, however, conformal coating may by itself cause problems.

Some conformal coatings, especially epoxy-based materials, can have unacceptable levels of ionic contamination. In addition, conformal coatings can, if the PC board surface is not sufficiently cleaned prior to conformal coating, cause contaminants to concentrate around leads and traces.

Solder flux residue can cause leakage between pins. RTC oscillator circuits are especially sensitive to leakage because of their low-power operation. Leakage between the oscillator input and output, or leakage to ground, often keep the oscillator from running.

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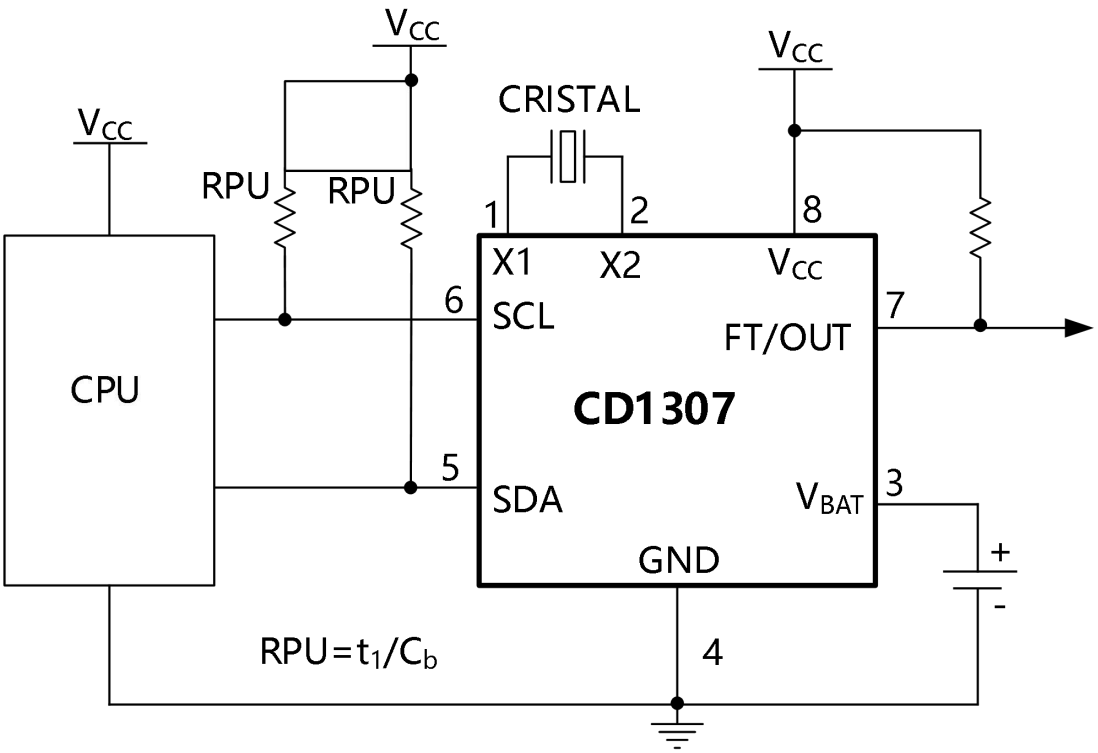
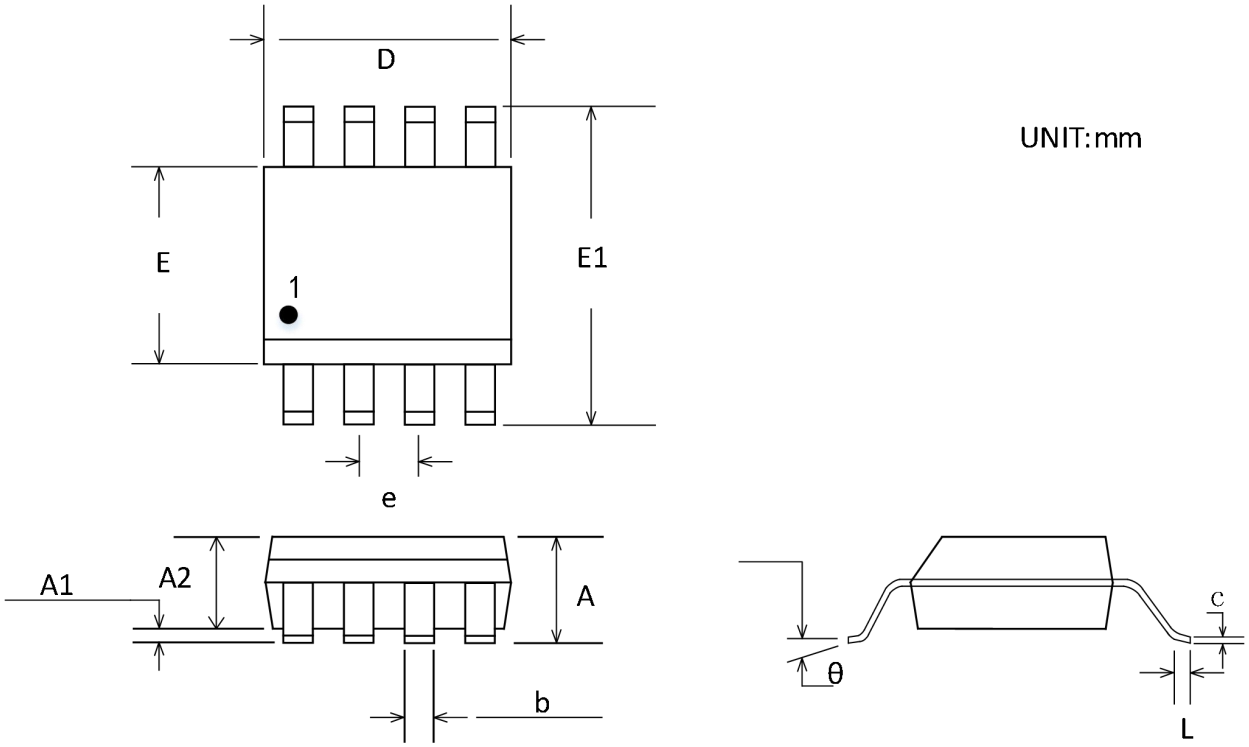
Typical Application Circuit



Package Outline Dimensions

SOP-8



UNIT:mm

Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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Chinese version:CD1307

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD1307AS8	-40℃ ~ 85℃	SOP-8	Tape and Reel, 2500
CD1307AS8-RL	-40℃ ~ 85℃	SOP-8	Tape and Reel, 3000
CD1307AS8-REEL	-40℃ ~ 85℃	SOP-8	Tape and Reel, 4000

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Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.18	Initial version	Regular update	WW	LYL	

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Chinese version:CD1307