CoreadDvices
承芯微电子

CD13S38

I2C RTC with 56-Byte NV RAM

Version: Rev 1.0.0 Date: 2025-6-25

Features

- Completely Manages All Timekeeping Functions
  - o RTC Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
  - o 56-Byte, Battery-Backed, GeneralPurpose RAM with Unlimited Writes
  - o Programmable Square-Wave Output Signal
- Interfaces with Most Microcontrollers
  - o I2C Serial Interface
- Low-Power Operation Extends Battery Backup Run Time
  - o Automatic Power-Fail Detect and Switch Circuitry
- -40°C to +85°C Industrial Temperature Range Supports Operation in a Wide Range of Applications

Application

- Handhelds (GPS, POS Terminal)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)
- Office Equipment (Fax/Printer, Copier)
- Medical (Glucometer, Medicine
- Telecommunications (Router, Switcher,
- Other (Utility Meter, Vending Machine,

Description

The CD13S38 serial real-time clock (RTC) is a lowpower, full binary-coded decimal (BCD) clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I2C interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The CD13S38 has a built-in powersense circuit that detects power failures and automatically switches to the backup supply, maintaining time and date operation.

Contents

Pin Configurations

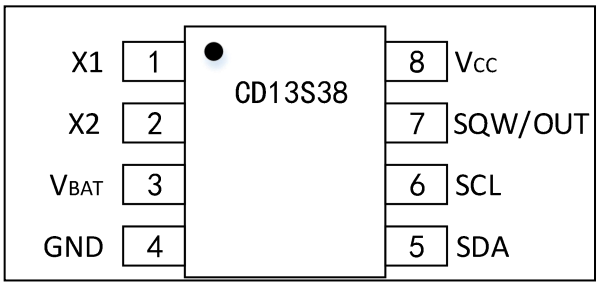


Figure 1. SOP8 Pin Configuration

Pin Description

Table 1. Pin description

Pin No.	Pin Name	Description
1	X1	32.768kHz Crystal Connections. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5pF. An external 32.768kHz oscillator can also drive the CD13S38. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left unconnected.
2	X2	
3	V_{BAT}	Backup Supply Input for Lithium Cell or Other Energy Source. Battery voltage must be held between the minimum and maximum limits for proper operation. Diodes placed in series between the backup source and the VBAT pin may prevent proper operation. If a backup supply is not required, VBAT must be grounded. UL recognized to ensure against reverse charging when used with a lithium cell.
4	GND	Ground. DC power is provided to the device on these pins. VCC is the primary power input. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and VCC is below VPF, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.
5	SDA	Serial Data. Input/output pin for the I2C serial interface. It is an open drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V regardless of the voltage on VCC.
6	SCL	Serial Clock. Input pin for the I2C serial interface. Used to synchronize data movement on the serial interface. The pull up voltage may be up to 5.5V regardless of the voltage on VCC.

7	SQW/OUT	Square-Wave/Output Driver. When enabled and the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). It is an open drain output and requires an external pullup resistor. Operates with either VCC or VBAT applied. The pull up voltage may be up to 5.5V regardless of the voltage on VCC. If not used, this pin may be left unconnected.
8	V_{CC}	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and VCC is below VPF, reads and writes are inhibited. The backup supply maintains the timekeeping function while VCC is absent.

Notes:

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor via a 0.75 µH series inductor and a 10 Ω series resistor.
3. Junction temperature in accordance with IEC 60747-1. An alternative definition of Tvj is: Tvj = Tamb + P × Rth(vj-amb),
where Rth(vj-amb) is a fixed value to be used for the calculating of Tvj. The rating for Tvj limits the allowable
combinations of power dissipation (P) and ambient temperature (Tamb).

Functional Block diagram

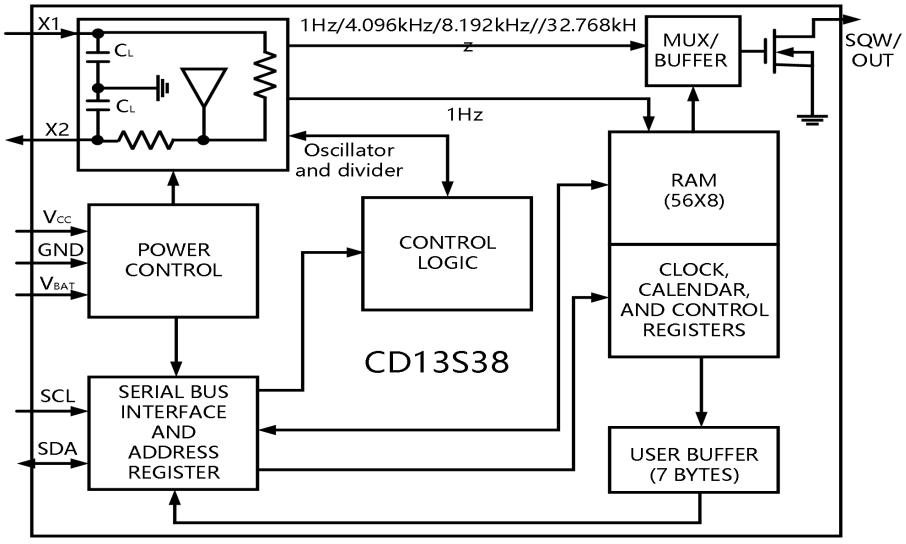


Figure 2. Functional Block Diagram

Typical Application Circuit

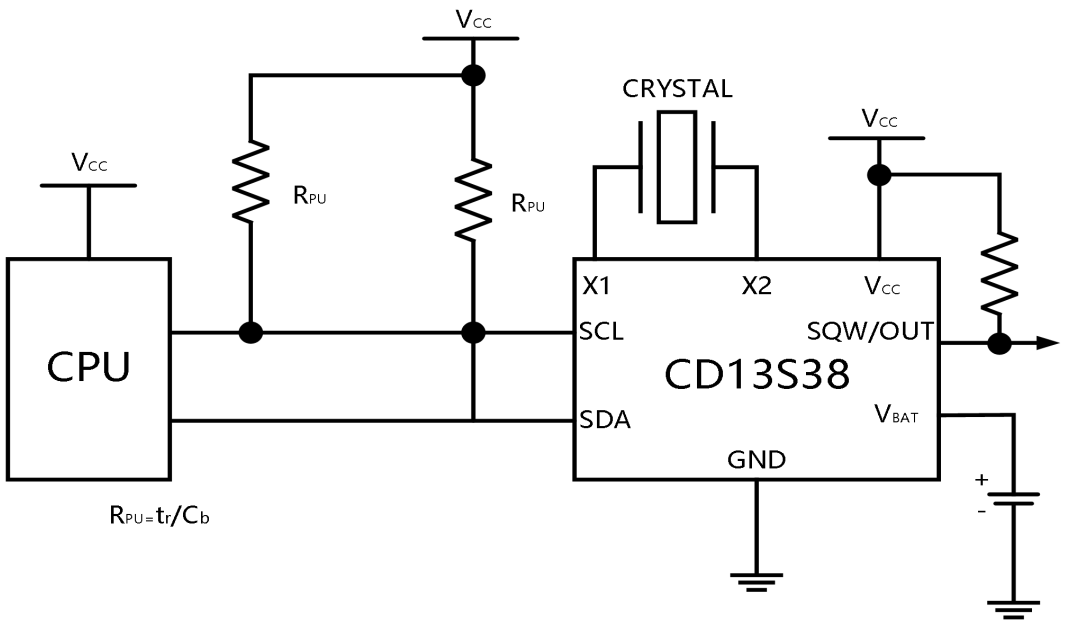


Figure 3. Typical Application Circuit Diagram

Absolute Maximum Ratings

Parameter	Range
Voltage Range on Any Pin Relative to GND	−0.3 V to +6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10s)	260°C
Soldering Temperature (reflow)	260°C

Operating Temperatures Range

(VCC = VCC(MIN) to VCC(MAX), TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C, unless otherwise noted.) (Note 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	VCC	CD13S38-1.8	1.71	1.8	5.5	V
		CD13S38-3	2.7	3.0	5.5	
		CD13S38-3.3	3.0	3.3	5.5	

Logic0	V_{IL}	(Note2)	-0.3		$+0.3V_{CC}$	V
Logic1	V_{IH}	(Note2)	$0.7V_{CC}$		$V_{CC}+0.3$	V
Power-Fail Voltage	V_{PF}	CD13S38-1.8	1.51	1.62	1.71	V
		CD13S38-3	2.45	2.59	2.70	
		CD13S38-3.3	2.70	2.82	2.97	
V_{BAT} Input Voltage	V_{BAT}	(Note2)	1.3	3.0	3.7	V

DC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = TYP, T_A = +25°C, unless otherwise noted.) (Note 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage	I_{LI}	(Note3)	--	--	1	μA
I/O Leakage	I_{LO}	(Note4)	--	--	1	μA
SDA Logic 0 Output	I_{OLSDA}	V_{CC} > 2V; V_{OL} = 0.4V	--	--	3.0	mA
		V_{CC} < 2V; V_{OL} = 0.2 x V_{CC}	--	--	3.0	
SQW/OUT Logic 0 Output	I_{OLSQW}	V_{CC} > 2V; V_{OL} = 0.4V	--	--	3.0	μA
		1.71V < V_{CC} < 2V;V_{OL} = 0.2 x V_{CC}	--	--	3.0	mA
		1.3V < V_{CC} < 1.71V;V_{OL} = 0.2 x V_{CC}	--	--	250	μA
Active Supply Current (Note 5)	I_{CCA}	CD13S38-1.8: V_{CC} = 1.89V	--	75	150	μA
		CD13S38-3.0: V_{CC} = 3.30V	--	110	200	μA
		CD13S38-3.3: V_{CC} = 3.63V	--	120	200	
		CD13S38-3.3: V_{CC} = 5.5V	--	--	325	
Standby Current (Note 6)	I_{CCS}	CD13S38-1.8: V_{CC} = 1.89V	--	60	100	μA
		CD13S38-3.0: V_{CC} = 3.30V	--	80	125	μA
		CD13S38-3.3: V_{CC} = 3.63V	--	85	125	
		CD13S38-3.3: V_{CC} = 5.5V	--	--	200	
V_{BAT} Leakage Current (V_{CC} Active)	I_{BATLKG}		--	25	100	nA

(V_{CC} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{BAT} Current (OSC ON); V_{BAT} = 3.7V, SQW/OUT OFF (Note 7)	$I_{BATOSC1}$	--	800	1200	nA
V_{BAT} Current (OSC ON); V_{BAT} = 3.7V, SQW/OUT ON (32kHz) (Note 7)	$I_{BATOSC2}$	--	1025	1400	nA
V_{BAT} Data-Retention Current (Osc Off); V_{BAT} = 3.7V (Note 7)	I_{BATDAT}	--	10	100	nA

AC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C) (Note 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL Clock Frequency	f_{SCL}	Fast mode	100	--	400	kHz
		Standard mode	0	--	100	
Bus Free Time Between STOP and START Condition	t_{BUF}	Fast mode	1.3	--	--	μs
		Standard mode	4.7	--	--	
Hold Time (Repeated) START Condition (Note 8)	$t_{HD:STA}$	Fast mode	0.6	--	--	μs
		Standard mode	4.0	--	--	
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3	--	--	μs
		Standard mode	4.7	--	--	
High Period of SCL Clock	t_{High}	Fast mode	0.6	--	--	μs
		Standard mode	4.0	--	--	
Setup Time for Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6	--	--	μs
		Standard mode	4.7	--	--	
Data Hold Time (Notes 9, 10)	$t_{HD:DAT}$	Fast mode	0	--	0.9	μs
		Standard mode	0	--	--	
Data Setup Time (Note 11)	$t_{SU:DAT}$	Fast mode	100	--	--	ns
		Standard mode	250	--	--	
Rise Time of Both SDA and SCL Signals (Note 12)	t_R	Fast mode	20+0.1 C_B	--	300	ns
		Standard mode	20+0.1 C_B	--	1000	
Fall Time of Both SDA and	t_F	Fast mode	20+0.1	--	300	ns

SCL Signals (Note 12)			C_B			
		Standard mode	20+0.1 C_B	--	1000	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6	--	--	μs
		Standard mode	4.0	--	--	
Capacitive Load for Each Bus Line	C_B	(Note 12)			400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	(Note 13)			10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 14)		100		ms

Power-Up/Power-Down Characteristics

(T_A = -40°C to +85°C) (Note 1, Figure 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Recovery at Power-Up (Note 15)	t_{REC}	--	--	2	ms
VCC Fall Time; VPF(MAX) to $V_{PF(MIN)}$	t_{VCCF}	300	--	--	μs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}	0	--	--	μs

Warning: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

Note 1: Limits at -40°C are guaranteed by design and not production tested.

Note 2: All voltages are referenced to ground.

Note 3: SCL only.

Note 4: SDA and SQW/OUT.

Note 5: ICCA—SCL clocking at max frequency = 400kHz.

Note 6: Specified with the I2C bus inactive.

Note 7: Measured with a 32.768kHz crystal attached to X1 and X2.

Note 8: After this period, the first clock pulse is generated.

Note 9: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIH(MIN) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 10: The maximum tHD:DAT need only be met if the device does not stretch the LOW period (tLOW) of the SCL signal.

Note 11: A fast-mode device can be used in a standard-mode system, but the requirement tSU:DAT ≥ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tR(MAX) + tSU:DAT = 1000 + 250 =

1250ns before the SCL line is released.
Note 12: CB—total capacitance of one bus line in pF.
Note 13: Guaranteed by design. Not production tested.
Note 14: The parameter tOSF is the time period the oscillator must be stopped for the OSF flag to be set over the voltage range of 0.0V ≤ VCC ≤ VCC(MAX) and 1.3V ≤ VBAT ≤ 3.7V.
Note 15: This delay applies only if the oscillator is enabled and running. If the oscillator is disabled or stopped, no power-up delay occurs.

DETAILED DESCRIPTION

The CD13S38 serial RTC is a low-power, full BCD clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I2C interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The CD13S38 has a built-in power-sense circuit that detects power failures and automatically switches to the VBAT supply.

OPERATION

The CD13S38 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code, followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when VCC is greater than VPF. However, when VCC falls below VPF, the internal clock registers are blocked from any access. If VPF is less than VBAT, the device power is switched from VCC to VBAT when VCC drops below VPF. If VPF is greater than VBAT, the device power is switched from VCC to VBAT when VCC drops below VBAT. The oscillator and timekeeping functions are maintained from the VBAT source until VCC is returned to nominal levels. The block diagram (Figure 3) shows the main elements of the CD13S38.An enable bit in the seconds register controls the oscillator. Oscillator startup times are highly dependent upon crystal characteristics, PC board leakage, and layout. High ESR and excessive capacitive loads are the major contributors to long start-up times. A circuit using a crystal with the recommended characteristics and proper layout usually starts within 1 second.

POWER CONTROL

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the VCC level. The device is fully accessible and data can be written and read when VCC is greater than VPF. However, when VCC falls below VPF,

the internal clock registers are blocked from any access. If VPF is less than VBAT, the device power is switched from VCC to VBAT when VCC drops below VPF. If VPF is greater than VBAT, the device power is switched from VCC to VBAT when VCC drops below VBAT. The registers are maintained from the VBAT source until VCC is returned to nominal levels (Table 1). After VCC returns above VPF, read and write access is allowed after tREC (Figure 1). On the first application of power to the device the time and date registers are reset to 01/01/00 01 00:00:00 (DD/MM/YY DOW HH:MM:SS). The CH bit in the seconds register will be set to a 0.

Table 1. Power Control

Supply Condition	Read/Write Access	Powered By
$V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$	No	V_{BAT}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$	Yes	V_{CC}

OSCILLATOR CIRCUIT

The CD13S38 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 2 specifies several crystal parameters for the external crystal. Figure 3 shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 2. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O	--	32.768	--	kHz
Series Resistance	ESR	--	--	50	kΩ
Load Capacitance	C_L	--	12.5	--	pF

CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 4 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to Application Note 58: Crystal Considerations with Dallas Real-Time Clocks for detailed

information.

RTC AND RAM ADDRESS MAP

Table 3 shows the address map for the RTC and RAM registers. The RTC registers and control register are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multibyte access, when the register pointer reaches 3Fh (the end of RAM space) it wraps around to location 00h (the beginning of the clock space). On an I2C START, STOP, or register pointer incrementing to location 00h, the current time and date is transferred to a second set of registers. The time and date in the secondary registers are read in a multibyte data transfer, while the clock continues to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. See Figure 6 for the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. Bit 7 of Register 0 is the clock halt (CH) bit. When this bit is set to 1, the oscillator is disabled. When cleared to 0, the oscillator is enabled. The clock can be halted whenever the timekeeping functions are not required, which minimizes VBAT current (IBATDAT) when VCC is not applied.
The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any start or stop and when the register pointer rolls over to zero. The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the CD13S38. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running. The CD13S38 runs in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit, with logic high being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20–23 hours). If the 12/24-hour mode select is changed, the hours register must be re-initialized to the new format. On an I2C START, the current time is transferred to a

second set of registers. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 3. RTC and RAM Address Map

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Range
00H	CH	10 Seconds			Seconds				Seconds	00-59
01H	0	10 Minutes			Minutes				Minutes	00-59
02H	0	12/24	AM/PM 20Hour	10Hours	Hour				Hours	1–12 +AM/PM 00–23
03H	0	0	0	0	0	Day			Day	1-7
04H	0	0	10Date		Day				Date	01-31
05H	0	0	0	10Month	Month				Month	01-12
06H	10 Year				Year				Year	00-99
07H	Out	0	OSF	SQWE	0	0	RS1	RS0	Control	
08H-3FH									RAM56x8	-00H-FFH

CONTROL REGISTER (07H)

The control register controls the operation of the SQW/OUT pin and provides oscillator status.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Out	0	OSF	SQWE	0	0	RS1	RS0
1	0	1	1	0	0	1	1

Bit 7: Output Control (OUT). Controls the output level of the SQW/OUT pin when the square-wave output is disabled. If SQWE = 0, the logic level on the SQW/OUT pin is 1 if OUT = 1; it is 0 if OUT = 0.

Bit 5: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator has stopped or was stopped for some time period and can be used to judge the validity of the clock and calendar data. This bit is edge triggered, and is set to logic 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a STOP condition. The following are examples of conditions that may cause the OSF bit to be set:

1) The first time power is applied.

2) The voltage present on VCC and VBAT are insufficient to support oscillation.

3) The CH bit is set to 1, disabling the oscillator.

4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

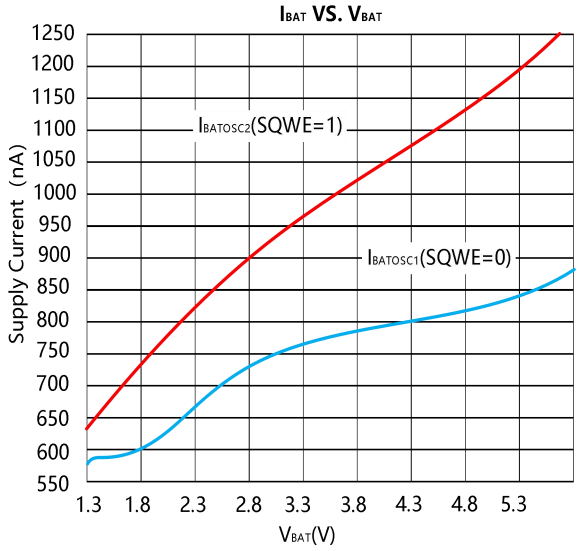
Bit 4: Square-Wave Enable (SQWE). When set to logic 1, this bit enables the oscillator output to operate with either VCC or VBAT applied. The frequency of the square-wave output depends upon the value of the RS0 and RS1 bits.

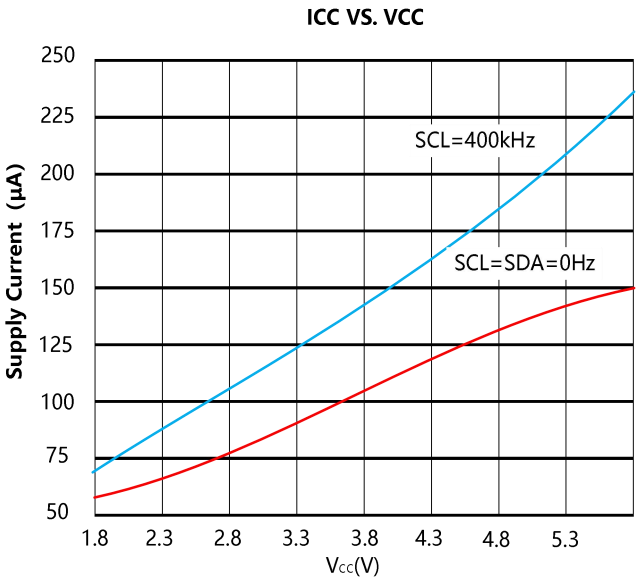
Bits 1 and 0: Rate Select (RS1 and RS0). These bits control the frequency of the square-wave output when the square-wave output has been enabled. The table below lists the square-wave frequencies that can be selected with the RS bits.

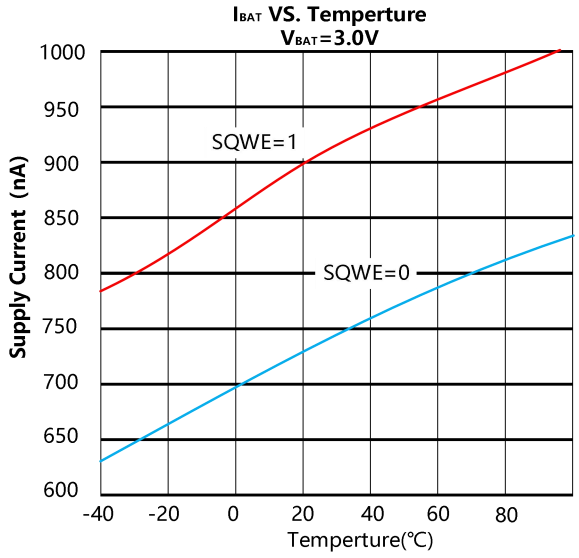
Square-Wave Output

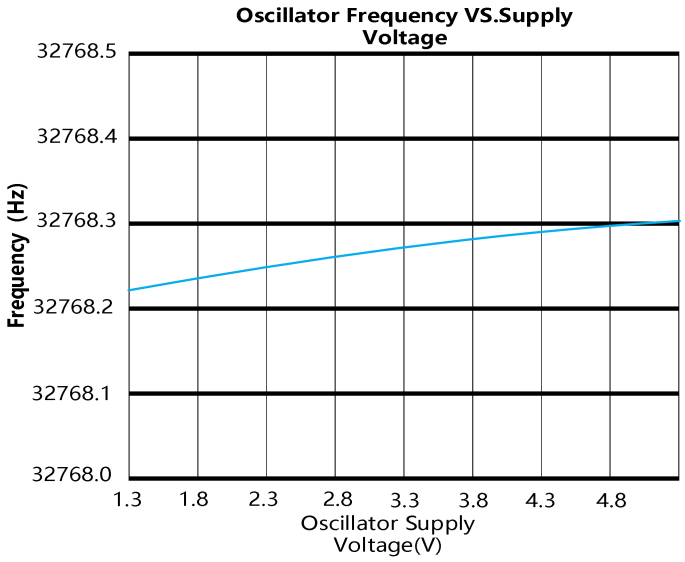
Out	RS1	RS0	SQW Output	SQWE
X	0	0	1Hz	1
X	0	1	4.096kHz	1
X	1	0	8.192kHz	1
X	1	1	32.768kHz	1
0	X	X	0	0
1	X	X	1	0

Typical Electrical Characteristics









Chinese version:CD13S38

Package Outline Dimensions

SOP-8

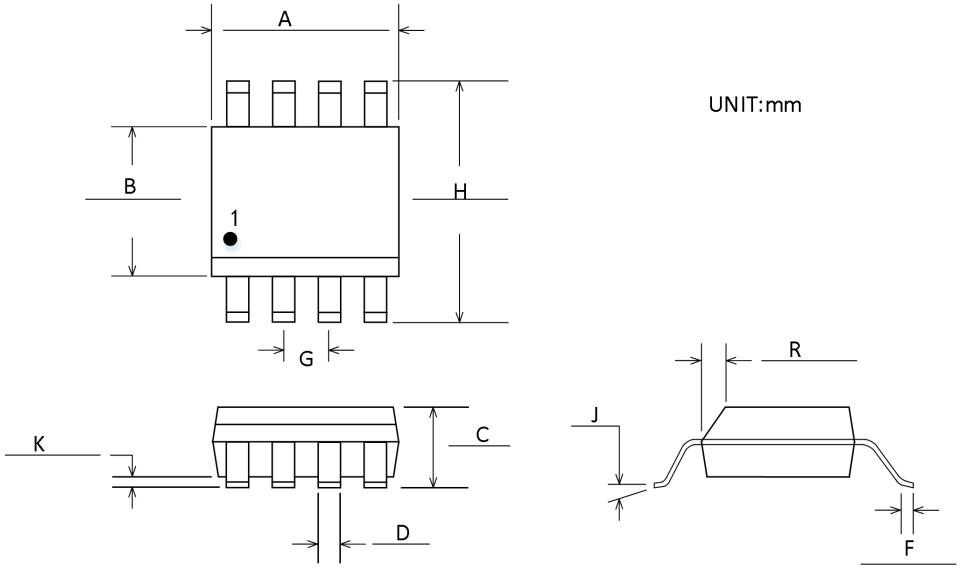


Figure 4 . 8-Lead Outline Package [SOP-8]

Symbol	Dimensions (mm)	
	Min	Max
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.31	0.51
F	0.40	1.27
G	1.27BSC	
H	5.80	6.20
J	0°	8°
K	0.10	0.25
R	0.25	0.50

Chinese version:CD13S38

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD13S38-1.8	-40℃~85℃	SOP-8	Tape and Reel, 2500
CD13S38-1.8-RL	-40℃~85℃	SOP-8	Tape and Reel, 3000
CD13S38-1.8-REEL	-40℃~85℃	SOP-8	Tape and Reel, 4000
CD13S38-3.0	-40℃~85℃	SOP-8	Tape and Reel, 2500
CD13S38-3.0-RL	-40℃~85℃	SOP-8	Tape and Reel, 3000
CD13S38-3.0-REEL	-40℃~85℃	SOP-8	Tape and Reel, 4000
CD13S38-3.3	-40℃~85℃	SOP-8	Tape and Reel, 2500
CD13S38-3.3-RL	-40℃~85℃	SOP-8	Tape and Reel, 3000
CD13S38-3.3-REEL	-40℃~85℃	SOP-8	Tape and Reel, 4000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.25	Initial version	Regular update	WW	LYL	