CoreadDvices
承芯微电子

CD13S39

I2C Serial Real-Time Clock

Version: Rev 1.0.0 Date: 2025-6-25

Features

- Completely Manages All Timekeeping Functions
  - o RTC Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap-Year Compensation Valid Up to 2100
  - oTwo Time-of-Day Alarms
  - o Programmable Square-Wave Output Signal
  - o Oscillator Stop Flag
- Interfaces with Most Microcontrollers
  - o I2C Serial Interface
- Low-Power Operation Extends Battery Backup Run Time
  - o Automatic Power-Fail Detect and Switch Circuitry
  - o Trickle-Charge Capability
- -40°C to +85°C Industrial Temperature Range Supports Operation in a Wide Range of Applications

Application

- Handhelds (GPS, POS Terminal)
- Consumer Electronics (Set-Top Box, Digital Recording, Network Appliance)
- Office Equipment (Fax/Printer, Copier)
- Medical (Glucometer, Medicine Dispenser)
- Telecommunications (Router, Switcher, Server)
- Other (Utility Meter, Vending Machine, Thermostat, Modem)

Description

The CD13S39 serial real-time clock (RTC) is a lowpower clock/date device with two programmable timeof-day alarms and a programmable square-wave output. Address and data are transferred serially through an I2C bus. The clock/date provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The CD13S39 has a built-in powersense circuit that detects power failures and automatically switches to the backup supply, maintaining time, date, and alarm operation.

Chinese version:CD13S39

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Pin Configurations

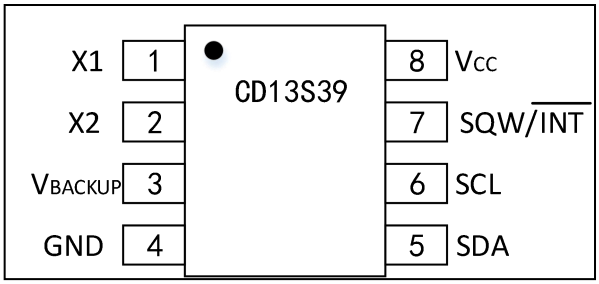

Figure 1. SOP8 Pin Configuration

Pin Description

Table 1. Pin description

Pin No.	Pin Name	Description
1	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 6pF. An external 32.768kHz oscillator can also drive the CD13S39. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is left unconnected.
2	X2	
3	VBACKUP	Secondary Power Supply. Supply voltage must be held between 1.3V and 3.7V for proper operation. This pin can be connected to a primary cell, such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used in conjunction with the trickle-charge feature. Diodes should not be placed in series between the backup source and the VBACKUP input, or improper operation will result. If a backup supply is not required, VBACKUP must be grounded. UL recognized to ensure against reverse charging current when used with a lithium cell.
4	GND	Ground. DC power is provided to the device on these pins.
5	SDA	Serial Data Input/Output. SDA is the input/output pin for the I2 C serial interface. The SDA pin is an open-drain output and requires an external pullup resistor. The pull up voltage may be up to 5.5V regardless of the voltage on VCC.
6	SCL	Serial Clock Input. SCL is used to synchronize data movement on the I2C serial interface. The pull up voltage may be up to 5.5V regardless of the voltage on VCC.
7	SQW/INT	Square-Wave/Interrupt Output. Programmable square-wave or interrupt output signal. The SQW/INT pin is an open-drain output and requires an external pull up resistor. The pull up voltage may be up to 5.5V regardless

		of the voltage on VCC. If not used, this pin may be left unconnected.
8	VCC	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected and VCC is below VPF, reads and writes are inhibited. The timekeeping and alarm functions operate when the device is powered by VCC or VBACKUP.

Notes:

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor via a 0.75 µH series inductor and a 10 Ω series resistor.
3. Junction temperature in accordance with IEC 60747-1. An alternative definition of Tvj is: Tvj = Tamb + P × Rth(vj-amb),
where Rth(vj-amb) is a fixed value to be used for the calculating of Tvj. The rating for Tvj limits the allowable
combinations of power dissipation (P) and ambient temperature (Tamb).

Functional Block diagram

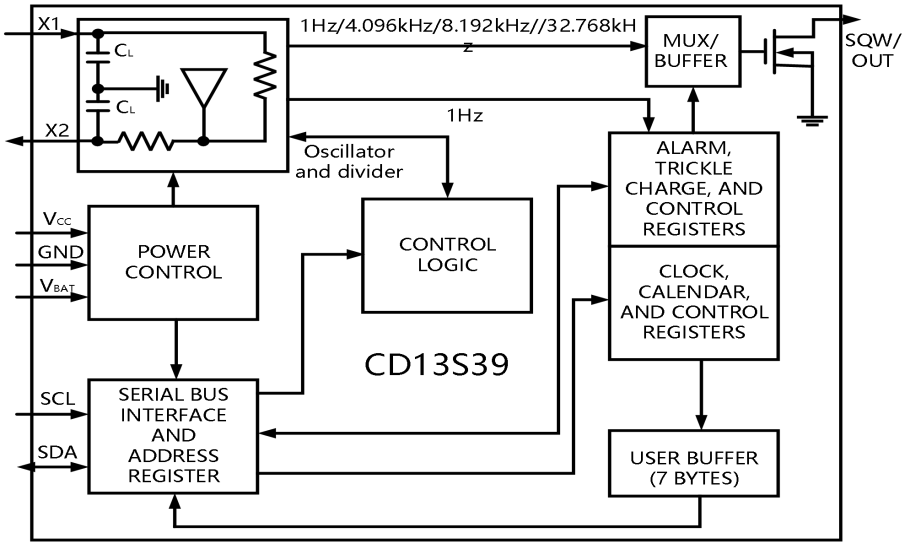

Figure 2. Functional Block Diagram

Typical Application Circuit

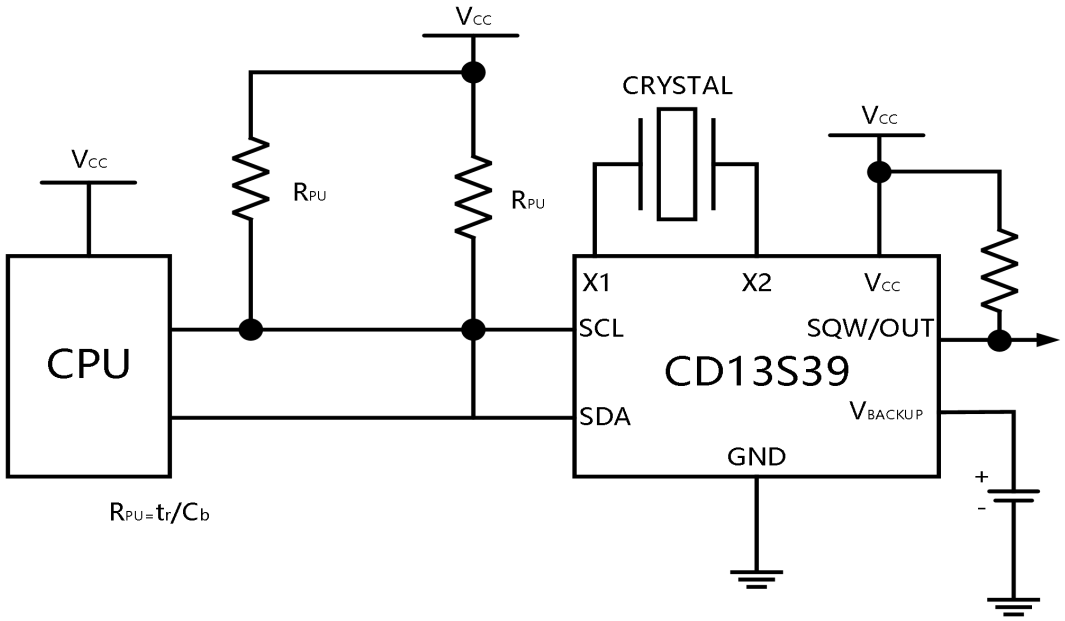

Figure 3. Typical Application Circuit Diagram

Absolute Maximum Ratings

Parameter	Range
Voltage Range on Any Pin Relative to GND	−0.3 V to +6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10s)	260°C
Soldering Temperature (reflow)	260°C
Junction-to-Ambient Thermal Resistance ((θ_{JA}),MSOP)	206.3°C/W
Junction-to-Case Thermal Resistance ((θ_{JC}),MSOP)	42°C/W
Junction-to-Ambient Thermal Resistance ((θ_{JA}),SOP)	73°C/W
Junction-to-Case Thermal Resistance ((θ_{JC}),SOP)	23°C/W

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Operating Temperatures Range

(VCC = VCC(MIN) to VCC(MAX), TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C, unless otherwise noted.) (Note 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	VCC	CD13S39-2	1.8	2.0	5.5	V
		CD13S39-3	2.7	3.0	5.5	
		CD13S38-3.3	2.97	3.3	5.5	
Logic0	V_{IL}		-0.3		$+0.3V_{CC}$	V
Logic1	V_{IH}		$0.7V_{CC}$		$V_{CC}+0.3$	V
Power-Fail Voltage	V_{PF}	CD13S38-2	1.58	1.70	1.80	V
		CD13S38-3	2.45	2.59	2.70	
		CD13S38-3.3	2.70	2.85	2.97	
V_{BACKUP} Input Voltage	V_{BACKUP}		1.3	3.0	3.7	V

DC Electrical Characteristics

(V_{CC} = MIN to MAX, T_A = -40°C to +85°C.) (Note 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage	I_{LI}	(Note3)	--	--	1	μA
I/O Leakage	I_{LO}	(Note4)	--	--	1	μA
Logic 0 Out V_{OL} = 0.4V; V_{CC} > V_{CC} MIN (-3, -33); V_{CC} ≥ 2.0V (-2)	I_{OL}	(Note4)	--	--	3.0	mA
Logic 0 Out V_{OL} = 0.2 (V_{CC}); 1.8V < V_{CC} < 2.0V (CD13S39-2)	I_{OL}	(Note4)	--	--	3.0	mA
Logic 0 Out V_{OL} = 0.2 (V_{CC}); 1.3V < V_{CC} < 2.0V (CD13S39-2)	I_{OL}	(Note4)	--	--	250	μA
V_{CC} Active Current	I_{CCA}	(Note5)	--	--	450	μA
V_{CC} Standby Current (Note 6)	I_{CCS}	-2: V_{CC} = 2.2V	--	60	100	μA
		-3: V_{CC} = 3.3V	--	80	150	
		-33: V_{CC} = 5.5V	--	--	200	μA
V_{BAT} Leakage Current	I_{BATLKG}		--	25	100	nA

Trickle-Charger Resistor Register 10h = A5h, V_{CC} = Typ, V_{BACKUP} = 0V	R1	(Note7)	--	250	--	Ω
Trickle-Charger Resistor Register 10h = A6h, V_{CC} = Typ, V_{BACKUP} = 0V	R2		--	2000	--	Ω
Trickle-Charger Resistor Register 10h = A7h, V_{CC} = Typ, V_{BACKUP} = 0V	R3		--	4000	--	Ω

(V_{CC} = 0V, T_A = -40°C to +85°C.) (Note 2)

Parameter	Symbol		Min.	Typ.	Max.	Unit
V_{BACKUP} Current (EOSC=0),SQW Off	I_{BKOSC}	(Note8)	--	400	700	nA
V_{BACKUP} Current (EOSC=0),SQW On	I_{BKSQW}	(Note8)	--	600	1000	nA
V_{BACKUP} Current (EOSC=1)	I_{BKDR}		--	10	100	nA

AC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C) (Note 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL Clock Frequency	f_{SCL}	Fast mode	100	--	400	kHz
		Standard mode	0	--	100	
Bus Free Time Between STOP and START Condition	t_{BUF}	Fast mode	1.3	--	--	μs
		Standard mode	4.7	--	--	
Hold Time (Repeated) START Condition (Note 8)	$t_{HD:STA}$	Fast mode	0.6	--	--	μs
		Standard mode	4.0	--	--	
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3	--	--	μs
		Standard mode	4.7	--	--	
High Period of SCL Clock	t_{High}	Fast mode	0.6	--	--	μs
		Standard mode	4.0	--	--	
Setup Time for Repeated	$t_{SU:STA}$	Fast mode	0.6	--	--	μs

START Condition		Standard mode	4.7	--	--	
Data Hold Time (Notes 11, 12)	$t_{HD:DAT}$	Fast mode	0	--	0.9	µs
		Standard mode	0	--	--	
Data Setup Time (Note 13)	$t_{SU:DAT}$	Fast mode	100	--	--	ns
		Standard mode	250	--	--	
Rise Time of Both SDA and SCL Signals (Note 14)	t_R	Fast mode	20+0.1 C_B	--	300	ns
		Standard mode	20+0.1 C_B	--	1000	
Fall Time of Both SDA and SCL Signals (Note 14)	t_F	Fast mode	20+0.1 C_B	--	300	ns
		Standard mode	20+0.1 C_B	--	300	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6	--	--	µs
		Standard mode	4.0	--	--	
Capacitive Load for Each Bus Line (Note 14)	C_B		--	--	400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$	(Note 9)	--	--	10	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 15)	--	100	--	ms

Power-Up/Power-Down Characteristics

(T_A = -40°C to +85°C) (Note 1, Figure 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Recovery at Power-Up	t_{REC}	(Note 16)	--	--	2
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}		300	--	--
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}		0	--	--

WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

Note 2: Limits at -40°C are guaranteed by design and are not production tested.

Note 3: SCL only.

Note 4: SDA and SQW/INT.

Note 5: I_{CCA}—SCL at f_{SC} max, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charger disabled.

Note 6: Specified with the I2C bus inactive, V_{IL} = 0.0V, V_{IH} = V_{CC}, trickle charger disabled.

Note 7: V_{CC} must be less than 3.63V if the 250Ω resistor is selected.
Note 8: Using recommended crystal on X1 and X2.
Note 9: Guaranteed by design; not production tested.
Note 10: After this period, the first clock pulse is generated.
Note 11: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge
the undefined region of the falling edge of SCL.
Note 12: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 13: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT}$ ≥ to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.
Note 14: C_B—total capacitance of one bus line in pF.
Note 15: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of $0.0V \le V_{CC} \le V_{CCMAX}$ and $1.3V \le V_{BACKUP} \le 3.7V$.
Note 16: This delay applies only if the oscillator is running. If the oscillator is disabled or stopped, no power-up delay occurs.

DETAILED DESCRIPTION

The CD13S39 serial real-time clock (RTC) is a low-power clock/date device with two programmable time-of-day alarms and a programmable square-wave output. Address and data are transferred serially through an I2 C bus. The clock/date provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The CD13S39 has a built-in powersense circuit that detects power failures and automatically switches to the backup supply, maintaining time, date, and alarm operation.

OPERATION

The CD13S39 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by data. Subsequent registers can be accessed sequentially until a STOP condition is executed. The device is fully accessible and data can be written and read when V_{CC} is greater than VPF. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP},

the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below VPF. If VPF is greater than V_{BACKUP}, the device power is switched from VCC to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels. The block diagram in Figure 3 shows the main elements of the serial real-time clock.

POWER CONTROL

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If VPF is less than VBACKUP, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the VBACKUP source until VCC is returned to nominal levels (Table 1). After V_{CC} returns above V_{PF}, read and write access is allowed after t_{REC} (Figure 1). On the first application of power to the device the time and date registers are reset to 01/01/00 01 00:00:00 (MM/DD/YY DOW HH:MM:SS).

Table 1. Power Control

Supply Condition	Read/Write Access	Powered By
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKUP}$	No	V_{BACKUP}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	V_{CC}

OSCILLATOR CIRCUIT

The CD13S39 uses an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 2 specifies several crystal parameters for the external crystal. Figure 3 shows a functional schematic of the oscillator circuit. The startup time is usually less than 1 second when using a crystal with the specified characteristics.

Table 2. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O	--	32.768	--	kHz
Series Resistance	ESR	--	--	50	kΩ
Load	C_L	--	12.5	--	pF

Capacitance					

CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Crystal frequency drift caused by temperature shifts creates additional error. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 4 shows a typical PC board layout for isolating the crystal and oscillator from noise. Refer to Application Note 58: Crystal Considerations with Dallas Real-Time Clocks for detailed information.

RTC AND RAM ADDRESS MAP

Table 3 shows the address map for the CD13S39 registers. During a multibyte access, when the address pointer reaches the end of the register space (10h), it wraps around to location 00h. On an I2C START, STOP, or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Table 3. Timekeeper Registers

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Range
00H	CH	10 Seconds			Seconds				Seconds	00-59
01H	0	10 Minutes			Minutes				Minutes	00-59
02H	0	12/24	AM/PM 20Hour	10Hours	Hour				Hours	1–12 +AM/PM 00–23
03H	0	0	0	0	0	Day			Day	1-7
04H	0	0	10Date		Day				Date	01-31
05H	Century	0	0	10Month	Month				Month/Century	01-12+ Century
06H	10 Year				Year				Year	00-99
07H	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00-59
08H	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00-59
09H	A1M3	12/24	AM/PM 20Hour	10 Hour	Hour				Alarm 1 Hours	1–12 +AM/PM 00–23

0AH	A1M4	DY/DT	10 Date		Day,Date				Alarm 1 Day Alarm 1 Date	1-7,1-31
0BH	A2M2	10 Minutes			Minutes				Alarm2 Minutes	00-59
0CH	A2M3	12/24	AM/PM 20Hour	10 Hour	Hour				Alarm 2 Hours	1–12 +AM/PM 00–23
0DH	A2M4	DY/DT	10 Date		Day,Date				Alarm 2 Day Alarm 2 Date	1-7,1-31
0EH	EOSC	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE	Control	--
0FH	OSF	0	0	0	0	0	A2F	A1F	Status	--
10H	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charger	--

TIME AND DATE OPERATION

The time and date information is obtained by reading the appropriate register bytes. Table 3 shows the RTC registers. The time and date are set or initialized by writing the appropriate register bytes. The contents of the time and date registers are in the BCD format. The CD13S39 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20 to 23 hours). All hours values, including the alarms, must be re-entered whenever the 12/24-hour mode bit is changed. The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined, but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday and so on). Illogical time and date entries result in undefined operation.
When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START or STOP, and when the address pointer rolls over to zero. The countdown chain is reset whenever the seconds register is written. Write transfers occurs on the acknowledge pulse from the device. To avoid rollover issues, once the countdown chain is reset, the remaining time and date registers must be written within one second. If enabled, the 1Hz square-wave output transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

ALARMS

The CD13S39 contains two time of day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be

programmed (by the Alarm Enable and INTCN bits of the Control Register) to activate the SQW/INT output on an alarm match condition. Bit 7 of each of the time of day/date alarm registers are mask bits (Table 4). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h to 06h match the values stored in the time of day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 4 shows the possible settings. Configurations not listed in the table result in illogical operation. The DY/DT bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/DT is written to a logic 0, the alarm is the result of a match with date of the month. If DY/DT is written to a logic 1, the alarm is the result of a match with day of the week. The device checks for an alarm match once per second. When the RTC register values match alarm register settings, the corresponding Alarm Flag 'A1F' or 'A2F' bit is set to logic 1. If the corresponding Alarm Interrupt Enable 'A1IE' or 'A2IE' is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the SQW/INT) signal. If the BBSQI bit is set to 1, the INT output activates while the part is being powered by V_{BACKUP}. The alarm output remains active until the alarm flag is cleared by the user.

DY/DT	ALARM 1 REGISTER MASK BITS (Bit 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

SPECIAL-PURPOSE REGISTERS

The CD13S39 has two additional registers (control and status) that control the RTC, alarms, and square-wave output.

CONTROL REGISTER (0EH)

The control register controls the operation of the SQW/OUT pin and provides oscillator status.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EOSC	0	BBSQI	RS2	RS1	INTCN	A2IE	A1IE

Bit 7: Enable Oscillator (EOSC). This bit when set to logic 0 starts the oscillator. When this bit is set to a logic 1, the oscillator is stopped. This bit is enabled (logic 0) when power is first applied.

Bit 5: Battery-Backed Square-Wave and Interrupt Enable (BBSQI). This bit when set to a logic 1 enables the square wave or interrupt output when VCC is absent and the CD13S39 is being powered by the VBACKUP pin. When BBSQI is a logic 0, the SQW/INT pin goes high impedance when VCC falls below the power-fail trip point. This bit is disabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. Table 5 shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

Table 5. SQW/INT Output

INTCN	RS2	RS1	SQW/INT Output	A2IE	A1IE
0	0	0	1Hz	X	X
0	0	1	4.096kHz	X	X
0	1	0	8.192kHz	X	X
0	1	1	32.768kHz	X	X
1	X	X	A1F	0	1
1	X	X	A2F	1	0
1	X	X	A2F+A1F	1	1

Bit 2: Interrupt Control (INTCN). This bit controls the relationship between the two alarms and the interrupt output pins. When the INTCN bit is set to logic 1, a match between the timekeeping registers and the alarm 1 or alarm 2 registers activate the SQW/INT pin (provided that the alarm is enabled). When the INTCN bit is set to logic 0, a square wave is output on the SQW/INT pin. This bit is set to logic 0 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE). When set to a logic 1, this bit permits the Alarm 2 Flag (A2F) bit in the status register to assert SQW/INT (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE). When set to logic 1, this bit permits the Alarm 1 Flag (A1F) bit in the status register to assert SQW/INT (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate an interrupt signal. The A1IE bit is disabled (logic 0) when power is first applied.

Status REGISTER (0FH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OSF	0	0	0	0	0	A2F	A1F

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period of time and may be used to judge the validity of the clock and date data. This bit is edge triggered and is set to logic 1 when the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.

2) The voltage on both VCC and VBACKUP are insufficient to support oscillation.

3) The EOSC bit is turned off.

4) External influences on the crystal (e.g., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to a logic 0.

Bit 1: Alarm 2 Flag (A2F). A logic 1 in the Alarm 2 Flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/INT pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F). A logic 1 in the Alarm 1 Flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is a logic 1 and the INTCN bit is set to a logic 1, the SQW/INT pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

TRICKLE CHARGER REGISTER (10H)

The simplified schematic in Figure 5 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode-select (DS) bits (bits 2 and 3) select whether or not a diode is connected between VCC and VBACKUP. The ROUT bits (bits 0 and 1) select the value of the resistor connected between VCC and VBACKUP. Table 6 shows the bit values.

Table 6. Trickle Charger Register (10H)

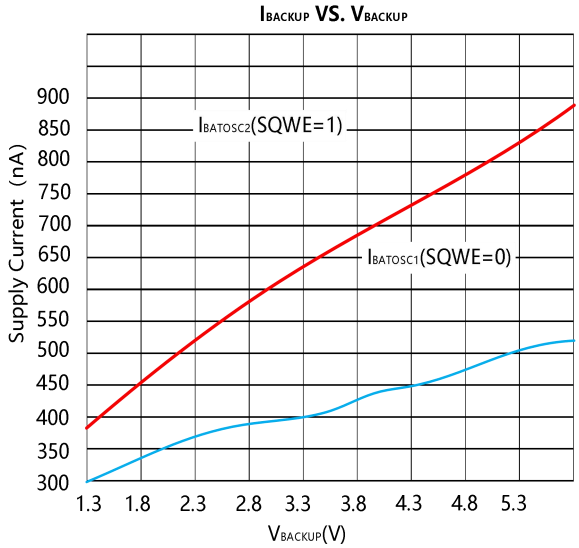
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Disabled
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	No diode, 250Ω resistor
1	0	1	0	0	1	0	1	One diode, 250Ω resistor
1	0	1	0	1	0	0	1	No diode, 2kΩ resistor
1	0	1	0	0	1	1	0	One diode, 2kΩ resistor

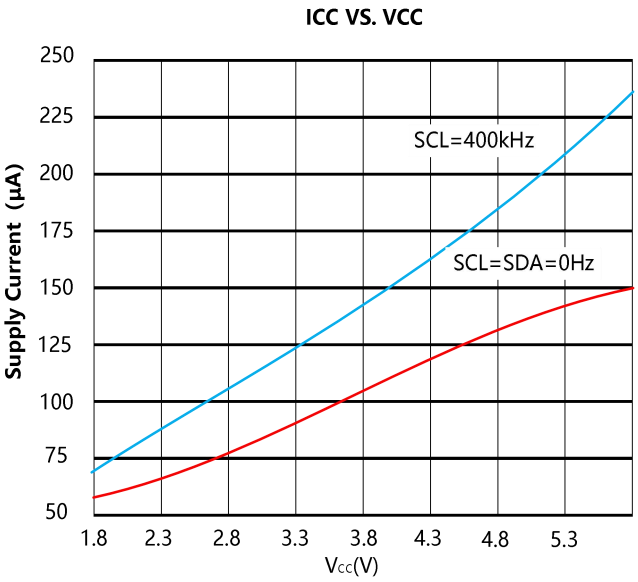
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Initial power-up values

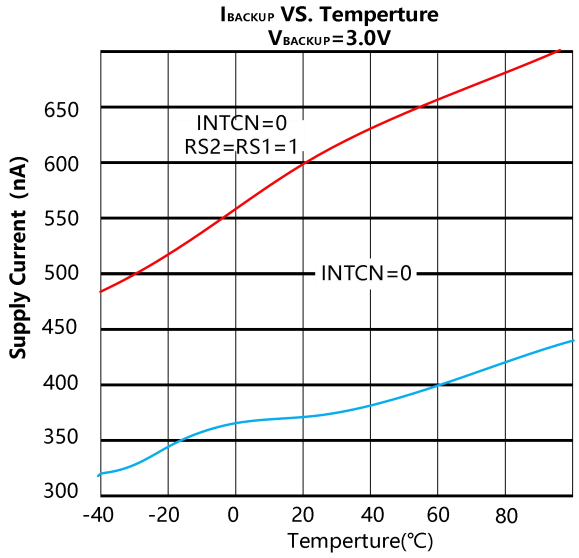
The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a 3.3V system power supply is applied to VCC and a super cap is connected to VBACKUP. Also assume that the trickle charger has been enabled with a diode and resistor R2 between VCC and VBACKUP. The maximum current IMAX would therefore be calculated as follows: IMAX = (3.3V - diode drop) / R2 ≈ (3.3V - 0.7V) / 2kΩ ≈ 1.3mA

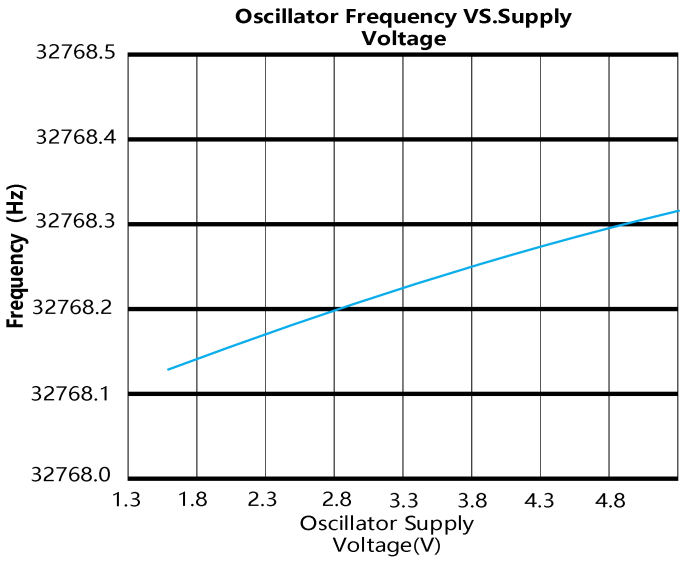
As the super cap or battery charges, the voltage drop between VCC and VBACKUP decreases and therefore the charge current decreases.

Typical Electrical Characteristics









Chinese version:CD13S39

Package Outline Dimensions

SOP-8

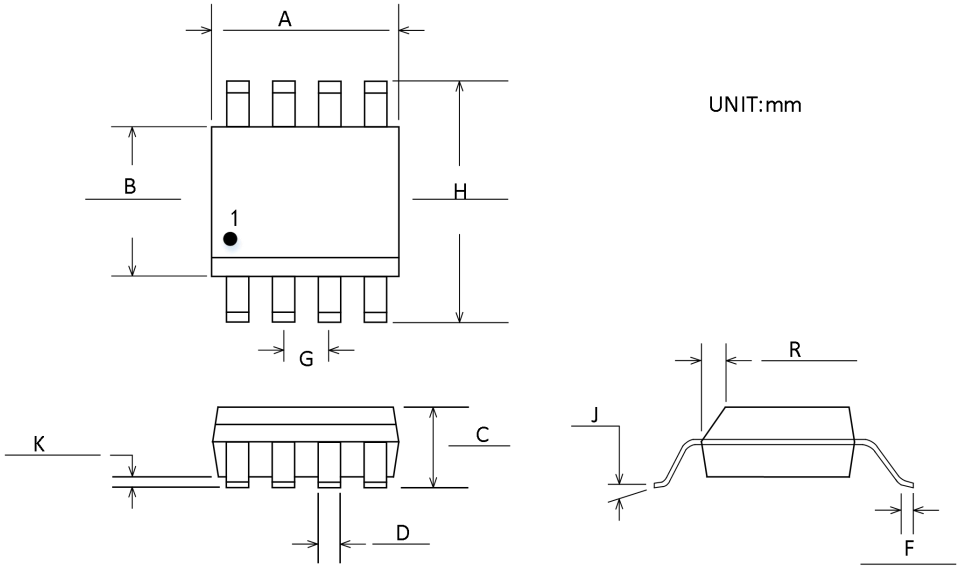


Figure 4 . 8-Lead Outline Package [SOP-8]

Symbol	Dimensions (mm)	
	Min	Max
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.31	0.51
F	0.40	1.27
G	1.27BSC	
H	5.80	6.20
J	0°	8°
K	0.10	0.25
R	0.25	0.50

Chinese version:CD13S39

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD13S39AS8	-40℃~85℃	SOP-8	Tape and Reel, 2500
CD13S39AS8-RL	-40℃~85℃	SOP-8	Tape and Reel, 3000
CD13S39AS8-REEL	-40℃~85℃	SOP-8	Tape and Reel, 4000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.25	Initial version	Regular update	WW	LYL	