CD32S32A

Ultra-high precision, I²C RTC, integrated crystal and SRAM

Version: Rev 1.0.0 Date: 2025-6-25

Features

- Accuracy ±2ppm from 0°C to +40°C
- Accuracy ±3.5ppm from -40°C to +85°C
- Battery Backup Input for Continuous Timekeeping
- Operating Temperature Ranges
  Commercial: 0°C to +70°C
  Industrial: -40°C to +85°C
- 236 Bytes of Battery-Backed SRAM
- Low-Power Consumption
- Real-Time Clock Counts Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap Year Compensation Valid Up to 2099
- Two Time-of-Day Alarms
- Programmable Square-Wave Output
- Fast (400kHz) I2C Interface
- 3.3V Operation
- Digital Temp Sensor Output: ±3°C Accuracy
- Register for Aging Trim
- RST Input/Output
- 300-Mil, 20-Pin SO Package

Application

- Servers
- Telematics
- Utility Power Meters
- GPS

Description

The CD32S32A is a low-cost temperature-compensated crystal oscillator (TCXO) with a very accurate, temperature-compensated, integrated real-time clock (RTC) and 236 bytes of battery-backed SRAM. Additionally, the CD32S32A incorporates a battery input and maintains accurate timekeeping when main power to the device is interrupted. The integration of the crystal resonator enhances the long-term accuracy of the device as well as reduces the piece-part count in a manufacturing line. The CD32S32A is available in commercial and industrial temperature ranges, and is offered in an industry-standard 20-pin, 300-mil SO package. The RTC maintains seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Two programmable time-ofday alarms and a programmable square-wave output are provided. Address and data are transferred serially through an I2C bidirectional bus. A precision temperature-compensated voltage reference and comparator circuit monitors the status of VCC to detect power failures, to provide a reset output, and to automatically switch to the backup supply when necessary. Additionally, the RST pin is monitored as a pushbutton input for generating a µP reset.

Contents

Pin Configurations

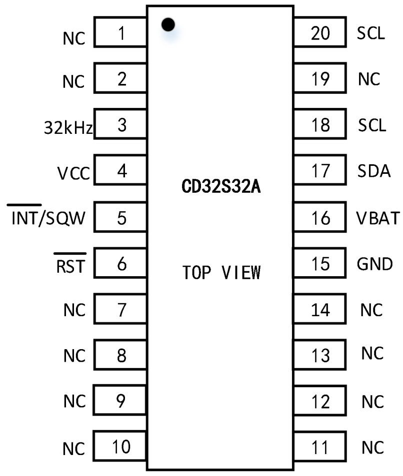

Figure 1. SOP20 Pin Configuration

Pin Description

Table 1. Pin description

Pin No.	Pin Name	Description
1,2,7-14,19	NC	No Connection. Not connected internally. Must be connected to ground.
3	32kHz	32kHz Push-Pull Output. If disabled with either EN32kHz = 0 or BB32kHz = 0, the state of the 32kHz pin will be low.
4	VCC	DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1μF to 1.0μF capacitor.
5	$\overline{\text{INT}}$/SQW	Active-Low Interrupt or Square-Wave Output. This open-drain pin requires an external pullup resistor. It can be left open if not used. This multifunction pin is determined by the state of the INTCN bit in the Control Register (0Eh). When INTCN is set to logic 0, this pin outputs a square wave and its frequency is determined by RS2 and RS1 bits. When INTCN is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the INT/SQW pin (if the alarm is enabled). Because the INTCN bit is set to logic 1 when power is first applied, the pin defaults to an interrupt output with alarms disabled. The pullup voltage can be up to 5.5V,regardless of the voltage on VCC. If not used, this pin can be left unconnected.
6	RST	Active-Low Reset. This pin is an open-drain input/output. It indicates the

		status of VCC relative to the VPF specification. As VCC falls below VPF, the RST pin is driven low. When VCC exceeds VPF, for tRST, the RST pin is driven high impedance. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50k nominal value pullup resistor to VCC. No external pullup resistors should be connected. If the crystal oscillator is disabled, tRST is bypassed and RST immediately goes high.
15	GND	Ground
16	V_{BAT}	Backup Power-Supply Input. When using the device with the VBAT input as the primary power source, this pin should be decoupled using a 0.1µF to 1.0µF low-leakage capacitor. When using the device with the VBAT input as the backup power source, the capacitor is not required. If VBAT is not used, connect to ground. The device is UL recognized to ensure against reverse charging when used with a primary lithium battery.
17	SDA	Serial Data Input/Output. This pin is the data input/output for the I2C serial interface. This open-drain pin requires an external pullup resistor. The pullup voltage can be up to 5.5V, regardless of the voltage on VCC.
18,20	SCL	Serial Clock Input. This pin is the clock input for the I2C serial interface and is used to synchronize data movement on the serial interface. Up to 5.5V can be used for this pin, regardless of the voltage on VCC

Functional Block diagram

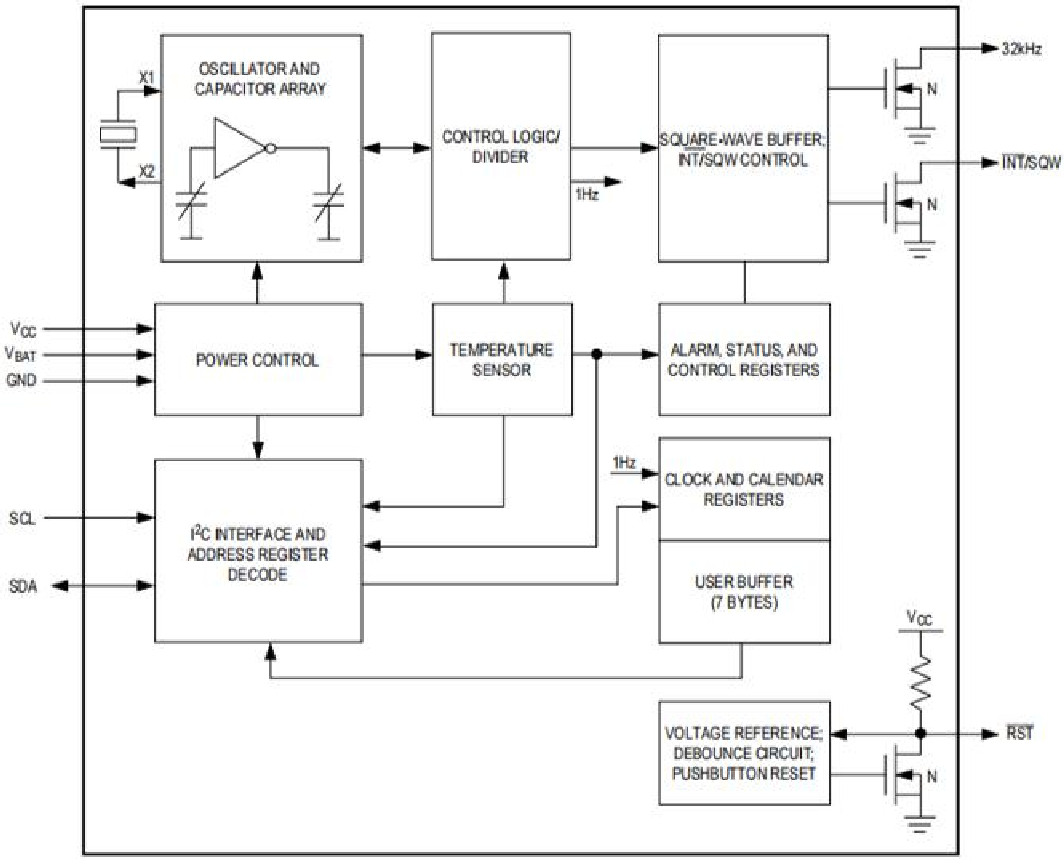

Figure 2. Functional Block Diagram

Typical Application Circuit

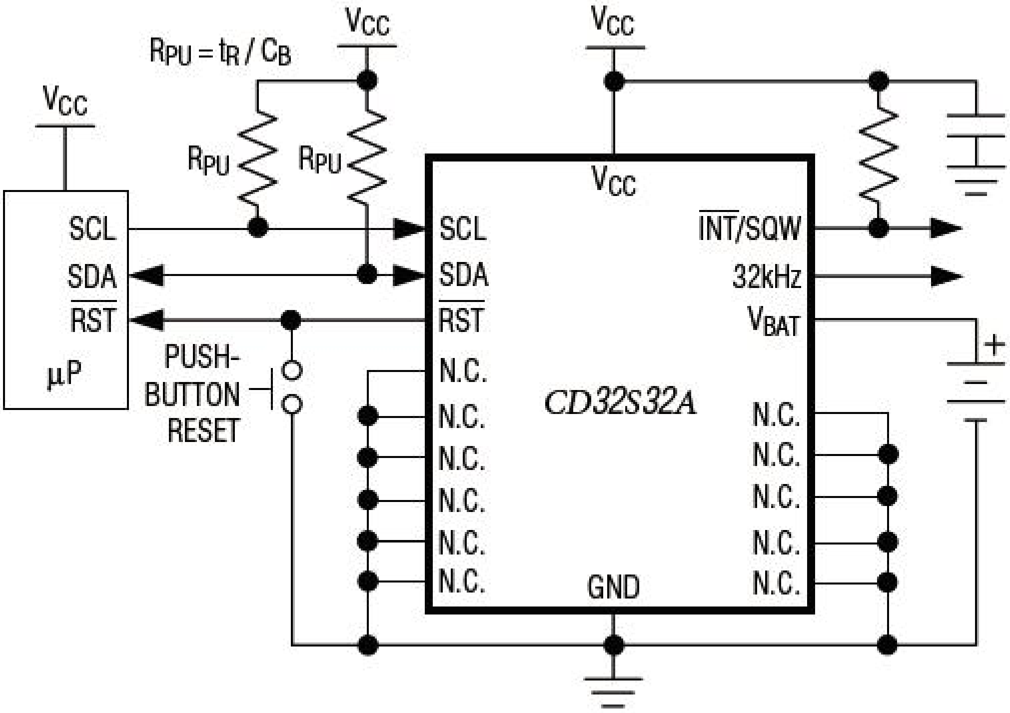

Figure 3. Typical Application Circuit Diagram

Absolute Maximum Ratings

Parameter	Range
Voltage Range on Any Pin Relative to GND	−0.3 V to +6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +85°C
Lead Temperature (soldering, 10s)	260°C
Soldering Temperature (reflow)	260°C
Junction Temperature	125°C
Junction-to-Ambient Thermal Resistance ((θJA)	55.1°C/W
Junction-to-Case Thermal Resistance ((θJC)	24°C/W

Operating Temperatures Range

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 2, 3)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	VCC		2.3	3.3	5.5	V
	VBAT		2.3	3.0	5.5	
Logic0 Input SDA, SCL	V_{IL}		-0.3		+0.3V_{CC}	V
Logic1 Input SDA, SCL	V_{IH}		0.7V_{CC}		V_{CC}+0.3	V

DC Electrical Characteristics

(V_{CC} = 2.3V to 5.5V, V_{CC} = Active Supply (see Table 1), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

(Typical values are at VCC = 3.3V, V_{BAT} = 3.0V, and TA = +25°C, unless otherwise noted.) (Notes 2, 3)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Active Supply Current	I_{CCA}	32kHz output off(Notes 4, 5)VCC = 3.3V	--	--	200	μA
		32kHz output off(Notes 4, 5)VCC = 5.5V	--	--	325	μA
Standby Supply Current	I_{CCS}	I2C bus inactive, 32kHz output on, SQW output off (Note 5)VCC = 3.3V	--	--	120	μA
		I2C bus inactive, 32kHz output on, SQW output off (Note 5)VCC = 5.5V	--	--	160	
Temperature Conversion Current	$I_{CCSCONV}$	I2C bus inactive, 32kHz output on, SQW output off,VCC = 3.3V	--	--	500	μA
		I2C bus inactive, 32kHz output on, SQW output off,VCC = 5.5V	--	--	600	μA
Power-Fail Voltage	V_{PF}		2.45	2.575	2.70	V

ACTIVE SUPPLY (Table 1) (2.3V to 5.5V, TA = -40°C to +85°C, unless otherwise noted) (Note 2)						
Logic 1 Output, 32kHz	V_{OH}		2.0	--	--	V
IOH = -1mA		Active supply > 3.3V,				
IOH = -0.75mA		3.3V > active supply > 2.7V,				
IOH = -0.14mA		2.7V > active supply > 2.3V				
Logic 0 Output, INT/SQW, SDA	V_{OL}	IOL = 3mAs	--	--	0.4	V
Logic 0 Output, $\overline{RST}$, 32kHz	V_{OL}	IOL = 1mA	--	--	0.4	V
Output Leakage Current 32kHz, INT/SQW, SDA	I_{LO}	Output high impedance	-1	0	+1	μA
Input Leakage SCL	I_{LI}		-1	--	+1	μA
$\overline{RST}$ Pin I/O Leakage	I_{OL}	RST high impedance (Note 6)	-200	--	+10	μA
TCXO						
Output Frequency	f_{OUT}	VCC = 3.3V or VBAT = 3.3V	--	32.768	--	kHz
Duty Cycle		2.97V ≤ VCC < 3.63	31	--	69	%
Frequency Stability vs. Temperature	$\Delta f/f_{OUT}$	VCC = 3.3V or VBAT = 3.3V, aging offset = 00h	--	--	±3.5	ppm
Frequency Stability vs. Voltage	Δf/V		--	1	--	ppm/V
Trim Register Frequency Sensitivity per LSB	Δf/LSB		--	0.1	--	ppm
Temperature Accuracy	Temp	VCC = 3.3V or VBAT = 3.3V	-3	--	+3	℃
Crystal Aging	Δf/fO	After reflow, not production tested，First year	--	±1.0	--	ppm
		After reflow, not production tested，0–10 years	--	±5.0	--	ppm

(V_{CC} = 2.3V to 5.5V, V_{CC} = Active Supply (see Table 1), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

(Typical values are at VCC = 3.3V, V_{BAT} = 3.0V, and TA = +25°C, unless otherwise noted.) (Notes 2, 3)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Active Supply Current	I_{CCA}	32kHz output off(Notes 4, 5)VCC = 3.3V	--	--	200	μA
		32kHz output off(Notes 4, 5)VCC = 5.5V	--	--	325	μA
Standby Supply Current	I_{CCS}	I2C bus inactive, 32kHz output on, SQW output off (Note 5)VCC = 3.3V	--	--	120	μA
		I2C bus inactive, 32kHz output on, SQW output off (Note 5)VCC = 5.5V	--	--	160	
Temperature Conversion Current	$I_{CCSCONV}$	I2C bus inactive, 32kHz output on, SQW output off,VCC = 3.3V	--	--	500	μA
		I2C bus inactive, 32kHz output on, SQW output off,VCC = 5.5V	--	--	600	μA
Power-Fail Voltage	V_{PF}		2.45	2.575	2.70	V
ACTIVE SUPPLY (Table 1) (2.3V to 5.5V, TA = -40°C to +85°C, unless otherwise noted) (Note 2)						
Logic 1 Output, 32kHz	V_{OH}		2.0	--	--	V
IOH = -1mA		Active supply > 3.3V,				
IOH = -0.75mA		3.3V > active supply > 2.7V,				
IOH = -0.14mA		2.7V > active supply > 2.3V				
Logic 0 Output, INT/SQW, SDA	V_{OL}	IOL = 3mAs	--	--	0.4	V
Logic 0 Output, RST, 32kHz	V_{OL}	IOL = 1mA	--	--	0.4	V
Output Leakage Current 32kHz, INT/SQW, SDA	I_{LO}	Output high impedance	-1	0	+1	μA
Input Leakage SCL	I_{LI}		-1	--	+1	μA
RST Pin I/O Leakage	I_{OL}	RST high impedance (Note 6)	-200	--	+10	μA
TCXO						
Output Frequency	f_{OUT}	VCC = 3.3V or VBAT = 3.3V	--	32.768	--	kHz
Duty Cycle		2.97V ≤ VCC < 3.63	31	--	69	%
Frequency Stability vs.	$\Delta f/f_{OUT}$	VCC = 3.3V or VBAT = 3.3V, aging offset = 00h	--	--	±3.5	ppm

Temperature						
Frequency Stability vs. Voltage	Δf/V		--	1	--	ppm/V
Trim Register Frequency Sensitivity per LSB	Δf/LSB		--	0.1	--	ppm
Temperature Accuracy	Temp	VCC = 3.3V or VBAT = 3.3V	-3	--	+3	℃
Crystal Aging	Δf/fO	After reflow, not production tested，First year	--	±1.0	--	ppm
		After reflow, not production tested，0–10 years	--	±5.0	--	ppm

(V_{CC} = 0V, V_{BAT} = 2.3V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Active Battery Current	IBATA	$\overline{EOSC}$ = 0,BBSQW = 0, SCL = 400kHz (Note 5),BB32kH z = 0	VBAT = 3.3V	--	--	80	μA
			VBAT = 5.5V	--	--	200	
Timekeeping Battery Current	IBATT	$\overline{EOSC}$ = 0, BBSQW = 0, SCL = SDA = 0V, BB32kHz = 0, CRATE0 = CRATE1 = 0	VBAT = 3.4V	--	1.5	2.5	μA
			VBAT = 5.5V	--	15	3.0	
Temperature Conversion Current	IBATTC	$\overline{EOSC}$ = 0, BBSQW = 0, SCL = SDA = 0V		--	--	600	μA
Data-Retention Current	IBATTDR	$\overline{EOSC}$ = 1, SCL = SDA = 0V, +25°C		--	--	100	nA

AC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$or V_{BAT} = $V_{BAT(MIN)}$ to $V_{BAT(MAX)}$, V_{BAT} > V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL Clock Frequency	f_{SCL}	Fast mode	100	--	400	kHz
		Standard mode	0	--	100	
Bus Free Time Between	t_{BUF}	Fast mode	1.3	--	--	μs

STOP and START Condition		Standard mode	4.7	--	--	
Hold Time (Repeated) START Condition (Note 7)	$t_{HD:STA}$	Fast mode	0.6	--	--	μs
		Standard mode	4.0	--	--	
LOW Period of SCL Clock	t_{LOW}	Fast mode	1.3	--	25000	μs
		Standard mode	4.7	--	25000	
Data Hold Time (Notes 8, 9)	$t_{HD:DAT}$	Fast mode	0	--	0.9	μs
		Standard mode	0	--	0.9	
Data Setup Time (Note 10)	$t_{SU:DAT}$	Fast mode	100	--	--	ns
		Standard mode	250	--	--	
START Setup Time	$t_{SU:STA}$	Fast mode	0.6	--	--	ns
		Standard mode	4.7	--	--	
Rise Time of Both SDA and SCL Signals (Note 11)	t_R	Fast mode	20+0.1 C_B	--	300	ns
		Standard mode	20+0.1 C_B	--	1000	
Fall Time of Both SDA and SCL Signals (Note 11)	t_F	Fast mode	20+0.1 C_B	--	300	ns
		Standard mode	20+0.1 C_B	--	1000	
Setup Time for STOP Condition	$t_{SU:STO}$	Fast mode	0.6	--	--	μs
		Standard mode	4.7	--	--	
Capacitive Load for Each Bus Line	C_B	(Note 11)	--	--	400	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$		--	10	--	pF
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 12)	--	100	--	ms
Pulse Width of Spikes That Must Be Suppressed by the Input Filter	t_{SP}		--	30	--	ns
Pushbutton Debounce	PB_{DB}		--	250	--	ms
Reset Active Time	t_{RST}		--	250	--	ms
Temperature Conversion Time	t_{CONV}		--	125	200	ms

Power-Up/Power-Down Characteristics

(T_A = T_{MIN} to T_{MAX})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Recovery at Power-Up	t_{REC}	--	125	300	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}	300	--	--	µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}	0	--	--	µs

WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a fourlayer board. For detailed information on package thermal considerations,

Note 2: Limits at -40°C are guaranteed by design and not production tested.

Note 3: All voltages are referenced to ground.

Note 4: ICCA—SCL clocking at max frequency = 400kHz.

Note 5: Current is the averaged input current, which includes the temperature conversion current.

Note 6: The RST pin has an internal 50kΩ (nominal) pullup resistor to VCC.

Note 7: After this period, the first clock pulse is generated.

Note 8: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIH(MIN) of the SCL signal)
to bridge the undefined region of the falling edge of SCL.

Note 9: The maximum tHD:DAT needs only to be met if the device does not stretch the low period (tLOW) of the SCL signal.

Note 10: A fast-mode device can be used in a standard-mode system, but the requirement tSU:DAT ≥ 250ns must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line tR(MAX) + tSU:DAT = 1000 + 250 = 1250ns before the SCL line is released.

Note 11: CB—total capacitance of one bus line in pF.

Note 12: Minimum operating frequency of the I2C interface is imposed by the timeout period.

Note 13: The parameter tOSF is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of 0V ≤ VCC ≤ VCC(MAX) and 2.3V ≤ VBAT ≤ 3.4V.

Note 14: This delay only applies if the oscillator is enabled and running. If the EOSC bit is 1, tREC is bypassed and RST immediately

Timing

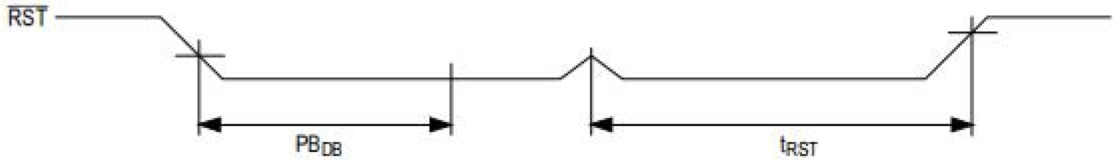

Figure 4. Pushbutton Reset Timing

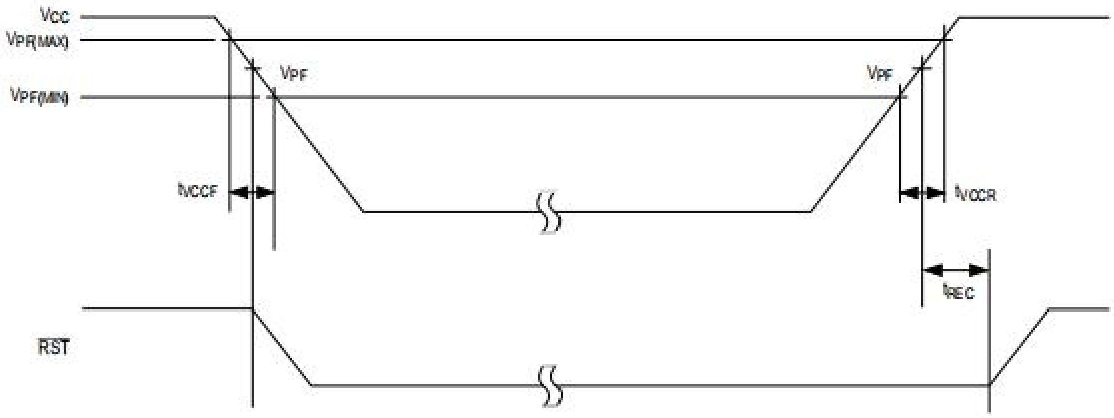

Figure 5. Power-Switch Timing

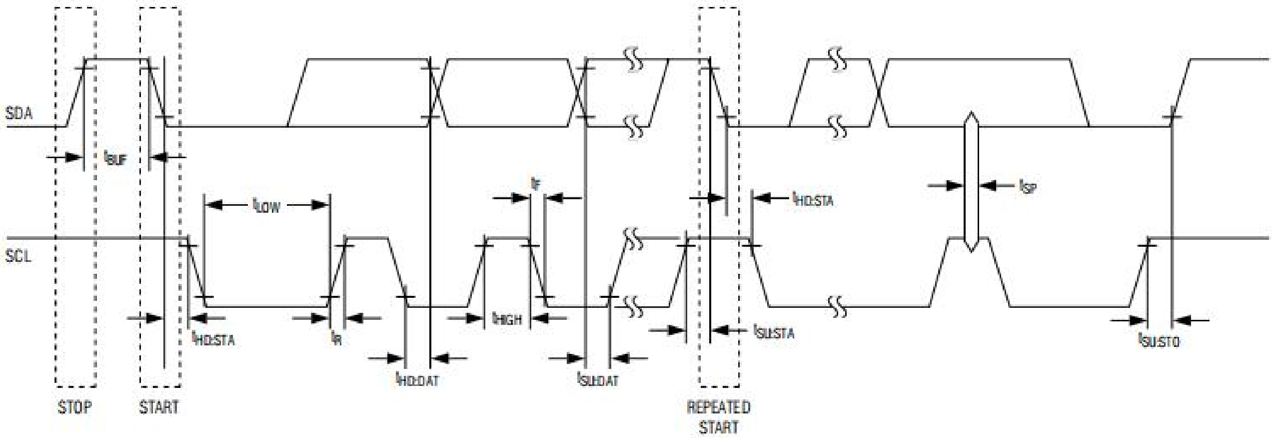

Figure 6. Data Transfer on I2C Serial Bus

Typical Electrical Characteristics

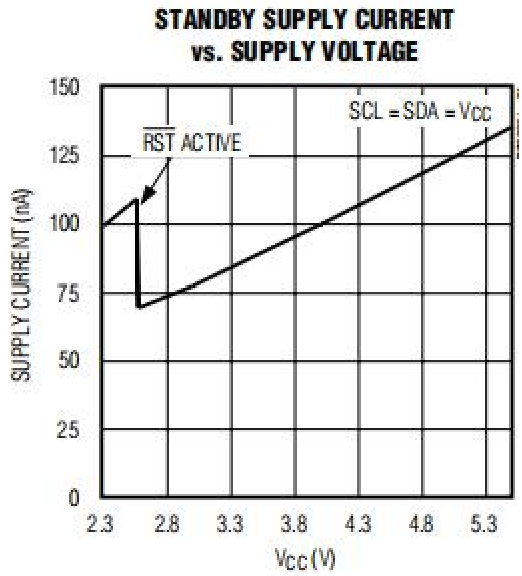

Figure 7. STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

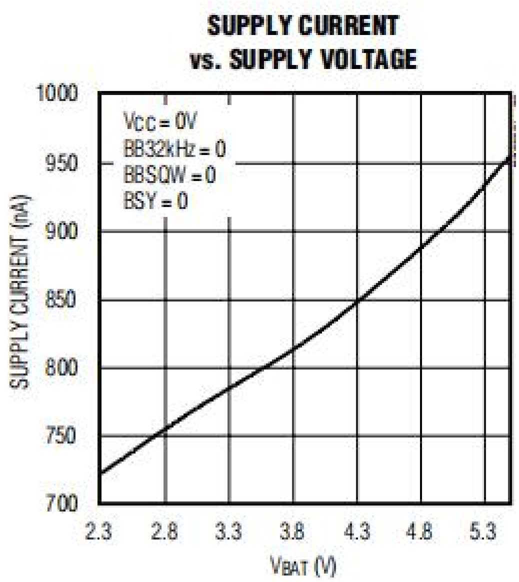

Figure 8. SUPPLY CURRENT vs. SUPPLY VOLTAGE

DETAILED DESCRIPTION

The CD32S32A is a serial RTC driven by a temperature compensated 32kHz crystal oscillator. The TCXO provides a stable and accurate reference clock, and maintains the RTC to within ±2 minutes per year accuracy from -40°C to +85°C. The TCXO frequency output is available at the 32kHz pin. The RTC is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. The INT/SQW provides either an interrupt signal due to alarm conditions or a square-wave output. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. The internal registers are accessible though an I2C bus interface. A temperature-compensated voltage reference and comparator circuit monitors the level of VCC to detect power failures and to automatically switch to the backup supply when necessary. The RST pin provides an external pushbutton function and acts as an indicator of a power-fail event. Also available are 236 bytes of general-purpose battery-backed SRAM.

Operation

The block diagram shows the main elements of the CD32S32A. The eight blocks can be grouped into four functional groups: TCXO, power control, pushbutton function, and RTC. Their operations are described separately in the following sections.

32kHz TCXO

The temperature sensor, oscillator, and control logic form the TCXO. The controller reads the output of the on-chip temperature sensor and uses a lookup table to determine the capacitance required, adds the aging correction in AGE register, and then sets the capacitance selection registers. New values, including changes to the AGE register, are loaded only when a change in the temperature value occurs. The temperature is read on initial application of VCC and once every 64 seconds (default, see the description for CRATE1 and CRATE0 in the control/status register) afterwards.

Power Control

This function is provided by a temperature-compensated voltage reference and a comparator circuit that monitors the VCC level. When VCC is greater than VPF, the part is powered by VCC. When VCC is less than VPF but greater than VBAT, the CD32S32A is powered by VCC. If VCC is less than VPF and is less than VBAT, the device is powered by VBAT. See Table 1.

Table 1. Power Control

Supply Condition	Powered By
$V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$	V_{BAT}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$	V_{CC}

To preserve the battery, the first time VBAT is applied to the device, the oscillator does not start up and no temperature conversions take place until VCC exceeds VPF or until a valid I2C address is written to the part. After the first time VCC is ramped up, the oscillator starts up and the VBAT source powers the oscillator during power-down and keeps the oscillator running. When the CD32S32A switches to VBAT, the oscillator may be disabled by setting the EOSC bit.

VBAT Operation

There are several modes of operation that affect the amount of VBAT current that is drawn. While the device is powered by VBAT and the serial interface is active, active battery current, IBATA, is drawn. When the serial interface is inactive, timekeeping current (IBATT), which includes the averaged temperature conversion current, IBATTC, is used (refer to Application Note 3644: Power Considerations for Accurate Real-Time Clocks for details). Temperature conversion current, IBATTC, is specified since the system must be able to support the periodic higher current pulse and still maintain a valid voltage level. Data retention current, IBATTDR, is the current drawn by the part when the oscillator is stopped (EOSC = 1). This mode can be used to minimize battery requirements for times when maintaining time and date information is not necessary, e.g., while the end system is waiting to be shipped to a customer.

Pushbutton Reset Function

The CD32S32A provides for a pushbutton switch to be connected to the RST output pin. When the CD32S32A is not in a reset cycle, it continuously monitors the RST signal for a low going edge. If an edge transition is detected, the CD32S32A debounces the switch by pulling the RST low. After the internal timer has expired (PBDB), the CD32S32A continues to monitor the RST line. If the line is still low, the CD32S32A continuously monitors the line looking for a rising edge. Upon detecting release, the CD32S32A forces the RST pin low and holds it low for tRST. The same pin, RST, is used to indicate a power-fail condition. When VCC is lower than VPF, an internal powerfail signal is generated, which forces the RST pin low. When VCC returns to a level above VPF, the RST pin is held low for tREC to allow the power supply to stabilize. If the oscillator is not running (see the Power Control section) when VCC is applied, tREC is bypassed and RST immediately goes high. Assertion of the RST output, whether by pushbutton or power-fail detection, does not affect the internal operation of the CD32S32A.

Real-Time Clock

With the clock source from the TCXO, the RTC provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. The clock provides two programmable time-of-day alarms and a programmable square-wave output. The INT/SQW pin either generates an interrupt due to alarm condition or outputs a square-wave signal and the selection is controlled by the bit INTCN.

SRAM

The CD32S32A provides 236 bytes of general-purpose battery-backed read/write memory. The I2C address ranges from 14h to 0FFh. The SRAM can be written or read whenever VCC or VBAT is greater than the minimum operating voltage.

Address Map

During a multibyte access, when the address pointer reaches the end of the register space (0FFh), it wraps around to location 00h. On an I2C START or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to reread the registers in case the main registers update during a read.

I2C Interface

The I2C interface is accessible whenever either VCC or VBAT is at a valid level. If a microcontroller connected to the CD32S32A resets because of a loss of VCC or other event, it is possible that the microcontroller and CD32S32A I2C communications could become unsynchronized, e.g., the microcontroller resets while reading data from the CD32S32A. When the microcontroller resets, the CD32S32A I2C interface may be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition. If SCL is held low for greater than tIF, the internal I2C interface is reset. This limits the minimum frequency at which the I2C interface can be operated. If data is being written to the device when the interface timeout is exceeded, prior to the acknowledge, the incomplete byte of data is not written.

Address Map for CD32S32A Timekeeping Registers and SRAM

ADDRESS	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	FUNCTION	RANGE
00h	0	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Hours	1–12 + $\overline{AM}$/PM 00–23
03h	0	0	0	0	0	Day			Day	1–7
04h	0	0	10 Date		Date				Date	1–31
05h	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century
06h	10 Year				Year				Year	00–99
07h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Alarm 1 Hours	1–12 + $\overline{AM}$/PM 00–23
0Ah	A1M4	DY/$\overline{DT}$	10 Date		Day Date				Alarm 1 Day Alarm 1 Date	1–7 1–31
0Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hour	10 Hour	Hour				Alarm 2 Hours	1–12 + $\overline{AM}$/PM 00–23
0Dh	A2M4	DY/$\overline{DT}$	10 Date		Day Date				Alarm 2 Day Alarm 2 Date	1–7 1–31
0Eh	$\overline{EOSC}$	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0Fh	OSF	BB32kHz	CRATE1	CRATE0	EN32kHz	BSY	A2F	A1F	Control/Status	—
10h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Aging Offset	—
11h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	MSB of Temp	—
12h	DATA	DATA	0	0	0	0	0	0	LSB of Temp	—
13h	0	0	0	0	0	0	0	0	Not used	Reserved for test
14h–0FFh	x	x	x	x	x	x	x	x	SRAM	00h–0FFh

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Figure 1 illustrates the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in binary-coded decimal (BCD) format. The CD32S32A can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, 12-hour mode is selected. In 12- hour mode, bit 5 is the AM/PM bit with logic-high being PM. In 24-hour mode, bit 5 is the 20-hour bit (20–23hours). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are userdefined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any START and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read. The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the CD32S32A. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer, provided the oscillator is already running.

Alarms

The CD32S32A contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the alarm enable and INTCN bits of the control register) to activate the INT/SQW output on an alarm match condition. Bit 7 of each of the time-ofday/date alarm registers are mask bits (Table 2). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-ofday/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 shows the possible settings. Configurations not listed in the table result in illogical operation. The DY/DT bits (bit 6 of the alarm day/date registers)
control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/DT is written to logic 0, the alarm will be the result of a match with date of the month. If DY/DT is written to logic 1, the alarm will be the result of a match with day

of the week. When the RTC register values match alarm register settings, the corresponding Alarm Flag 'A1F' or 'A2F' bit is set to logic 1. If the corresponding Alarm Interrupt Enable 'A1IE' or 'A2IE' is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the INT/SQW signal. The match is tested on the onceper-second update of the time and date registers.

Table 2. Alarm Mask Bits

DY/DT	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/DT	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A1M4	A1M3	A1M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
0	0	0	0	Alarm when day, hours, and minutes match

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EOSC	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE
Por	0	0	0	1	1	1	0	0

*POR is defined as the first application of power to the device, either VBAT or VCC.

Special-Purpose Registers

The CD32S32A has two additional registers (control and control/status) that control the real-time clock, alarms, and square-wave output.

Control Register (0Eh)

Bit 7: Enable Oscillator (EOSC). When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped when the CD32S32A switches to battery power. This bit is clear (logic 0) when power is first applied. When the CD32S32A is powered by VCC, the oscillator is always on regardless of the status of the EOSC bit. When EOSC is disabled, all register data is static.

Bit 6: Battery-Backed Square-Wave Enable (BBSQW).

When set to logic 1 with INTCN = 0 and VCC < VPF, this bit enables the square wave. When BBSQW is logic 0, the INT/SQW pin goes high impedance when VCC < VPF. This bit is disabled (logic 0) when power is first applied.

Bit 5: Convert Temperature (CONV).

Setting this bit to 1 forces the temperature sensor to convert the temperature into digital code and execute the TCXO algorithm to update the capacitance array to the oscillator. This can only happen when a conversion is not already in progress. The user should check the status bit BSY before forcing the controller to start a new TCXO execution. A user-initiated temperature conversion does not affect the internal 64-second (default interval) update cycle. A user-initiated temperature conversion does not affect the BSY bit for approximately 2ms. The CONV bit remains at a 1 from the time it is written until the conversion is finished, at which time both CONV and BSY go to 0. The CONV bit should be used when monitoring the status of a user-initiated conversion.

Bits 4 and 3: Rate Select (RS2 and RS1).

These bits control the frequency of the square-wave output when the square wave has been enabled. The following table shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (8.192kHz) when power is first applied.

SQUARE-WAVE OUTPUT FREQUENCY

RS2	RS1	SQUARE-WAVE OUTPUT FREQUENCY
0	0	1Hz
0	1	1.024kHz
1	0	4.096kHz
1	1	8.192kHz

Bit 2: Interrupt Control (INTCN).

This bit controls the INT/SQW signal. When the INTCN bit is set to logic 0, a square wave is output on the INT/SQW pin. When the INTCN bit is set to logic 1, a match between the time keeping registers and either of the alarm registers activates the INT/SQW (if the alarm is also enabled). The corresponding alarm flag is always set regardless of the state of the INTCN bit. The INTCN bit is set to logic 1 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE).

When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert INT/SQW (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE).

When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert INT/SQW (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate the INT/SQW signal. The A1IE bit is disabled (logic 0) when power is first applied.

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OSF	BB32kHz	CRATE1	CRATE0	EN32kHz	BSY	A2F	A1F
Por	1	1	0	0	1	0	0	0

Control/Status Register (0Fh)

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and may be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltages present on both VCC and VBAT are insufficient to support oscillation.
3) The EOSC bit is turned off in battery-backed mode.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0.

Bit 6: Battery-Backed 32kHz Output (BB32kHz).

This bit enables the 32kHz output when powered from VBAT (provided EN32kHz is enabled). If BB32kHz = 0, the 32kHz output is low when the part is powered by VBAT.

Bits 5 and 4: Conversion Rate (CRATE1 and CRATE0).

These two bits control the sample rate of the TCXO. The sample rate determines how often the temperature sensor makes a conversion and applies compensation to the oscillator. Decreasing the sample rate decreases the overall power consumption by decreasing the frequency at which the temperature sensor operates. However, significant temperature changes that occur between samples may not be completely compensated for, which reduce overall accuracy. When a new conversion rate is written to the register, it may take up to the new conversion rate time before the conversions occur at the new rate.

Bit 3: Enable 32kHz Output (EN32kHz).

This bit indicates the status of the 32kHz pin. When set to logic 1, the 32kHz pin is enabled and outputs a 32.768kHz square-wave signal. When set to logic 0, the 32kHz pin goes low. The initial power-up state of this bit is logic 1, and a 32.768kHz square-wave signal appears at the 32kHz pin after a power source is applied to the CD32S32A (if the oscillator is running).

Bit 2: Busy (BSY). This bit indicates the device is busy executing TCXO functions. It goes to logic 1 when the conversion signal to the temperature sensor is asserted and then is cleared when the conversion is complete.

Bit 1: Alarm 2 Flag (A2F).

A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is logic 1 and the INTCN bit is set to logic 1, the INT/SQW pin is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F).

A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is logic 1 and the INTCN bit is set to logic 1, the INT/SQW pin is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Carte1	Carte0	SAMPLE RATE (seconds)
0	0	64
0	1	128
1	0	256
1	1	512

Aging Offset (10h)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA

Por	0	0	0	0	0	0	0	0

Temperature Register (Upper Byte) (11h)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA
Por	0	0	0	0	0	0	0	0

Temperature Register (Lower Byte) (12h)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DATA	DATA	0	0	0	0	0	0
Por	0	0	0	0	0	0	0	0

SRAM (14h–FFh)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Por	X	X	X	X	X	X	X	X

Aging Offset Register

The aging offset register takes a user-provided value to add to or subtract from the oscillator capacitor array. The data is encoded in two’ s complement, with bit 7 representing the sign bit. One LSB represents the smallest capacitor to be switched in or out of the capacitance array at the crystal pins. The aging offset register capacitance value is added or subtracted from the capacitance value that the device calculates for each temperature compensation. The offset register is added to the capacitance array during a normal temperature conversion, if the temperature changes from the previous conversion, or during a manual user conversion (setting the CONV bit). To see the effects of the aging register on the 32kHz output frequency immediately, a manual conversion should be started after each aging offset register change.

Positive aging values add capacitance to the array, slowing the oscillator frequency. Negative values remove capacitance from the array, increasing the oscillator frequency. The change in ppm per LSB is different at different temperatures. The frequency vs. temperature curve is shifted by the values used in this register. At +25°C, one LSB typically provides about 0.1ppm change in frequency. Use of the aging register is not needed to achieve the accuracy as defined in the EC tables, but could be used to help compensate for aging at a given temperature. See the Typical Operating Characteristics section for a graph showing the effect of the register on accuracy over temperature.

Temperature Registers (11h–12h)

Temperature is represented as a 10-bit code with a resolution of 0.25°C and is accessible at location 11h and 12h. The temperature is encoded in two's complement format, with bit 7 in the MSB representing the sign bit. The upper 8 bits, the integer portion, are at location 11h and the lower 2 bits, the fractional portion, are in the upper nibble at location 12h. For example, 00011001 01b = +25.25°C. Upon power reset, the registers are set to a default temperature of 0°C and the controller starts a temperature conversion. The temperature is read on initial application of VCC or I 2C access on VBAT and once every 64 seconds afterwards. The temperature registers are updated after each user-initiated conversion and on every 64-second conversion. The temperature registers are read-only.

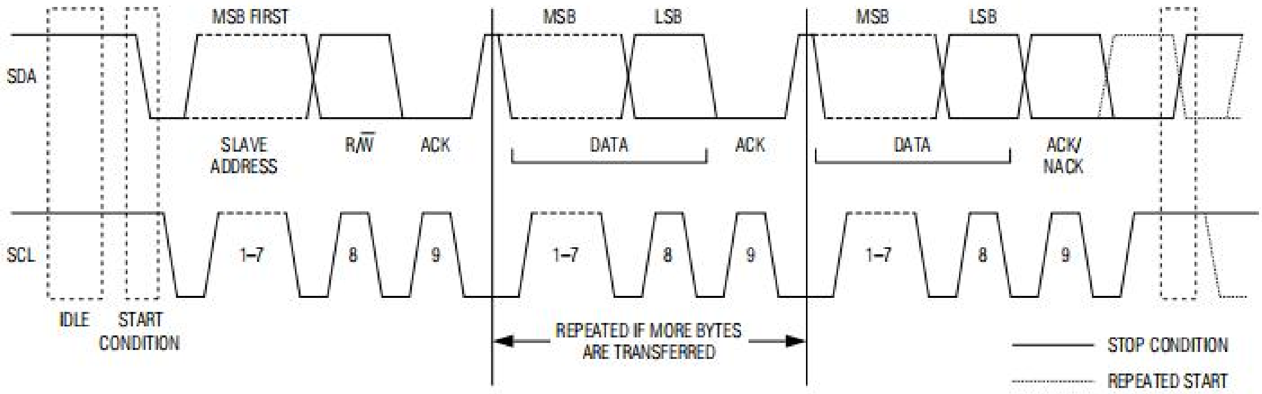

Figure 9. I2C Data Transfer Overview

Package Outline Dimensions

SOP-20

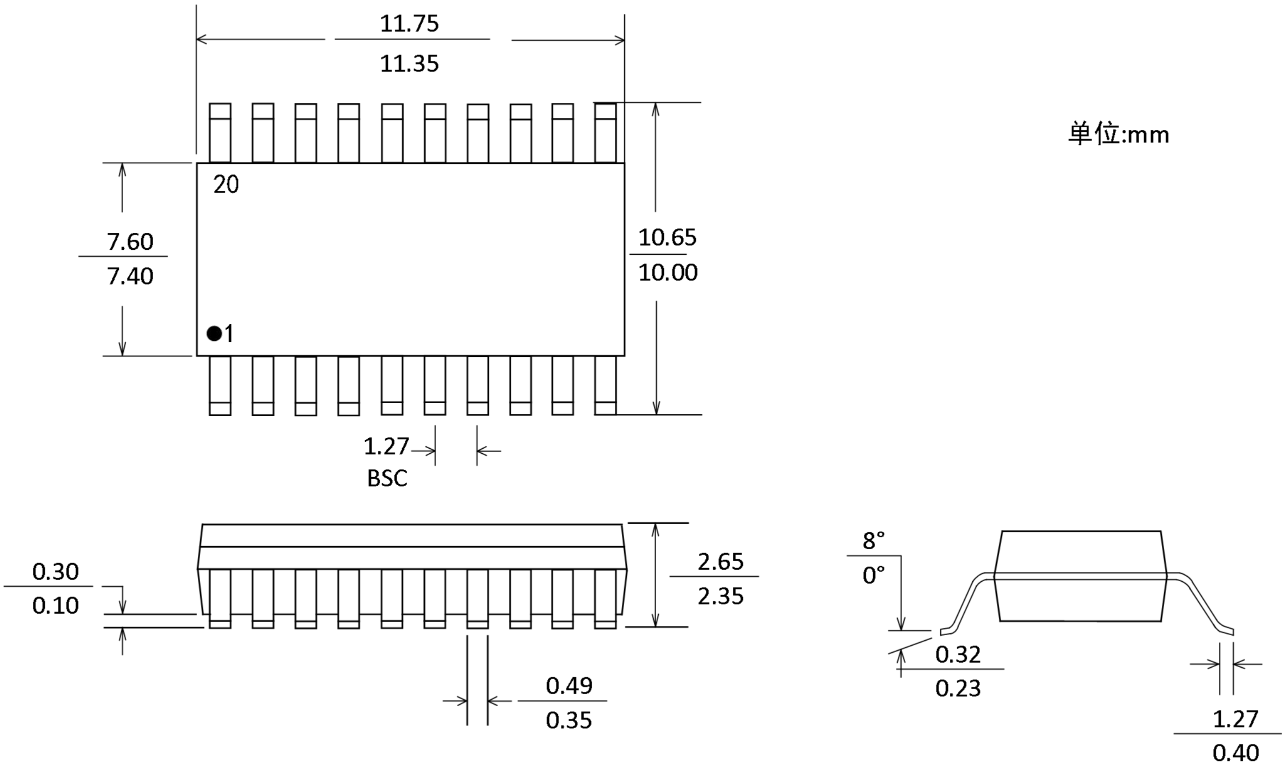

Figure 10 . 20-Lead Outline Package [SOP-20]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD32S32AS20	-40℃~85℃	SOP-20	Tape and Reel, 2500

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.25	Initial version	Regular update	WW	LYL	