CD32S34A

Extremely Accurate SPI Bus RTC with Integrated Crystal and SRAM

Version: Rev 1.0.0 Date: 2025-6-25

Features

- Highly Accurate RTC with Integrated Crystal and SRAM Completely Manages All Timekeeping Functions
- Accuracy ±2ppm from 0°C to +40°C
- Accuracy ±3.5ppm from -40°C to +85°C
- Real-Time Clock Counts Seconds, Minutes, Hours,Day, Date, Month, and Year, with Leap Year Compensation Valid Up to 2099
- Digital Temp Sensor Output: ±3°C Accuracy
- Register for Aging Trim
- RST Input/Output
- Two Time-of-Day Alarms
- Programmable Square-Wave Output
- Simple Serial Interface Connects to Most Microcontrollers
- 4MHz SPI Bus Supports Modes 1 and 3
- Battery-Backup Input for Continuous Timekeeping
- Low Power Operation Extends Battery Backup Run Time
- Operating Temperature Ranges Commercial: 0°C to+70°C, Industrial: -40°C to +85°C
- 300-Mil, 20-Pin SOP Package

Application

- Servers
- Telematics
- Utility Power Meters
- GPS

Description

The CD32S34A is a low-cost, extremely accurate SPI bus real-time clock (RTC) with an integrated temperature-compensated crystal oscillator (TCXO) and crystal. The CD32S34A incorporates a precision, temperature-compensated voltage reference and comparator circuit to monitor VCC. When VCC drops below the power-fail voltage (VPF),the device asserts the RST output and also disables read and write access to the part when VCC drops below both VPF and VBAT. The RST pin is monitored as a pushbutton input for generating a μP reset. The device switches to the backup supply input and maintains accurate timekeeping when main power to the device is interrupted. The integration of the crystal resonator enhances the long-term accuracy of the device as well as reduces the piece-part count in a manufacturing line. The CD32S34A is available in commercial and industrial temperature ranges, and is offered in an industry-standard 300-mil, 20-pin SO package.The CD32S34A also integrates 256 bytes of battery-backed SRAM. In the event of main power loss, the contents of the memory are maintained by the power source connected to the VBAT pin. The RTC maintains seconds,minutes, hours, day, date, month, and year information.The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. Two programmable time-of-day alarms and a programmable square-wave output are provided. Address and data are transferred serially by an SPI bidirectional bus.

The CD32S34A is a low-cost temperature-compensated crystal oscillator (TCXO) with a very accurate, temperature-compensated, integrated real-time clock (RTC) and 236 bytes of battery-backed SRAM. Additionally, the CD32S34A incorporates a battery input and maintains accurate timekeeping when main power to the device is interrupted. The integration of the crystal resonator enhances the long-term accuracy of the device as well as reduces the piece-part count in a manufacturing line. The CD32S34A is available in commercial and industrial temperature ranges, and is offered in an industry-standard 20-pin, 300-mil SO package. The RTC maintains seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Two programmable time-ofday alarms and a programmable square-wave output are provided. Address and data are transferred serially through an I2C bidirectional bus. A precision temperature-compensated voltage reference and comparator circuit monitors the status of VCC to detect power failures, to provide a reset output, and to automatically switch to the backup supply when necessary. Additionally, the RST pin is monitored as a pushbutton input for generating a μP reset.

Contents

Pin Configurations

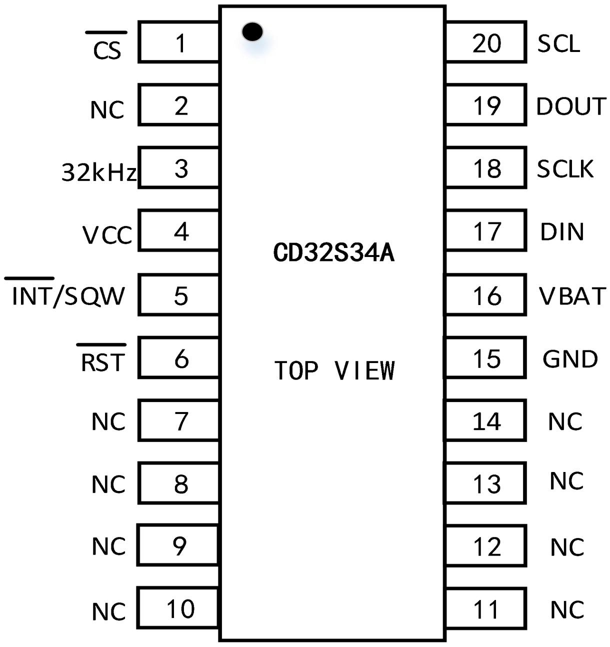

Figure 1. SOP20 Pin Configuration

Pin Description

Table 1. Pin description

Pin No.	Pin Name	Description
1	CS	Active-Low Chip Select Input. Used to select or deselect the device.
2,7-14	NC	No Connection. Not connected internally. Must be connected to ground.
3	32kHz	32kHz Push-Pull Output. If disabled with either EN32kHz = 0 or BB32kHz = 0, the state of the 32kHz pin will be low.
4	VCC	DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1µF to 1.0µF capacitor.
5	INT/SQW	Active-Low Interrupt or Square-Wave Output. This open-drain pin requires an external pullup resistor. It can be left open if not used. This multifunction pin is determined by the state of the INTCN bit in the Control Register (0Eh). When INTCN is set to logic 0, this pin outputs a square wave and its frequency is determined by RS2 and RS1 bits. When INTCN is set to logic 1, then a match between the timekeeping registers and either of the alarm registers activates the INT/SQW pin (if the alarm is

		enabled). Because the INTCN bit is set to logic 1 when power is first applied, the pin defaults to an interrupt output with alarms disabled. The pullup voltage can be up to 5.5V, regardless of the voltage on VCC. If not used, this pin can be left unconnected.
6	$\overline{\text{RST}}$	Active-Low Reset. This pin is an open-drain input/output. It indicates the status of VCC relative to the VPF specification. As VCC falls below VPF, the RST pin is driven low. When VCC exceeds VPF, for tRST, the RST pin is driven high impedance. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50k_ nominal value pullup resistor to VCC. No external pullup resistors should be connected. On first power-up, or if the crystal oscillator is disabled, tRST is bypassed and RST immediately goes high.
15	GND	Ground
16	VBAT	Backup Power-Supply Input. If VBAT is not used, connect to ground. Diodes placed in series between the VBAT pin and the battery can cause improper operation. UL recognized to ensure against reverse charging when used with a lithium battery.
17	DIN	SPI Data Input. Used to shift address and data into the device.
18,20	SCLK	SPI Clock Input. Used to control timing of data into and out of the device. Either clock polarity can be used. The clock polarity is determined by the device based on the state of SCLK when CS goes low. Pins 18 and 20 are electrically connected together internally.
19	DOUT	SPI Data Output. Data is output on this pin when the device is in read mode; CMOS push-pull driver.

Functional Block diagram

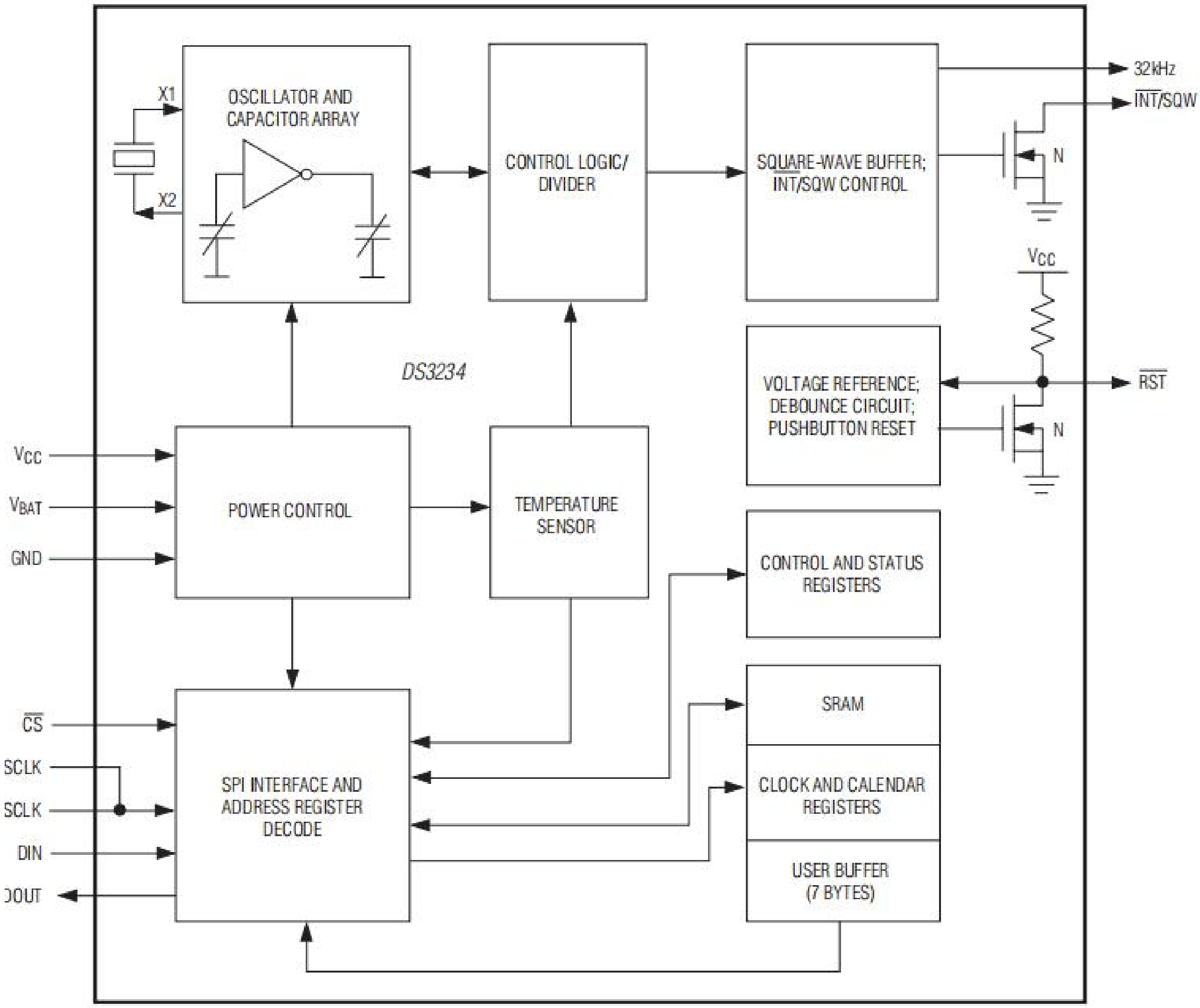

Figure 2. Functional Block Diagram

Typical Application Circuit

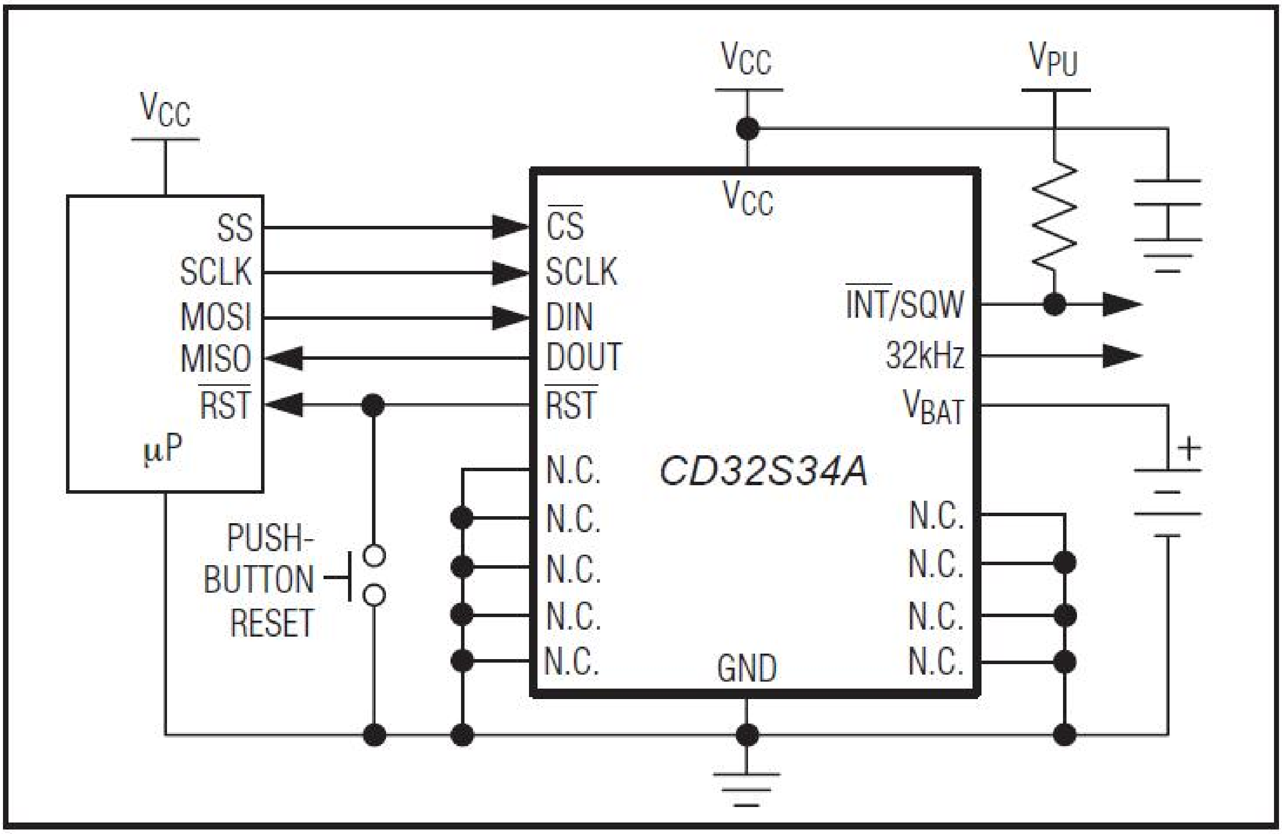

Figure 3. Typical Application Circuit Diagram

Absolute Maximum Ratings

Parameter	Range
Voltage Range on Any Pin Relative to GND	−0.3 V to +6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +85°C
Lead Temperature (soldering, 10s)	260°C
Soldering Temperature (reflow)	260°C
Junction Temperature	125°C
Junction-to-Ambient Thermal Resistance ((θJA)	55.1°C/W
Junction-to-Case Thermal Resistance ((θJC)	24°C/W

Operating Temperatures Range

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 2, 3)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	VCC		2.0	3.3	5.5	V
	VBAT		2.0	3.0	3.8	
Logic0 Input SDA, SCL	V_{IL}		-0.3		$+0.2V_{CC}$	V
Logic1 Input SDA, SCL	V_{IH}		$0.7V_{CC}$		$V_{CC}+0.3$	V

DC Electrical Characteristics

(VCC = 2.0V to 5.5V, VCC = active supply (see Table 1), TA = -40°C to +85°C, unless otherwise noted.) (Typical values are at VCC=3.3V, VBAT = 3.0V, and TA = +25°C, unless otherwise noted. TCXO operation guaranteed from 2.3V to 5.5V on VCC and 2.3V to 3.8V on VBAT.) (Notes 2, 3)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Active Supply Current	I_{CCA}	SCLK = 4MHz, BSY = 0 (Notes 4, 5)VCC = 3.63V	--	--	400	μA
		SCLK = 4MHz, BSY = 0 (Notes 4, 5)VCC = 5.5V	--	--	700	μA
Standby Supply Current	I_{CCS}	CS = VIH, 32kHz output off, SQW output off (Note 5)VCC = 3.63V	--	--	120	μA
		CS = VIH, 32kHz output off, SQW output off (Note 5)VCC = 5.5V	--	--	160	
Temperature Conversion Current	$I_{CCSCONV}$	SPI bus inactive, 32kHz output off, SQW output off,VCC = 3.63V	--	--	500	μA
		SPI bus inactive, 32kHz output off, SQW output off,VCC = 5.5V	--	--	600	μA
Power-Fail Voltage	V_{PF}		2.45	2.575	2.70	V
VBAT Leakage Current	IBATLKG		--	25	100	nA
(VCC = 2.0V to 5.5V, TA = -40°C to +85°C, unless otherwise noted.) (Notes 2 and 3)						
Logic 1 Output, 32kHz	V_{OH}	VCC > 3.63V, 3.63V > VCC > 2.7V, 2.7V > (VCC or VBAT) > 2.0V (BB32kHz = 1)	0.85*VCC	--	--	V
IOH = -500μA						
IOH = -250μA						
IOH = -125μA						

Logic 0 Output, 32kHz	V_{OL}	IOL = 1mA	--	--	0.4	V
Logic 1 Output, DOUT	V_{OH}	IOH = -1mA	0.85*VCC	--	--	V
Logic 0 Output, DOUT, INT/SQW	V_{OL}	IOL = 3mA	--	--	0.4	V
Logic 0 Output, RST	V_{OL}	IOL = 1mA	--	--	0.4	V
Output Leakage Current 32kHz, INT/SQW, DOUT	I_{LO}	Output high impedance	-1	0	+1	μA
TCXO (VCC = 2.3V to 5.5V, VBAT = 2.3V to 3.8V, TA = -40°C to +85°C, unless otherwise noted.) (Notes 2 and 3)						
Output Frequency	f_{OUT}	VCC = 3.3V or VBAT = 3.3V	--	32.768	--	kHz
Frequency Stability vs. Temperature	$\Delta f/f_{OUT}$	VCC = 3.3V or VBAT = 3.3V	-3.5	--	3.5	ppm
Frequency Stability vs. Voltage	Δf/V		--	1	--	ppm/V
Trim Register Frequency Sensitivity per LSB	Δf/LSB		--	0.1	--	ppm
Temperature Accuracy	Temp		-3	--	+3	℃
Crystal Aging	Δf/fO	After reflow, not production tested，First year	--	±1.0	--	ppm
		After reflow, not production tested，0–10 years	--	±5.0	--	ppm
Output Frequency	f_{OUT}	VCC = 3.3V or VBAT = 3.3V	--	32.768	--	kHz

(VCC = 0V, VBAT = 2.0V to 3.8V, TA = -40°C to +85°C, unless otherwise noted.) (Note 2)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
			VBAT = 5.5V	--	--	200	
Timekeeping Battery Current	IBATT	EOSC = 0, BBSQW = 0, CRATE1 = CRATE0 = 0	VBAT = 3.4V	--	1.5	2.3	μA
			VBAT = 3.8V	--	15	2.5	
Temperature Conversion Current	IBATTC	$\overline{EOSC}$ = 0, BBSQW = 0		--	--	400	μA

Data-Retention Current	IBATTDR	$\overline{EOSC}$ = 1	--	--	100	nA

AC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$or V_{BAT} = $V_{BAT(MIN)}$ to $V_{BAT(MAX)}$, V_{BAT} > V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL Clock Frequency	f_{SCL}	2.7V ≤ VCC ≤ 5.5V	--	--	4	MHz
		2.0V ≤ VCC < 2.7V	--	--	2	
Data to SCLK Setup	t_{DC}		30	--	--	ns
SCLK to Data Hold	t_{CDH}		30	--	--	ns
SCLK to CS Setup	t_{CCS}		30	--	--	ns
SCLK to Data Valid (Note 7)	t_{CDD}	2.7V ≤ VCC ≤ 5.5V	--	--	80	ns
		2.0V ≤ VCC < 2.7V	--	--	160	ns
SCLK Low Time	t_{CL}	2.7V ≤ VCC ≤ 5.5V	110	--	--	ns
		2.0V ≤ VCC < 2.7V	220	--	--	
SCLK High Time	t_{CH}	2.7V ≤ VCC ≤ 5.5V	110	--	--	ns
		2.0V ≤ VCC < 2.7V	220	--	--	
SCLK Rise and Fall	t_R, t_F		--	--	200	ns
CS to SCLK Setup	t_{CC}		400	--	--	ns
SCLK to CS Hold	t_{CCH}	2.7V ≤ VCC ≤ 5.5V	100	--	--	ns
		2.0V ≤ VCC < 2.7V	200	--	--	
CS Inactive Time	t_{CWH}		400	--	--	ns
CS to Output High Impedance	t_{CDZ}	(Note 8)	--	--	40	ns
Pushbutton Debounce	PBDB		--	250	--	ms
Reset Active Time	t_{RST}		--	250	--	ms
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 9)	--	100	--	ms
Temperature Conversion Time	t_{CONV}		--	125	200	ms

Power-Up/Power-Down Characteristics

(T_A = T_{MIN} to T_{MAX})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Recovery at Power-Up	t_{REC}	--	125	300	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_{VCCF}	300	--	--	µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_{VCCR}	0	--	--	µs

WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations

Note 2: Limits at -40°C are guaranteed by design and not production tested.

Note 3: All voltages are referenced to ground.

Note 4: Measured at VIH = 0.8 x VCC or VIL = 0.2 x VCC, 10ns rise/fall time, DOUT = no load.

Note 5: Current is the averaged input current, which includes the temperature conversion current. CRATE1 = CRATE0 = 0.

Note 6: The RST pin has an internal 50kΩ (nominal) pullup resistor to VCC.

Note 7: Measured at VOH = 0.8 x VCC or VOL = 0.2 x VCC. Measured from the 50% point of SCLK to the VOH minimum of DOUT.

Note 8: With 50pF load.

Note 9: The parameter tOSF is the period of time the oscillator must be stopped for the OSF flag to be set over the voltage range of 0V ≤ VCC ≤ VCC(MAX) and 2.3V ≤ VBAT ≤ VBAT(MAX).

Note 10: This delay only applies if the oscillator is enabled and running. If the EOSC bit is 1, tREC is bypassed and RST immediately goes high.

Note 11: Guaranteed by design and not production tested.

Timing

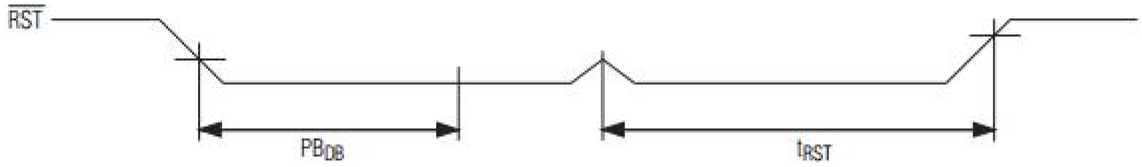

Figure 4. Pushbutton Reset Timing

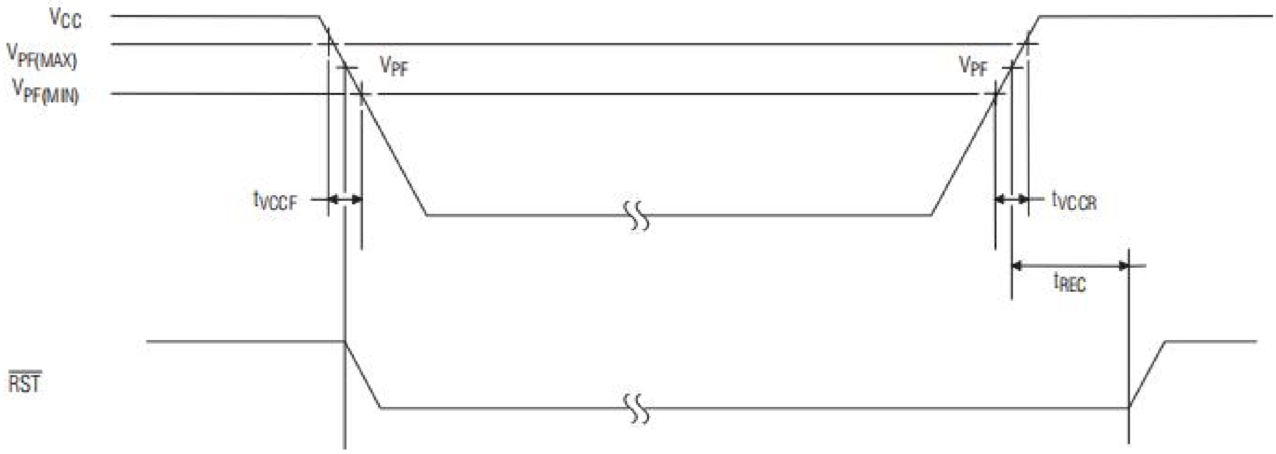

Figure 5. Power-Switch Timing

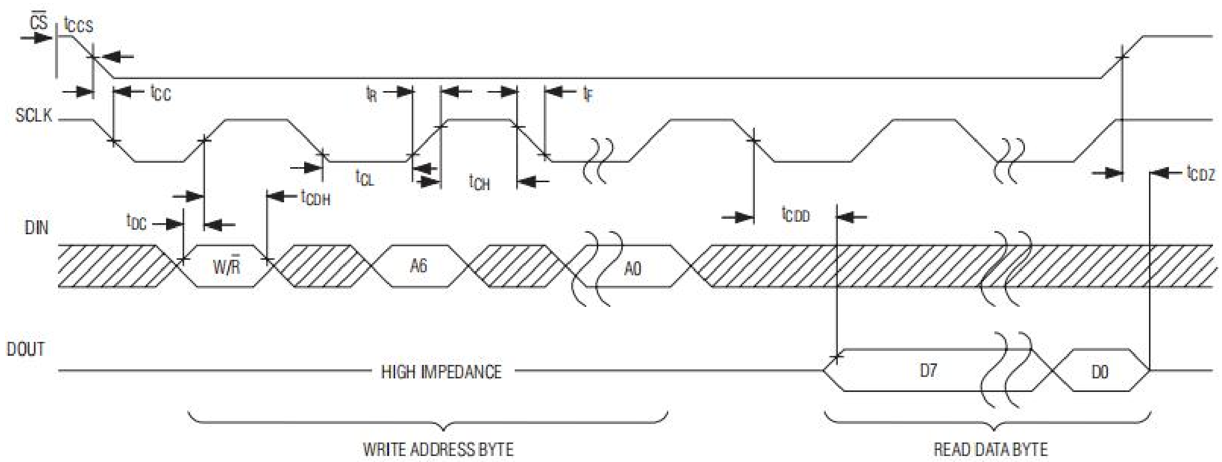

Figure 6. Timing Diagram—SPI Read Transfer

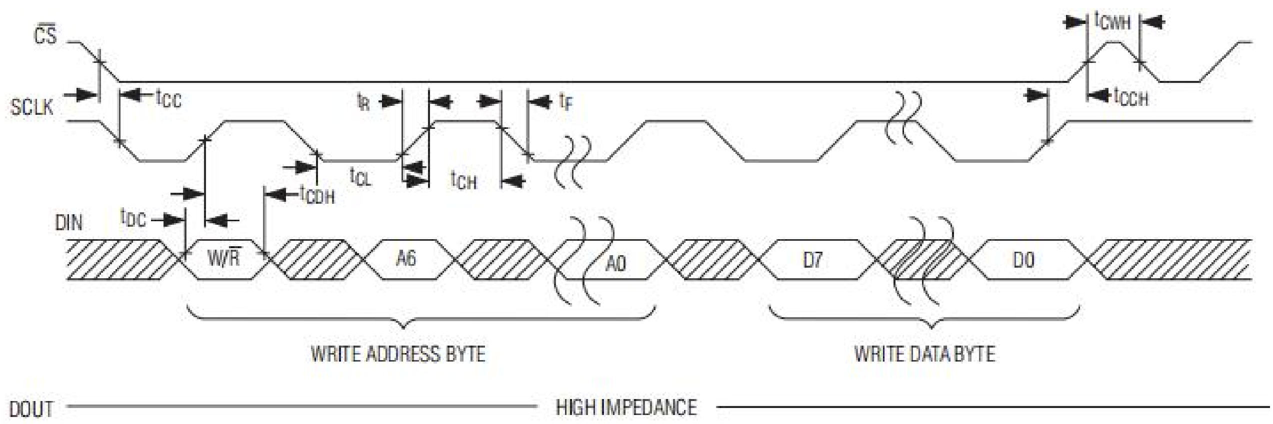

Figure 7. Timing Diagram—SPI Write Transfer

Typical Electrical Characteristics

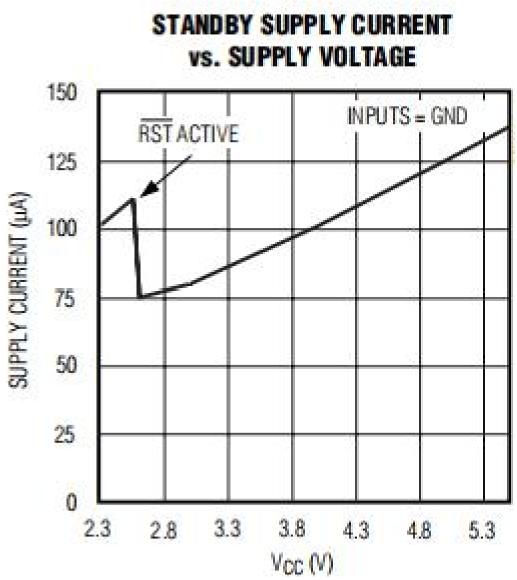

Figure 8. STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE

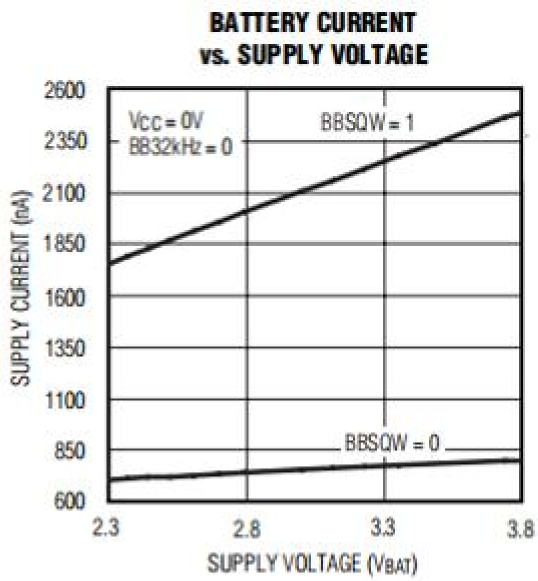

Figure 9. SUPPLY CURRENT vs. SUPPLY VOLTAGE

DETAILED DESCRIPTION

The CD32S34A is a TCXO and RTC with integrated crystal and 256 bytes of SRAM. An integrated sensor periodically samples the temperature and adjusts the oscillator load to compensate for crystal drift caused by temperature variations. The CD32S34A provides userselectable sample rates. This allows the user to select a temperature sensor sample rate that allows for various temperature rates of change, while minimizing current consumption by temperature sensor sampling. The user should select a sample rate based upon the expected temperature rate of change, with faster sample rates for applications where the ambient temperature changes significantly over a short time. The TCXO provides a stable and accurate reference clock, and maintains the RTC to within ±2 minutes per year accuracy from -40°C to +85°C. The TCXO

frequency output is available at the 32kHz pin. The RTC is a low-power clock/calendar with two programmable time-of-day alarms and a programmable square-wave output. The INT/SQW provides either an interrupt signal due to alarm conditions or a square-wave output. The clock/calendar provides seconds, minutes, hours, day,date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. Access to the internal registers is possible through an SPI bus interface.
A temperature-compensated voltage reference and comparator circuit monitors the level of VCC to detect power failures and to automatically switch to the backup supply when necessary. When operating from the backup supply, access is inhibited to minimize supply current. Oscillator, time and date, and TCXO operations can continue while the backup supply powers the device. The RST pin provides an external pushbutton function and acts as an indicator of a power-fail event.

Operation

The block diagram shows the main elements of the CD32S34A. The eight blocks can be grouped into four functional groups: TCXO, power control, pushbutton function, and RTC. Their operations are described separately in the following sections.

32kHz TCXO

The temperature sensor, oscillator, and control logic form the TCXO. The controller reads the output of the on-chip temperature sensor and uses a lookup table to determine the capacitance required, adds the aging correction in the AGE register, and then sets the capacitance selection registers. New values, including changes to the AGE register, are loaded only when a change in the temperature value occurs. The temperature is read on initial application of VCC and once every 64 seconds (default, see the description for CRATE1 and CRATE0 in the Control/Status Register section) afterwards.

Power Control

The power control function is provided by a temperature-compensated voltage reference and a comparator circuit that monitors the VCC level. The device is fully accessible and data can be written and read when VCC is greater than VPF. However, when VCC falls below both VPF and VBAT, the internal clock registers are blocked from any access. If VPF is less than VBAT, the device power is switched from VCC to VBAT when VCC drops below VPF. If VPF is greater than VBAT, the device power is switched from VCC to VBAT when VCC drops below VBAT. After VCC returns above both VPF and VBAT, read and write access is allowed after RST goes high (Table 1). To preserve the battery, the first time VBAT is applied to the device, the oscillator does not start up until VCC

Table 1. Power Control

Supply Condition	READ/WRITE ACCESS	ACTIVE SUPPLY	RST
$V_{CC} < V_{PF}$, $V_{CC} < V_{BAT}$	No	VBAT	Active
$V_{CC} < V_{PF}$, $V_{CC} > V_{BAT}$	Yes	VCC	Active
$V_{CC} > V_{PF}$, $V_{CC} < V_{BAT}$	Yes	VCC	Inactive
$V_{CC} > V_{PF}$, $V_{CC} > V_{BAT}$	Yes	VCC	Inactive

crosses VPF. After the first time VCC is ramped up, the oscillator starts up and the VBAT source powers the oscillator during power-down and keeps the oscillator running. When the CD32S34A switches to VBAT, the oscillator may be disabled by setting the EOSC bit.

VBAT Operation

There are several modes of operation that affect the amount of VBAT current that is drawn. When the part is powered by VBAT, timekeeping current (IBATT), which includes the averaged temperature conversion current, IBATTC, is drawn (refer to Application Note 3644: Power Considerations for Accurate Real-Time Clocks for details). Temperature conversion current, IBATTC, is specified since the system must be able to support the periodic higher current pulse and still maintain a valid
voltage level. Data retention current, IBATTDR, is the current drawn by the part when the oscillator is stopped (EOSC = 1). This mode can be used to minimize battery requirements for times when maintaining time and date information is not necessary, e.g., while the end system is waiting to be shipped to a customer.

Pushbutton Reset Function

The CD32S34A provides for a pushbutton switch to be connected to the RST output pin. When the CD32S34A is not in a reset cycle, it continuously monitors the RST signal for a low going edge. If an edge transition is detected, the CD32S34A debounces the switch by pulling the RST low. After the internal timer has expired (PBDB), the CD32S34A continues to monitor the RST line. If the line is still low, the CD32S34A continuously monitors the line looking for a rising edge. Upon detecting release, the CD32S34A forces the RST pin low and holds it low for tRST. The same pin, RST, is used to indicate a power-fail condition. When VCC is lower than VPF, an internal power-fail signal is generated, which forces the RST pin low. When VCC returns to a level above VPF, the RST pin is held low for tREC to allow the power supply to stabilize. If the EOSC bit is set to logic 1 (to disable the oscillator in battery-backup mode), tREC is bypassed and RST immediately goes high.When RST is active due to a power-fail condition (see Table 1), SPI operations are inhibited while the TCXO and RTC continue to operate. When RST is active due to a pushbutton event, it does not affect the operation of the TCXO, SPI interface, or RTC functions.

Real-Time Clock

With the clock source from the TCXO, the RTC provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. The clock provides two programmable time-of-day alarms and a programmable square-wave output. The INT/SQW pin either generates an interrupt due to alarm condition or outputs a square-wave signal and the selection is controlled by the bit INTCN.

SRAM

The CD32S34A provides 256 bytes of general-purpose battery-backed read/write memory. The SRAM can be written or read whenever VCC is above either VPF or VBAT.

Address Map

The address map for the CD32S34A timekeeping registers. During a multibyte access, when the address pointer reaches the end of the register space (13h read, 93h write), it wraps around to the beginning (00h read, 80h write). The CD32S34A does not respond to a read or write to any reserved address, and the internal address pointer does not increment. Address pointer operation when accessing the 256-byte SRAM data is covered in the description of the SRAM address and data registers. On the falling edge of CS, or during a multibyte access when the address pointer increments to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the internal clock registers continue to increment normally. If the time and date registers are read using a multibyte read, this eliminates the need to reread the registers in case the main registers update during a read.

SPI Interface

The CD32S34A operates as a slave device on the SPI serial bus. Access is obtained by selecting the part by the CS pin and clocking data into/out of the part using the SCLK and DIN/DOUT pins. Multiple byte transfers are supported within one CS low period. The SPI on the CD32S34A interface is accessible whenever VCC is above either VBAT or VPF.

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Below Figure illustrates the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in binary-coded decimal (BCD) format. The CD32S34A can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, 12-hour mode is selected. In 12- hour mode, bit 5 is the AM/PM bit with logic-high being PM. In 24-hour mode, bit 5 is the 20-hour bit (20–23 hours). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00.
The day-of-week register increments at midnight. Values that correspond to the day of week are userdefined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on the falling edge of CS or and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read. The countdown chain is reset whenever the seconds register is written. Write transfers occur when the last bit of a byte is clocked in. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1 second. The 1Hz square-wave output, if enabled, transitions high 500ms after the seconds data transfer.

Address Map for CD32S34A Timekeeping Registers and SRAM

ADDRESS READ/WRITE		MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0	FUNCTION	RANGE
00h	80h	0	10 Seconds			Seconds				Seconds	00–59
01h	81h	0	10 Minutes			Minutes				Minutes	00–59
02h	82h	0	12/$\overline{24}$	$\overline{AM}$/PM 20 hr	10 hr	Hour				Hours	1-12 +$\overline{AM}$/PM 00-23
03h	83h	0	0	0	0	0	Day			Day	1-7
04h	84h	0	0	10 Date		Date				Date	01-31
05h	85h	Century	0	0	10 Mo	Month				Month/ Century	01-12 + Century
06h	86h	10 Year				Year				Year	00-99
07h	87h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00-59
08h	88h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00-59
09h	89h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 20 hr	10 hr	Hour				Alarm 1 Hours	1-12 +$\overline{AM}$/PM 00-23
0Ah	8Ah	A1M4	DY/$\overline{DT}$	0 10 Date		Day Date				Alarm 1 Day Alarm 1 Date	1-7 01-31
0Bh	8Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00-59
0Ch	8Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 20 hr	10 hr	Hour				Alarm 2 Hours	1-12 +$\overline{AM}$/PM 00-23
0Dh	8Dh	A2M4	DY/$\overline{DT}$	0 10 Date		Day Date				Alarm 2 Day Alarm 2 Date	1-7 01-31
0Eh	8Eh	$\overline{EOSC}$	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE	Control	—
0Fh	8Fh	OSF	BB32kHz	CRATE1	CRATE0	EN32kHz	BSY	A2F	A1F	Control/ Status	—
10h	90h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Crystal Aging Offset	—
11h	91h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Temp MSB	Read Only
12h	92h	DATA	DATA	0	0	0	0	0	0	Temp LSB	Read Only
13h	93h	0	0	0	0	0	0	0	BB_TD	Disable Temp Conversions	—
14h–17h	94h–97h	—	—	—	—	—	—	—	—	Reserved	—
18h	98h	A7	A6	A5	A4	A3	A2	A1	A0	SRAM Address	—
19h	99h	D7	D6	D5	D4	D3	D2	D1	D0	SRAM Data	—

Alarms

The CD32S34A contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h to 0Ah. Alarm 2 can be set by writing to registers 0Bh to 0Dh. The alarms can be programmed (by the alarm enable and INTCN bits of the control register) to activate the INT/SQW output on an alarm match condition. Bit 7 of each of the time-ofday/date alarm registers are mask bits (Table 2). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-ofday/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 2 shows the possible settings. Configurations not listed in the table will result in illogical operations. The DY/DT bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/DT is written to logic 0, the alarm will be the result of a match with date of the month. If DY/DT is written to logic 1, the alarm will be the result of a match with day of the week.

When the RTC register values match alarm register settings, the corresponding Alarm Flag 'A1F' or 'A2F' bit is set to logic 1. If the corresponding Alarm Interrupt Enable 'A1IE' or 'A2IE' is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the INT/SQW signal. The match is tested on the onceper-second update of the time and date registers.

Table 2. Alarm Mask Bits

DY/DT	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once per second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/DT	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A1M4	A1M3	A1M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

Control Register (0Eh/8Eh)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EOSC	BBSQW	CONV	RS2	RS1	INTCN	A2IE	A1IE
Por	0	0	0	1	1	1	0	0

*POR is defined as the first application of power to the device, either VBAT or VCC.

Special-Purpose Registers

The CD32S34A has two additional registers (control and control/status) that control the real-time clock, alarms, and square-wave output.

Control Register (0Eh/8Eh)

Bit 7: Enable Oscillator (EOSC).

When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped when the CD32S34A switches to battery power. This bit is clear (logic 0) when power is first applied. When the CD32S34A is powered by VCC, the oscillator is always on regardless of the status of the EOSC bit. When EOSC is disabled, all register data is static.

Bit 6: Battery-Backed Square-Wave Enable (BBSQW).

When set to logic 1 with INTCN = 0 and VCC < VPF, this bit enables the square wave. When BBSQW is logic 0, the INT/SQW pin goes high impedance when VCC < VPF. This bit is disabled (logic 0) when power is first applied.

Bit 5: Convert Temperature (CONV).

Setting this bit to 1 forces the temperature sensor to convert the temperature into digital code and execute the TCXO algorithm to update the capacitance array to the oscillator. This can only happen when a conversion is not already in progress. The user should check the status bit BSY before forcing the controller to start a new TCXO execution. A user-initiated temperature conversion does not affect the internal 64-second (default interval) update cycle. This bit is disabled (logic 0) when power is first applied. A user-initiated temperature conversion does not affect the BSY bit for approximately 2ms. The CONV bit remains at a 1 from the time it is written until the conversion is finished, at which time both CONV and BSY go to 0. The CONV bit should be used when monitoring the status of a user-initiated conversion.

Bits 4 and 3: Rate Select (RS2 and RS1).

These bits control the frequency of the square-wave output when the square wave has been enabled. The following table shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (8.192kHz) when power is first applied.

SQUARE-WAVE OUTPUT FREQUENCY

RS2	RS1	SQUARE-WAVE OUTPUT FREQUENCY
0	0	1Hz
0	1	1.024kHz
1	0	4.096kHz
1	1	8.192kHz

Bit 2: Interrupt Control (INTCN).

This bit controls the INT/SQW signal. When the INTCN bit is set to logic 0, a square wave is output on the INT/SQW pin. When the INTCN bit is set to logic 1, a match between the timekeeping registers and either of the alarm registers activates the INT/SQW (if the alarm is also enabled). The corresponding alarm flag is always set regardless of the state of the INTCN bit. The INTCN bit is set to logic 1 when power is first applied.

Bit 1: Alarm 2 Interrupt Enable (A2IE).

When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert INT/SQW (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.

Bit 0: Alarm 1 Interrupt Enable (A1IE).

When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert INT/SQW (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate the INT/SQW signal. The A1IE bit is disabled (logic 0) when power is first applied.

Control/Status Register (0Fh/8Fh)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OSF	BB32kHz	CRATE1	CRATE0	EN32kHz	BSY	A2F	A1F
Por	1	1	0	0	1	0	0	0

Control/Status Register (0Fh/8Fh)

Bit 7: Oscillator Stop Flag (OSF).

A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and may be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltages present on both VCC and VBAT are

insufficient to support oscillation.
3) The EOSC bit is turned off in battery-backed mode.
4) External influences on the crystal (i.e., noise, leakage, etc.).
This bit remains at logic 1 until written to logic 0.

Bit 6: Battery-Backed 32kHz Output (BB32kHz).

This bit enables the 32kHz output when powered from VBAT (provided EN32kHz is enabled). If BB32kHz = 0, the 32kHz output is low when the part is powered by VBAT. This bit is enabled (logic 1) when power is first applied.

Bits 5 and 4: Conversion Rate (CRATE1 and

CRATE0).

These two bits control the sample rate of the TCXO. The sample rate determines how often the temperature sensor makes a conversion and applies compensation to the oscillator. Decreasing the sample rate decreases the overall power consumption by decreasing the frequency at which the temperature sensor operates. However, significant temperature changes that occur between samples may not be completely compensated for, which reduce overall accuracy. These bits are set to logic 0 when power is first applied.

Bit 3: Enable 32kHz Output (EN32kHz).

This bit indicates the status of the 32kHz pin. When set to logic 1, the 32kHz pin is enabled and outputs a 32.768kHz square-wave signal. When set to logic 0, the 32kHz pin is low. The initial power-up state of this bit is logic 1, and a 32.768kHz square-wave signal appears at the 32kHz pin after a power source is applied to the CD32S34A. This bit is enabled (logic 1) when power is first applied.

Bit 2: Busy (BSY).

This bit indicates the device is busy executing TCXO functions. It goes to logic 1 when the conversion signal to the temperature sensor is asserted and then is cleared when the conversion is complete.

Bit 1: Alarm 2 Flag (A2F).

A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit and INTCN bit are set to logic 1, the INT/SQW pin is driven low while A2F is active. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Bit 0: Alarm 1 Flag (A1F).

A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit and the INTCN bit are set to logic 1, the INT/SQW pin is driven low while A1F is active. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Carte1	Carte0	SAMPLE RATE (seconds)
0	0	64
0	1	128
1	0	256
1	1	512

Aging Offset (10h/90h)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA
Por	0	0	0	0	0	0	0	0

Temperature Register (MSB) (11h)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA
Por	0	0	0	0	0	0	0	0

Temperature Register (LSB) (12h)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	DATA	DATA	0	0	0	0	0	0
Por	0	0	0	0	0	0	0	0

Aging Offset Register (10h/90h)

The aging offset register takes a user-provided value to add to or subtract from the oscillator capacitor array. The data is encoded in two’ s complement, with bit 7 representing the SIGN bit. One LSB represents the smallest capacitor to be switched in or out of the capacitance array at the crystal pins. The aging offset register capacitance value is added or subtracted from the capacitance value that the device calculates for each temperature compensation. The offset register is added to the capacitance array during a normal temperature conversion, if the temperature changes from the previous conversion, or during a manual user conversion (setting the CONV bit). To see the effects of the aging register on the 32kHz output frequency immediately, a manual conversion should be performed after each aging offset register change. Positive aging values add capacitance to the array, slowing the oscillator frequency. Negative values remove capacitance from the array, increasing the oscillator frequency. The change in ppm per LSB is different at different temperatures. The frequency vs. temperature curve is shifted by the values used in this register. At +25°C, one LSB typically provides about 0.1ppm change in frequency. These bits are all set to logic 0 when power is first applied. Use of the aging register is not needed to achieve the accuracy as defined in the EC tables, but could be used to help compensate for aging at a given temperature. See the Typical Operating Characteristics section for a graph showing the effect of the register on accuracy over temperature.

Temperature Registers (11h–12h)

Temperature is represented as a 10-bit code with a resolution of 0.25°C and is accessible at location 11h and 12h. The temperature is encoded in two' s complement format, with bit 7 in the MSB representing the SIGN bit. The upper 8 bits, the integer portion, are at location 11h and the lower 2 bits, the fractional portion, are in the upper nibble at location 12h. Example: 00011001 01b = +25.25°C. Upon power reset, the registers are set to a default temperature of 0°C and the controller starts a temperature conversion. The temperature is read on initial application of VCC and once every 64 seconds afterwards. The temperature registers are updated after each user-initiated conversion and on every 64-second conversion. The temperature registers are read-only

Temperature Control (13h/93h)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	0	0	0	0	0	0	0	BB_TD
Por	0	0	0	0	0	0	0	0

SRAM Address (18h/98h)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	A7	A6	A5	A4	A3	A2	A0	

SRAM Data (19h/99h)

—	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	D7	D6	D5	D4	D3	D2	D1	D0

Temperature Control Register (13h/93h)

Bit 0: Battery-Backed Temperature Conversion

Disable (BB_TD).

The battery-backed tempconv disable bit prevents automatic temperature conversions when the device is powered by the VBAT supply. This reduces the battery current at the expense of frequency accuracy.

SRAM Address Register (18h/98h)

The SRAM address register provides the 8-bit address of the 256-byte memory array. The desired memory address should be written to this register before the data register is accessed. The contents of this register are incremented automatically if the data register is accessed more than once during a single transfer. When the contents of the address register reach 0FFh, the next access causes the register to roll over to 00h.

SRAM Data Register (19h/99h)

The SRAM data register provides the data to be written to or the data read from the 256-byte memory array. During a read cycle, the data in this register is that found in the memory location in the SRAM address register (18h/98h). During a write cycle, the data in this register is placed in the memory location in the SRAM address register (18h/98h). When the SRAM data register is read or written, the internal register pointer remains at 19h/99h and the SRAM address register increments after each byte that is read or written, allowing multibyte transfers.

SPI Serial Data Bus

The CD32S34A provides a 4-wire SPI serial data bus to communicate in systems with an SPI host controller. The CD32S34A supports both single byte and multiple byte data transfers for maximum flexibility. The DIN and DOUT pins are the serial data input and output pins, respectively. The CS input is used to initiate and terminate a data transfer. The SCLK pin is used to synchronize data movement between the master (microcontroller) and the slave devices (see Table 3). The shift clock (SCLK), which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. Input data (DIN) is latched on the internal strobe edge and output data (DOUT) is shifted out on the shift edge (Figure 2). There is one clock for each bit transferred. Address and data bits are transferred in groups of eight.Address and data bytes are shifted MSB first into the serial data input (DIN) and out of the serial data output (DOUT). Any transfer requires the address of the byte to specify a write or read, followed by one or more bytes of data. Data is transferred out of the DOUT pin for a read operation and into the DIN for a write operation (Figures 3 and 4). The address byte is always the first byte entered after CS is driven low. The most significant bit of this byte determines if a read or write takes place. If the MSB is 0, one or more read cycles occur. If the MSB is 1, one or more write cycles occur.

Package Outline Dimensions

SOP-20

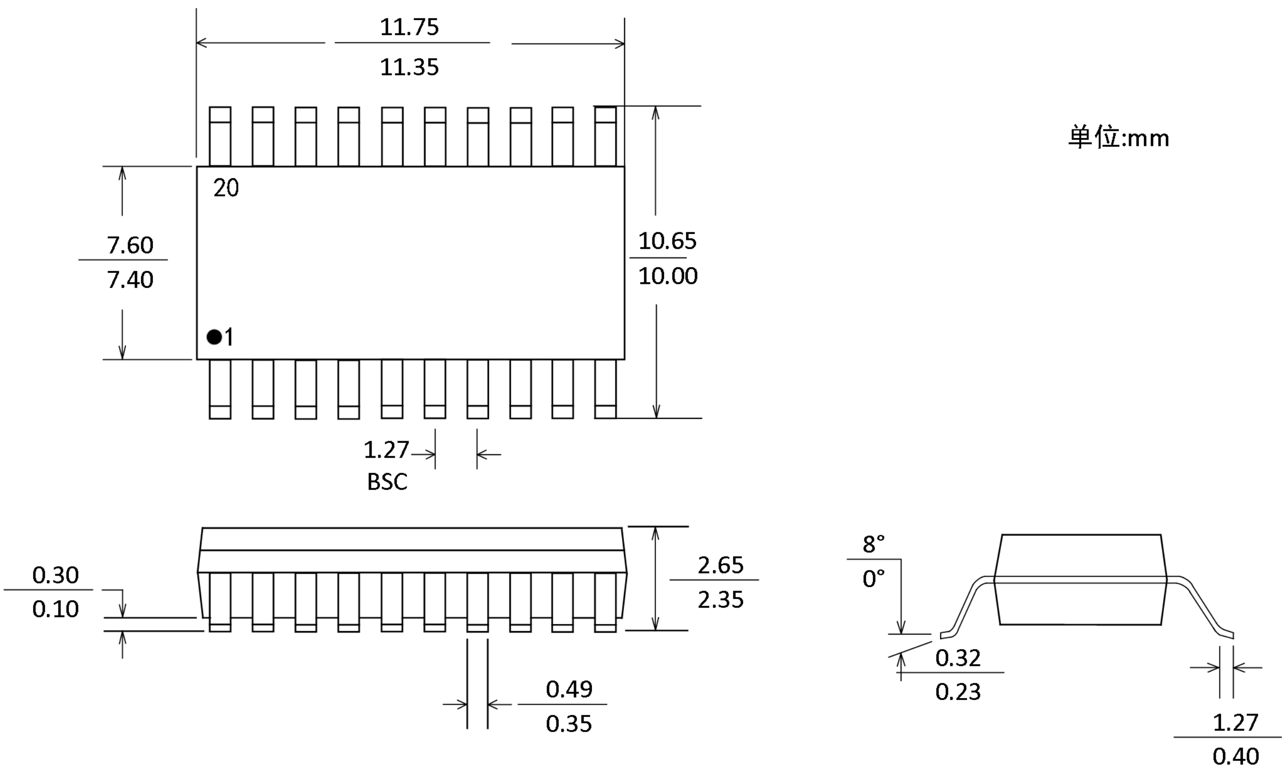

Figure 10 . 20-Lead Outline Package [SOP-20]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD32S34AS20	-40℃~85℃	SOP-20	Tape and Reel, 2500

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.25	Initial version	Regular update	WW	LYL	