CoreadDvices
承芯微电子

CD431

Programmable Precision Shunt Regulator

Version: Rev 1.0.0 Date: 2025-6-12

Features

- Programmable Output Voltage to 40V
- Low Dynamic Output Impedance 0.2Ω
- Sink Current Capability of 0.1 mA to 100 mA
- Equivalent Full-Range Temperature
- Temperature Compensated for Operation
- Low Output Noise Voltage
- Fast Turn on Response
- SOT23-3,SOT89-3 packages

Application

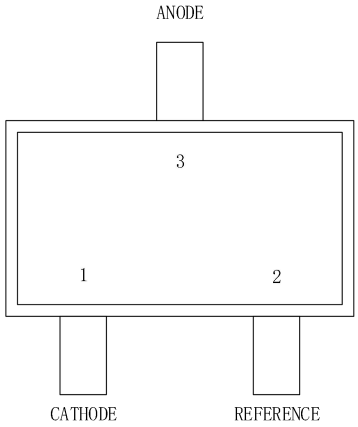
- Rack server power supply
- Industrial AC/DC power supply
- AC inverter and variable-frequency
- Servo drive control module
- Notebook computer power adapter

Description

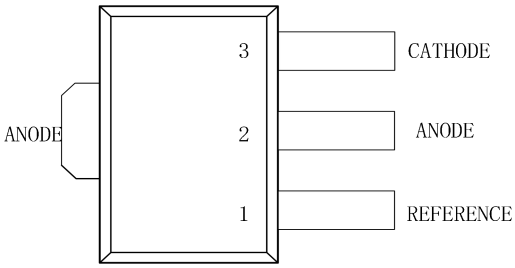
The CD431 is a three-terminal adjustable regulator series with a guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between Vref (approximately 2.5 volts) and 40 volts with two external resistors. These devices have a typical dynamic output impedance of 0.2Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacement for zener diodes in many applications.The CD431 is characterized for operation from -40℃ to +125℃.

Contents

Pin Configurations



SOT23-3



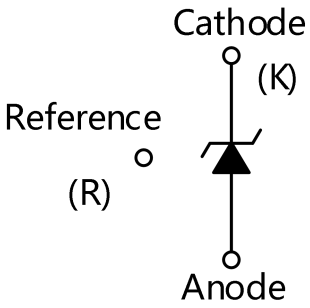
SOT89-3

Pin Description

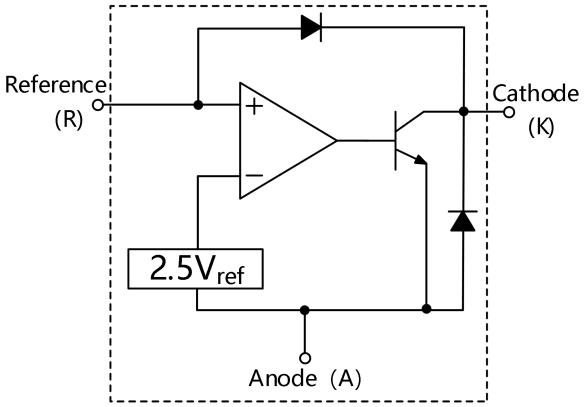
Name	SYMBOL (SOT23-3)	SYMBOL (SOT89-3)	TYPE (I/O)	NAME AND FUNCTION
REFERENCE	2	1	I	Threshold relative to common anode
ANODE	3	2	O	Common pin, normally connected to ground
CATHODE	1	3	I/O	Shunt Current/Voltage input

Chinese version:CD431

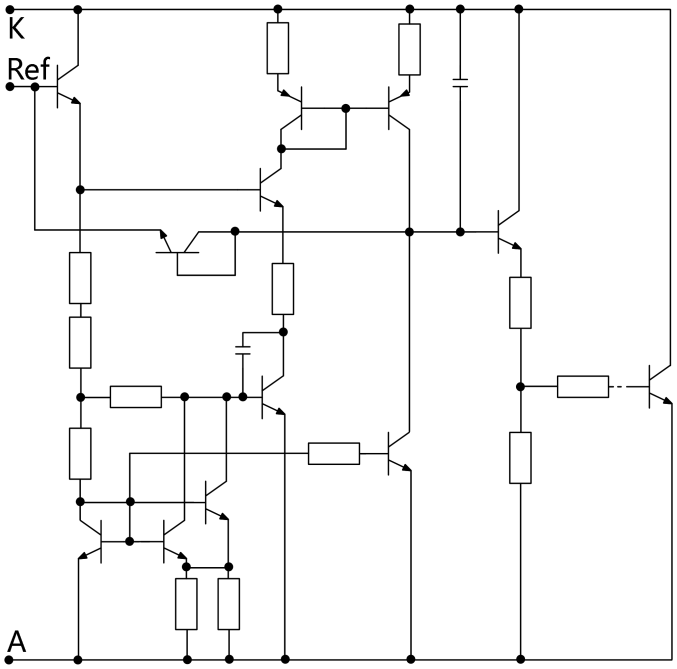
Symbol



Functional Block Diagram



Equivalent Schematic



Chinese version:CD431

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Cathode to Anode Voltage	VKA	VREF	0.01	40	V
Cathode Current	I_K	0.5	0.5	100	mA

Thermal information

Symbol	THERMAL METRIC	DBZ (CD432AST23/CD432AST89)	单位
$R_{\theta JA}$	Junction-to-ambient thermal resistance	371.7	C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	145.9	C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	104.7	C/W
ψJT	Junction-to-top characterization parameter	23.9	C/W
ψJB	Junction-to-board characterization parameter	102.9	C/W

Electrical Characteristics

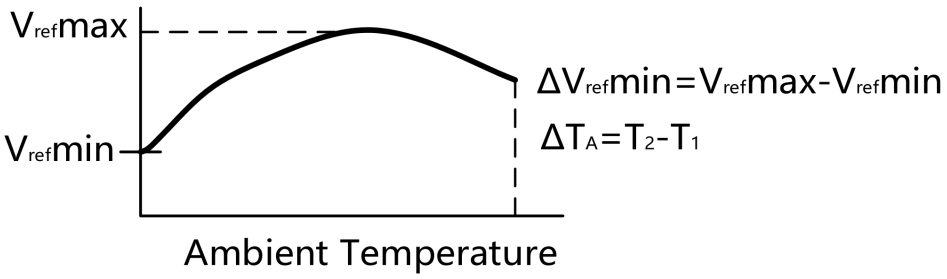
(T_A= 25℃, V_{KA} = VREF, I_K = 10mA unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Input Voltage	VREF	V_{KA} = VREF, I_K = 10mA				
		CD431 (2%) CD431-A (1%) CD431-C (0.5%)	2.440 2.470 2.482	2.495 2.495 2.495	2.550 2.520 2.508	V
Deviation of Reference Input Voltage Over Full Temperature Range	$V_{REF(dev)}$	Tmin ≤ Ta ≤ Tmax		3	17	MV
Ratio of Change in Reference Input Voltage to the Change in Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	ΔV_{KA} = 10V-V_{REF} ΔV_{KA} = 36V- 10V		-1.4 -1.0	-2.7 -2.0	mV/V
Reference Input Current	I_{REF}	R_1 = 10KΩ, R_2 = ∞		2	4	μA
Deviation of Reference Input Current Over Full Temperature Range	$I_{REF(dev)}$	R_1 = 10KΩ, R_2 = ∞		0.4	1.2	μA

Minimum Cathode Current for Regulation	$I_{K(min)}$			0.25	0.5	mA
Off-State Cathode Current	$I_{K(off)}$	V_{KA} = 40 V, V_{REF} = 0		0.17	0.9	μA
Dynamic Impedance	Z_{KA}	I_K = 10mA to 100 mA f ≤ 1.0KHz		0.27	0.5	Ω

Note :

1. The deviation parameter ΔVref is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies



The average temperature coefficient of the reference input voltage, aV_{ref} is defined as:

$$V_{ref}\frac{ppm}{℃}=\frac{(\frac{\Delta V_{ref}}{V_{ref}@25℃})\times 10^6}{\Delta V_A}=\frac{\Delta V_{ref}\times 10^6}{\Delta V_A(V_{ref}@25℃)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example: ΔV_{ref} = 8.0 mV and slope is positive,

$$V_{ref}@25℃=2.495V,\Delta T_A=70℃\quad \alpha V_{ref}=\frac{0.008\times 10^6}{70(2.495)}=45.8ppm/℃$$

2. The dynamic impedance ZKA is defined as

$$|Z_{KA}|=\frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{KA}'|=|Z_{KA}|(1+\frac{R1}{R2})$$

Test Circuits

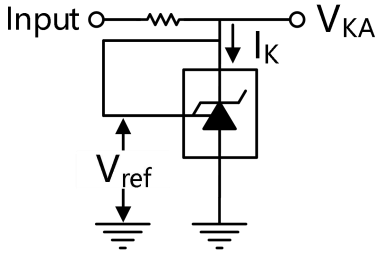


Figure 1. Test Circuit for $V_{KA} = V_{REF}$

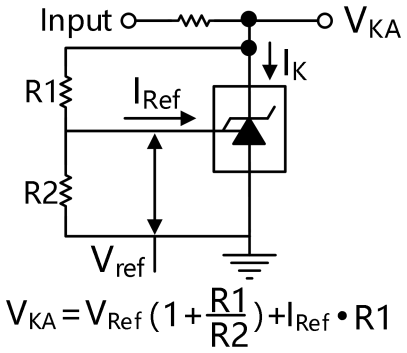


Figure 2. Test Circuit for $V_{KA} \geq V_{REF}$

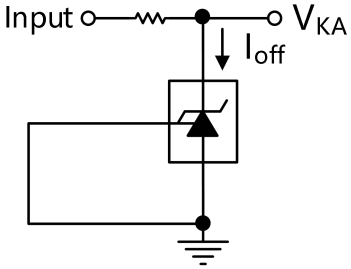


Figure 3. Test Circuit for I_{off}

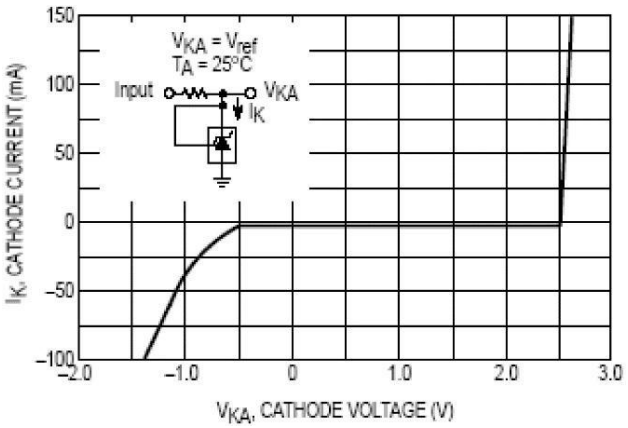


Figure 4. Cathode Current versus Cathode Voltage

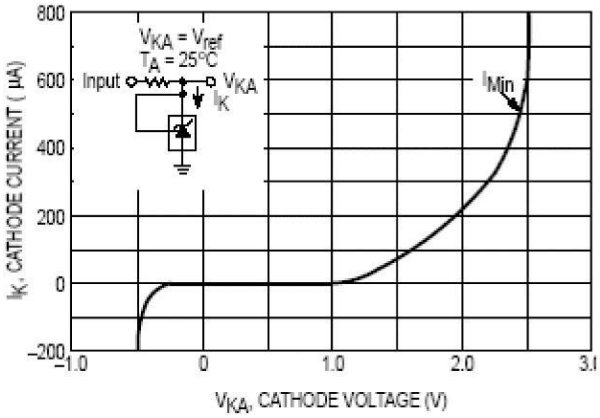


Figure 5. Cathode Current versus Cathode Voltage

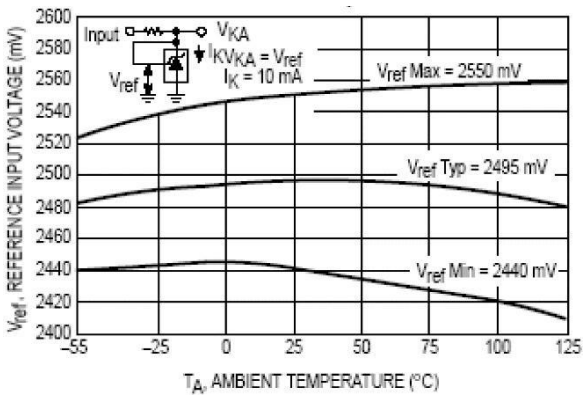
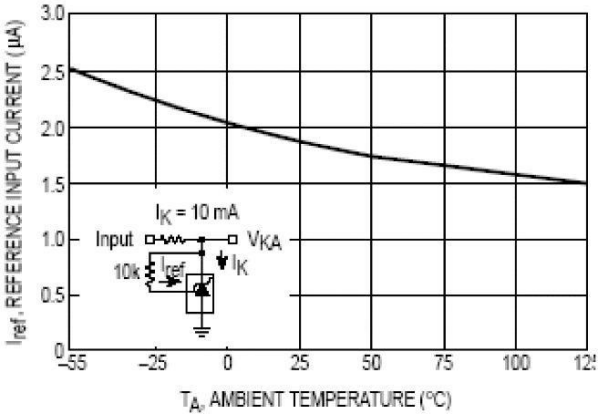


Figure 6. Reference Input Voltage versusFigure Ambient Temperature



7. Reference Input Current versus Ambient Temperature

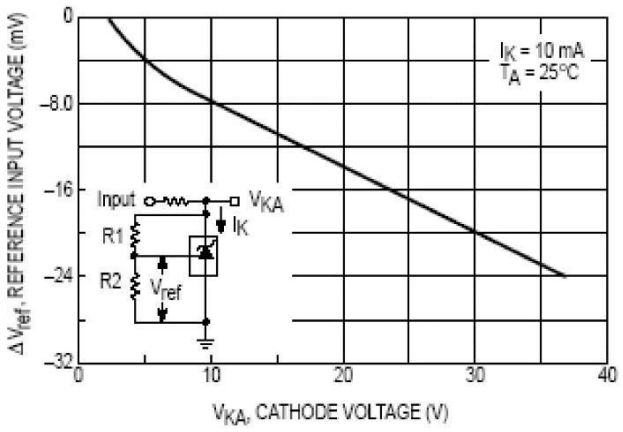


Figure 8. Change in Reference Input Voltage versus Cathode Voltage

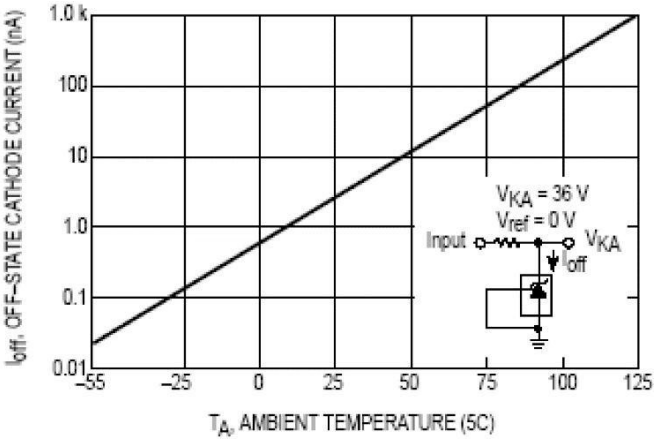


Figure 9. Off−State Cathode Current versus Ambient Temperature

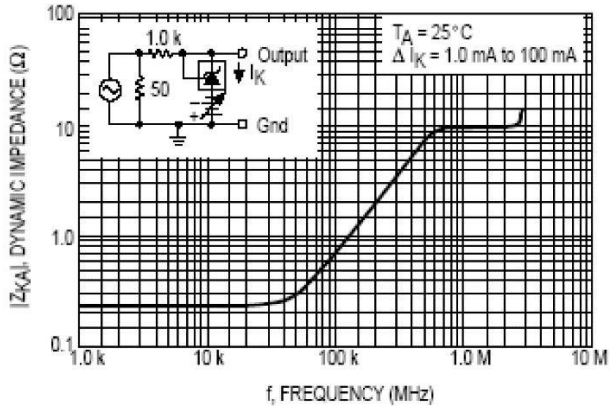
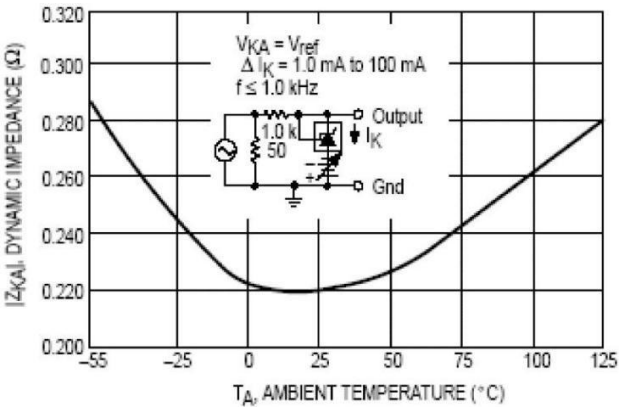


Figure 10. Dynamic Impedance versus Frequency Figure



11. Dynamic Impedance versus Ambient Temperature

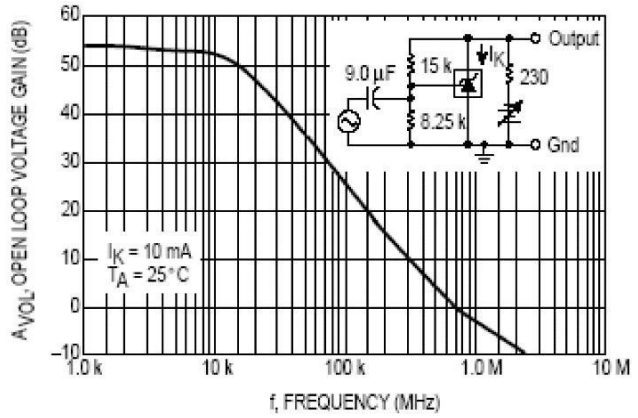


Figure 12. Open−Loop Voltage Gain versus Frequency

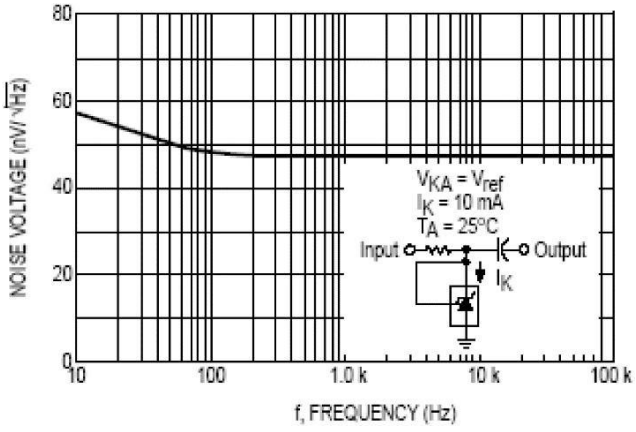


Figure 13. Spectral Noise Density

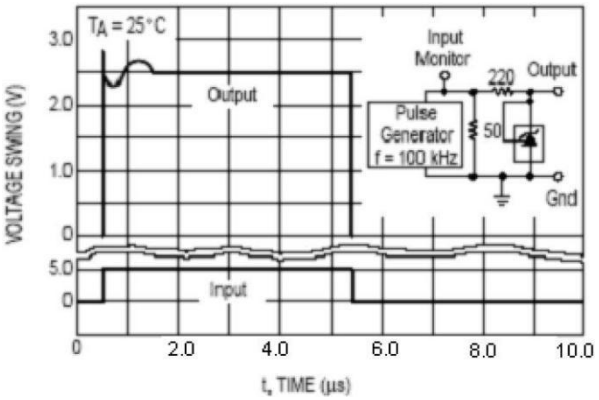
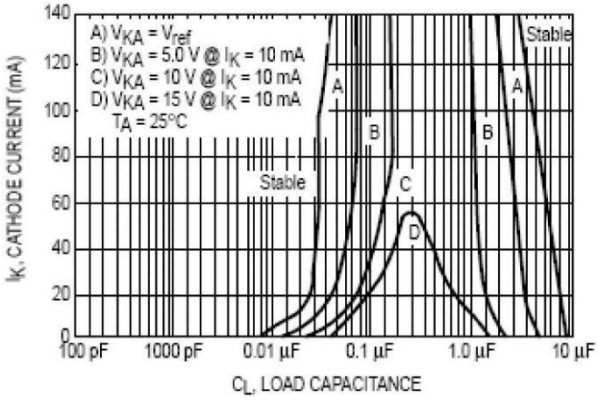


Figure 14. Pulse Response Figure



15. Stability Boundary Conditions

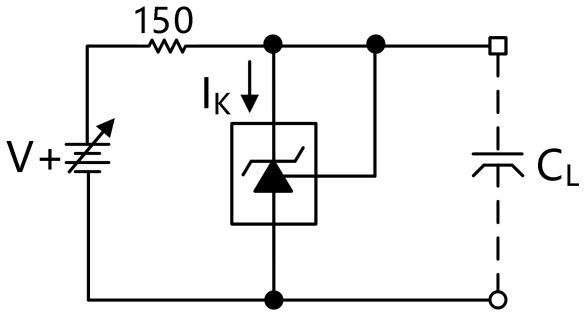


Figure 16. Test Circuit For Curve A of Stability Boundary Conditions

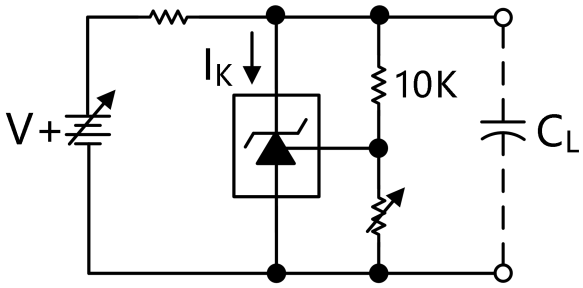


Figure 17. Test Circuit For Curves B, C, And D of Stability Boundary Conditions

Typical Applications

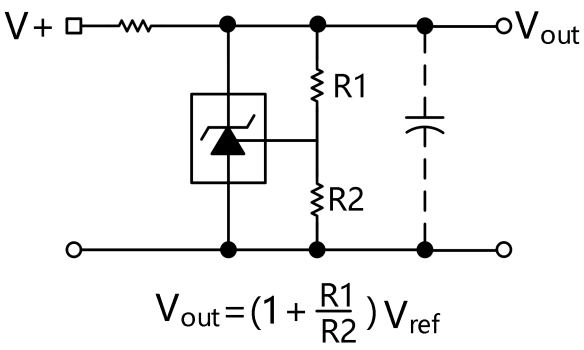


Figure 18. Shunt Regulator

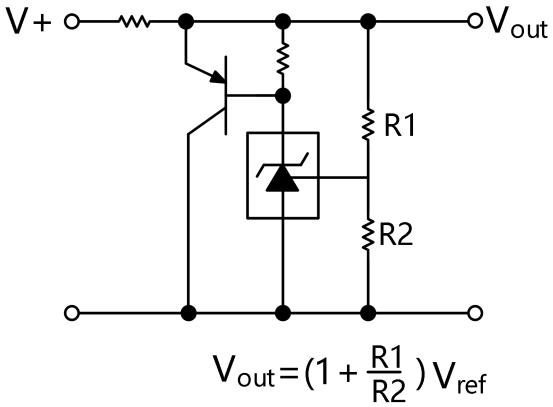
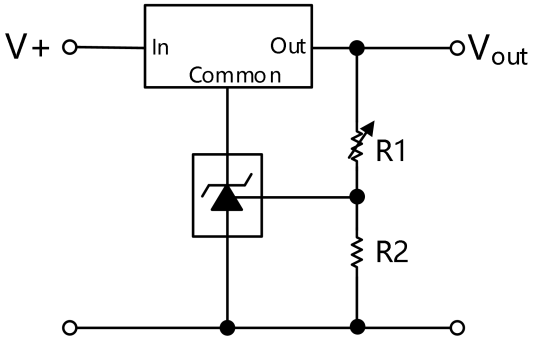


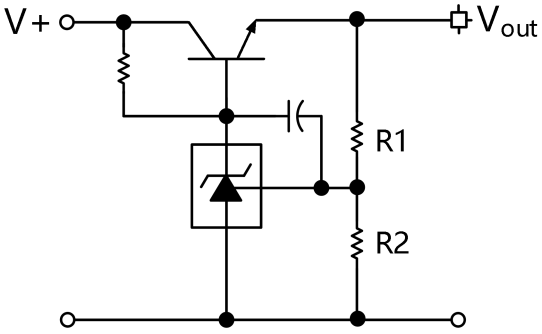
Figure 19. High Current Shunt Regulator



$$V_{out} = (1 + \frac{R1}{R2}) V_{ref}$$

$$V_{out}min = (V_{ref} + 5.0V)$$

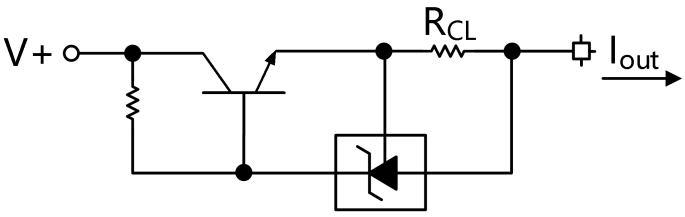
Figure 20. Output Control for a Three–Terminal Fixed Regulator



$$V_{out} = (1 + \frac{R1}{R2}) V_{ref}$$

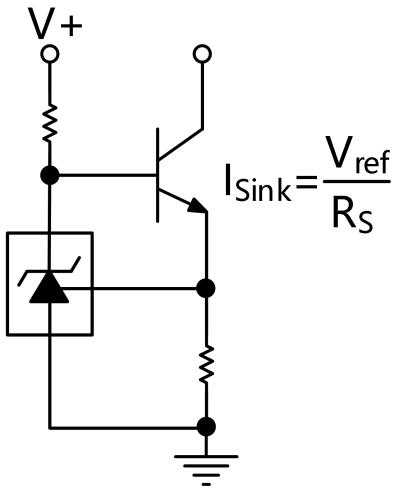
$$V_{out}min = V_{ref} + V_{be}$$

Figure 21. Series Pass Regulator

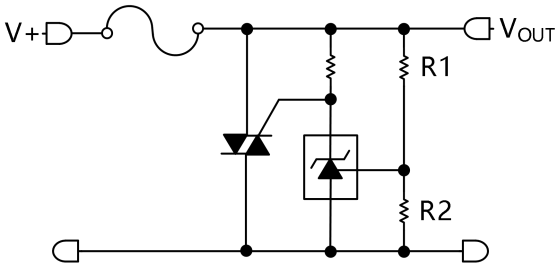


$$I_{out} = \frac{V_{ref}}{R_{CL}}$$

Figure 22. Constant Current Source Figure

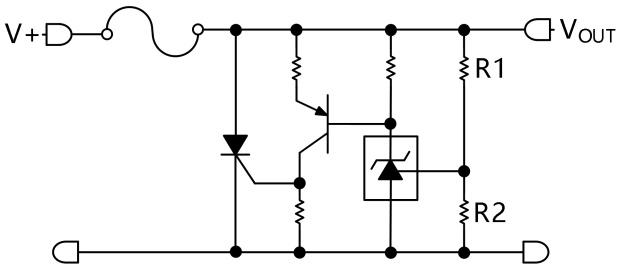


23. Constant Current Sink



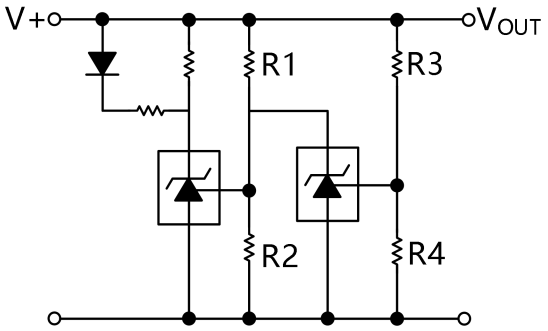
$$V_{OUT(trip)} = (1 + \frac{R1}{R2}) V_{ref}$$

Figure 24. TRIAC Crowbar



$$V_{OUT(trip)} = (1 + \frac{R1}{R2}) V_{ref}$$

Figure 25. SRC Crowbar



LED.Indicator is 'on' when V+ is between the upper and lower limits.

$$\text{Lower Limit} = (1 + \frac{R1}{R2})\, V_{ref}$$

$$\text{Upper Limit} = (1 + \frac{R3}{R4})\, V_{ref}$$

Figure 26. Voltage Monitor

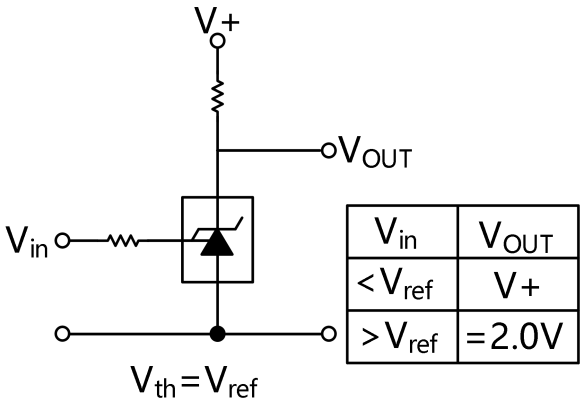


Figure 27. Single–Supply Comparator with Temperature–Compensated Threshold

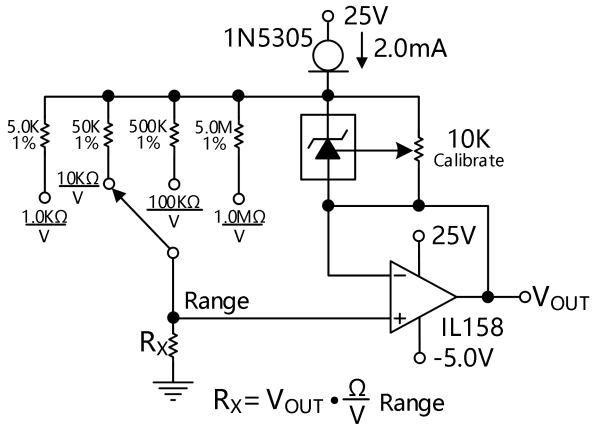


Figure 28. Linear Ohmmeter

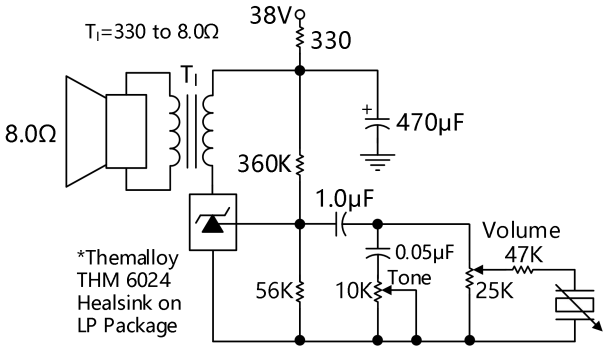


Figure 29. Simple 400 mW Phono Amplifier

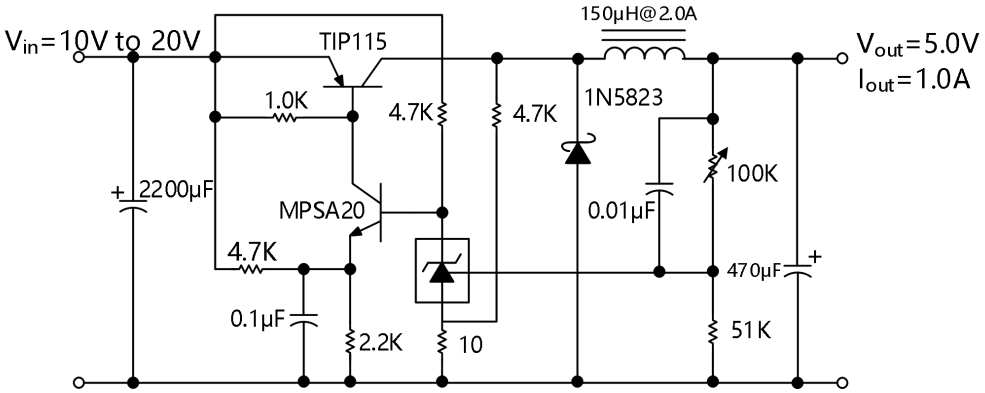


Figure 30. High Efficiency Step–Down Switching Converter

Test	Conditions	Results
Line Regulation	V_{IN}=10V to 20V，Io=1.0A	53mV（1.1%）
Load Regulation	V_{IN}=15V，Io=0A to 1.0A	25mV（0.5%）
Output Ripple	V_{IN}=10V，Io=1.0A	50mVpp P.A.R.D
Output Ripple	V_{IN}=20V，Io=1.0A	100mVpp P.A.R.D
Efficiency	V_{IN}=15V，Io=1.0A	82%

Application Information

The CD431 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non–standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 15. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition.

Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation. A simplified model of the CD431 is shown in Figure 31. When tested for stability boundaries, the load resistance is 150 Ω. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, Gm, develops a current whose amplidute is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of Gm flows through compensation capacitance, CP2. The voltage across CP2 drives the output dependent current source, Go, which is connected across the device cathode and anode.

Model component values are:

Vref = 1.78 V

Gm = 0.3 + 2.7 exp (–IC/26 mA)

where IC is the device cathode current and Gm is in mhos

Go = 1.25 (Vcp2) μmhos.

Resistor and capacitor typical values are shown on the model. Process tolerances are ±20% for resistors, ±10% for capacitors, and ±40% for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$P1 = \frac{1}{2_{\pi}R_{GM}C_{P1}} = \frac{1}{2_{\pi} * 1.0M * 20pF} = 7.96kHz$$

$$P2 = \frac{1}{2_{\pi}R_{P2}C_{P2}} = \frac{1}{2_{\pi} * 1.0M * 0.265pF} = 60kHz$$

$$Z1 = \frac{1}{2_{\pi}R_{Z1}C_{P1}} = \frac{1}{2_{\pi} * 15.9K * 20pF} = 500kHz$$

In addition, there is an external circuit pole defined by the load:

$$P_L = \frac{1}{2_{\pi}R_LC_L}$$

Also, the transfer dc voltage gain of the CD431 is:

$$G = G_M R_{GM} G_O R_L$$

Example 1:

I_C=10mA, R_L=230Ω, C_L=0, Define the transfer gain. The DC gain is:

$$G = G_M R_{GM} G_O R_L = (2.138)(1.0M)(1.25\mu)(230) = 615 = 56dB$$

$$\text{Loop gain} = G\frac{8.25k}{8.25k + 15k} = 218 = 47dB$$

The resulting transfer function Bode plot is shown in Figure 32. The asymptotic plot may be expressed as the following equation:

$$A_V = 615\frac{(\frac{1 + if}{500kHz})}{(\frac{1 + if}{8.0kHz})(\frac{1 + if}{60kHz})}$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9 degrees. This model matches the Open–Loop Bode Plot of Figure 12. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44 degrees.

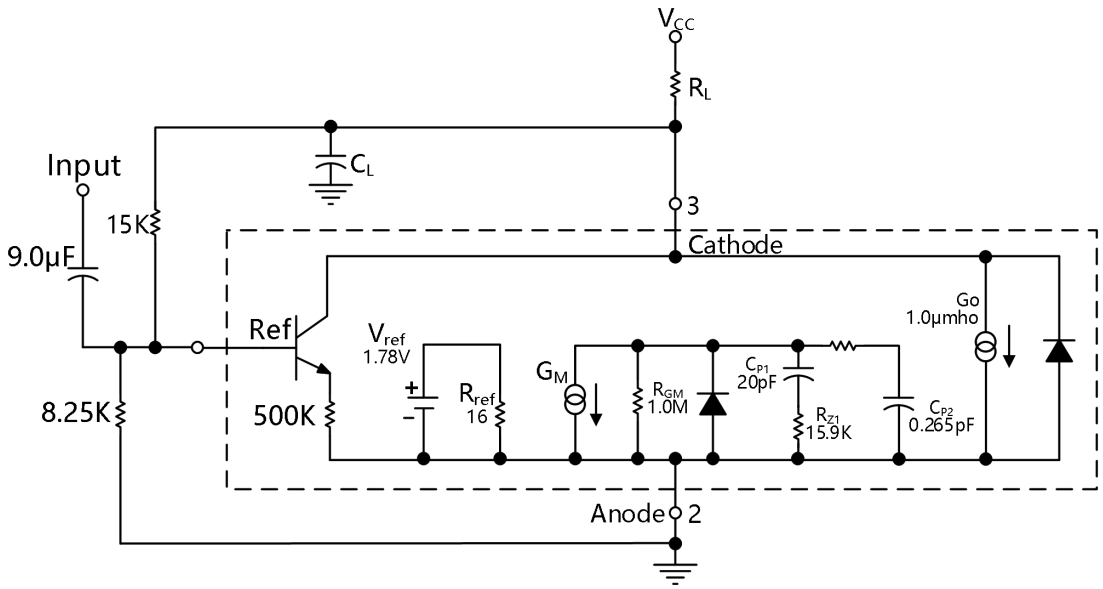


Figure 31. Simplified CD431 Device Model

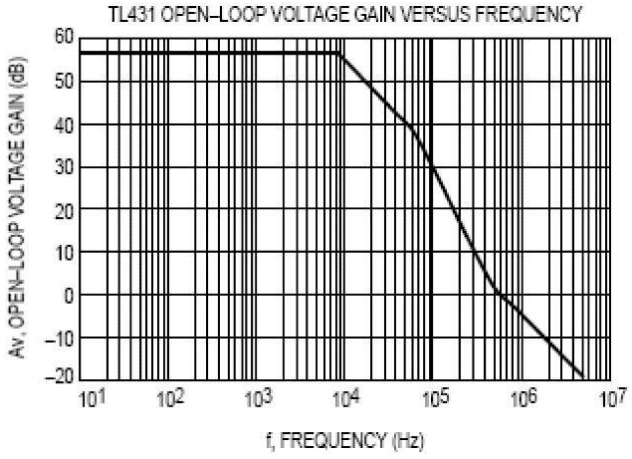


Figure 32. Example 1 Circuit Open Loop Gain Plot

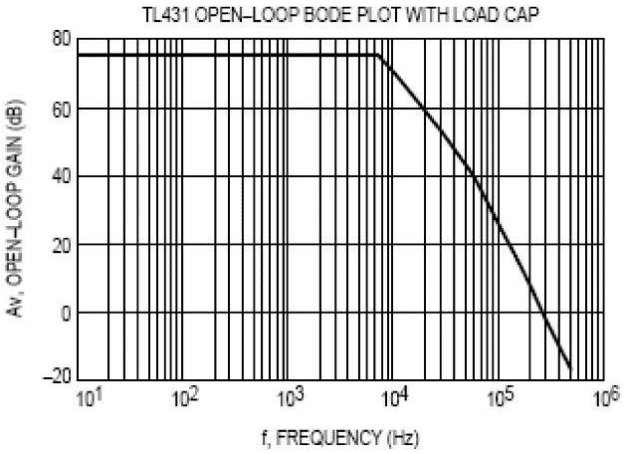


Figure 33. Example 2 Circuit Open Loop Gain Plot

Example 2.

I_C=7.5mA, R_L= 2.2kΩ, C_L =0.01 μF.

Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain. The DC gain is:

$$G = G_M R_{GM} G_0 R_L = (2.323)(1.0\ M)(1.25\ \mu)(2200) = 6389 = 76dB$$

The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

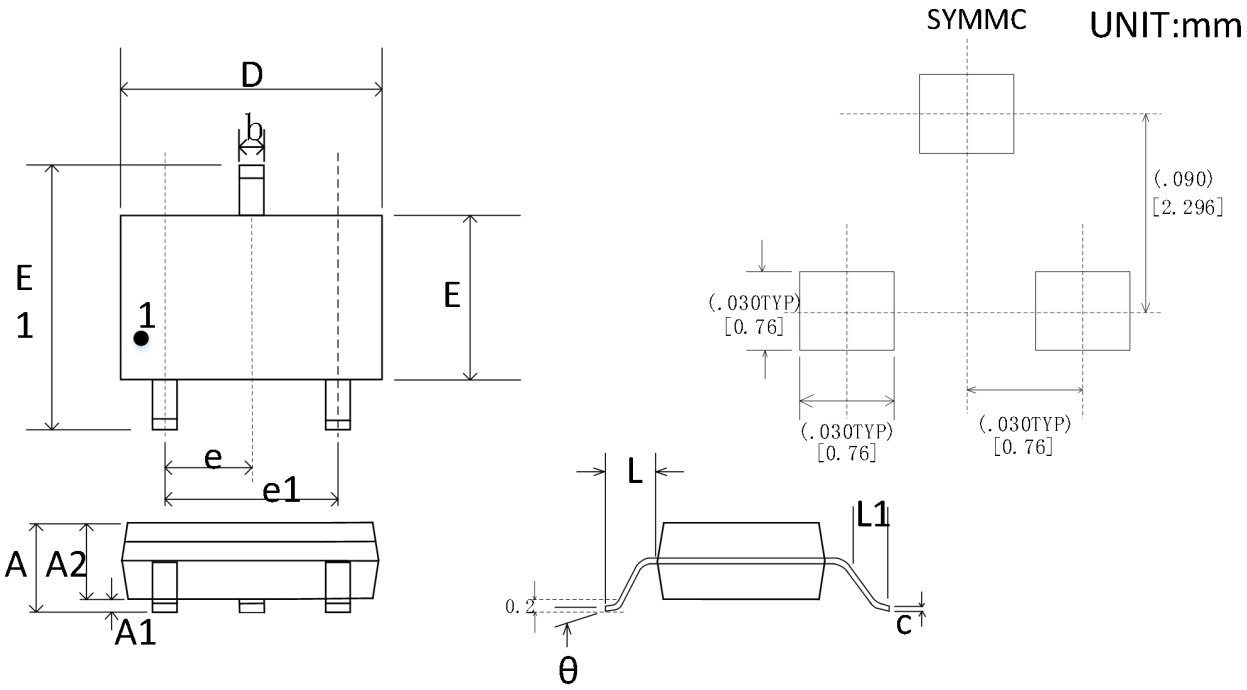
$$A_V = 615\frac{(\frac{1+if}{500kHz})}{(\frac{1+if}{8.0kHz})(\frac{1+if}{60kHz})(\frac{1+if}{7.2kHz})}$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance. Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about –46 degrees. Therefore, instability of this circuit is likely.

With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

Package Outline Dimensions

SOT23-3

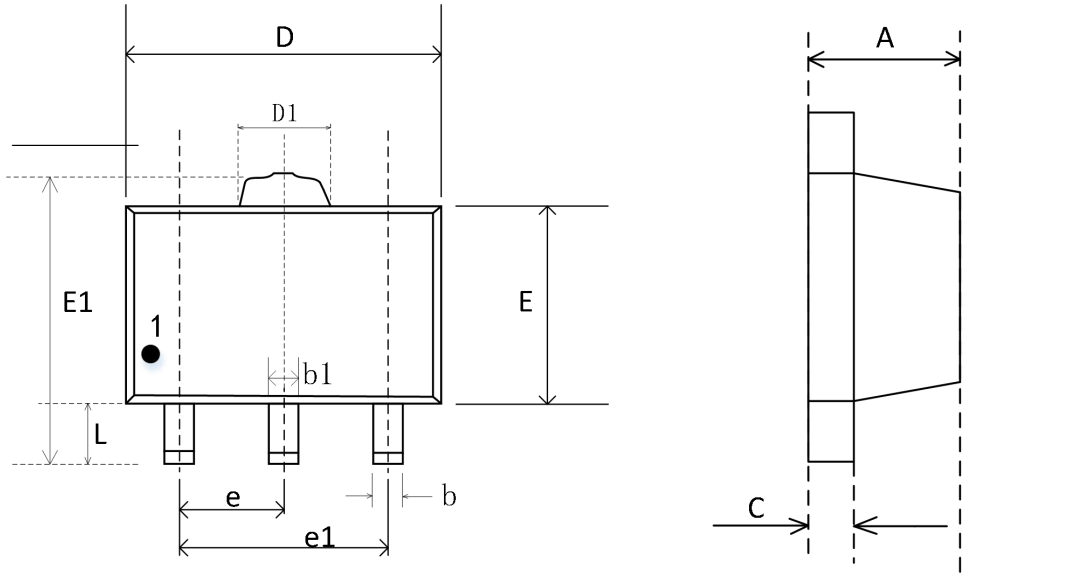


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045

b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT89-3

UNIT:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.360	0.560	0.014	0.022
c	0.350	0.440	0.016	0.017
D	4.400	4.600	0.173	0.181

D1	1.400	1.800	0.0.55	0.071
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP		0.060 TYP	
e1	2.900	3.100	0.114	0.122
L	0.900	1.100	0.035	0.043

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD431Z23	-40℃~125℃	SOT23-3	Tape and Reel, 3000
CD431Z89	-40℃~125℃	SOT89-3	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.12	Initial version	Regular update	WW	LYL	