CoreadDvices
承芯微电子

CD705A_CD706A_CD707A_CD708A

Low Cost Microprocessor Supervisory Circuits

Version: Rev 1.0.0 Date: 2025-6-3

Features

- Guaranteed $\overline{\text{RESET}}$ valid with VCC = 1V
- 190 μA quiescent current
- Precision supply voltage monitor
  - 4.65 V (CD705A/CD707A)
  - 4.40 V (CD706A/CD708A)
- 200 ms reset pulse width
- Debounced TTL/CMOS manual reset input
- Independent watchdog timer
- 1.60 sec timeout (CD705A/CD706A)
- Active high reset output (CD707A/CD708A)
- Voltage monitor for power fail or low battery
- Superior upgrade for CD705A to CD708A

Application

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Critical microprocessor supply

Description

The CD705A, CD706A, CD707A, CD708Amicroprocessor supervisory circuits are suitable for monitoring 5V power supplies/batteries and microprocessor activity.

The CD705A/CD706A provide power-supply monitoring circuitry that generate a reset output during power-up,power-down, and brownout conditions. The reset output remains operational with V_{CC} as low as 1V. Independent watchdog monitoring circuitry is also provided. This is activated if the watchdog input has not been toggled within 1.60 sec.

In addition, there is a 1.25V threshold detector to warn of power failures, to detect low battery conditions, or to monitor an additional power supply. An active low, debounced manual reset input ($\overline{\text{MR}}$) is also included.

The CD705A and CD706A are identical except for the reset threshold monitor levels, which are 4.65V and 4.40V, respectively. The CD707A and CD708A provide a similar functionality to the CD705A and CD706A and only differ in that a watchdog timer function is not available. Instead,

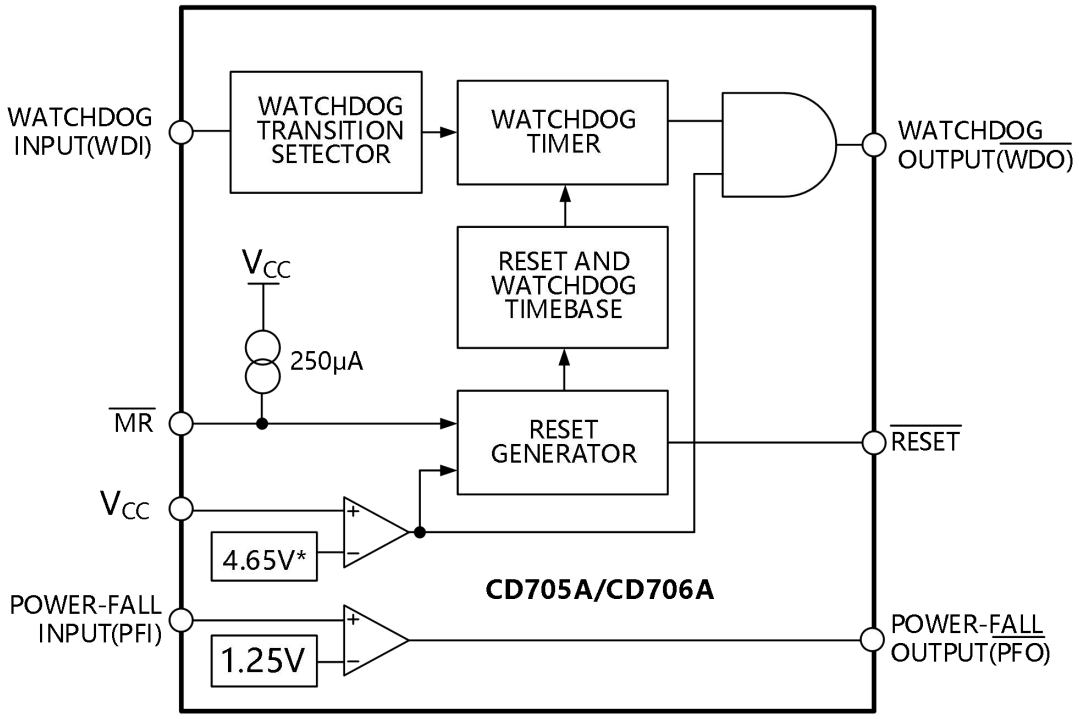
Chinese version:CD705A_CD706A_CD707A_CD708A

an active high reset output (RESET) is available as well as the active low reset output ($\overline{\text{RESET}}$). The CD707A and CD708A are identical except for the reset threshold monitor levels, which are 4.65V and 4.40V, respectively.All devices are available in narrow 8-lead SOIC packages.

Contents

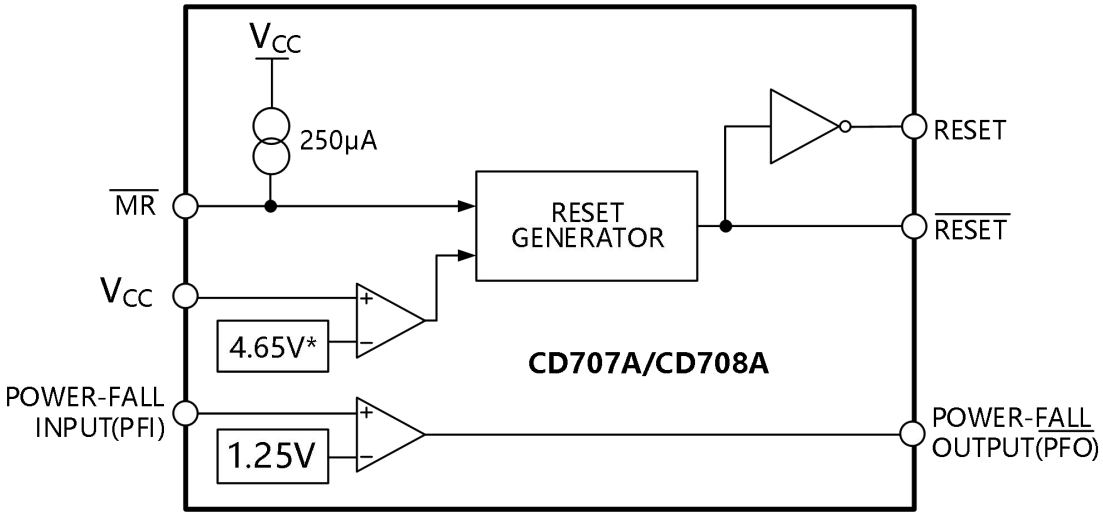
Features ..... - 1 -
Application ..... - 1 -
Description ..... - 1 -
Functional Block Diagram ..... - 3 -
Absolute Maximum Ratings ..... - 4 -
Electrical characteristics ..... - 4 -
Pin Configurations ..... - 6 -
Typical Characteristics ..... - 8 -
Circuit Information ..... - 9 -
Package Outline Dimensions ..... - 16 -
Package/Ordering Information ..... - 18 -
Revision Log ..... - 19 -

Functional Block Diagram



*VOLTAGE REFERENCE = 4.65V (CD705A), 4.40V (CD706A)

Figure 1. CD705A/CD706A



* VOLTAGE REFERENCE = 4.65V (CD707A), 4.40V (CD708A)

Figure 2. CD707A/CD708A

Chinese version:CD705A_CD706A_CD707A_CD708A

Absolute Maximum Ratings

T_A = 25°C, unless otherwise noted.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
All Other Inputs	−0.3V to V_{CC}+0.3V
Input Current	
V_{CC}	20mA
GND	20mA
Digital Output Current	20mA
Power Dissipation, N-8 PDIP	727mW
θ_{JA} Thermal Impedance	135℃/W
Power Dissipation, R-8 SOIC	470mW
θ_{JA} Thermal Impedance	110℃/W
Power Dissipation, RM-8 MSOP	900mW
θ_{JA} Thermal Impedance	206℃/W
Operating Temperature Range	
Industrial (Version A)	-40℃ to +85℃
Lead Temperature (Soldering,10 sec)	300℃
Vapor Phase (60 sec)	215℃
Infrared (15 sec)	220℃
Storage Temperature Range	-65℃ to +150℃
ESD Rating	>4.5kV

Electrical characteristics

V_{CC} = 4.75 V to 5.5 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		190	250	μA	
LOGIC OUTPUT					
Reset Threshold	4.5	4.65	4.75	V	CD705/CD707
	4.25	4.40	4.50	V	CD706/CD708
Reset Threshold Hysteresis		40		mV	

Chinese version:CD705A_CD706A_CD707A_CD708A

RESET PULSE WIDTH	160	200	280	ms	
RESET OUTPUT VOLTAGE	V_{CC}-1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 3.2 mA
			0.3	V	V_{CC} = 1 V, I_{SINK} = 50 µA
			0.3	V	V_{CC} = 1.2 V, I_{SINK} = 100 µA
RESET OUTPUT VOLTAGE	V_{CC}−1.5			V	CD707A/CD708A, I_{SOURCE} = 800 µA
			0.4	V	CD707A/CD708A, I_{SINK} = 1.2 mA
WATCHDOG TIMEOUT PERIOD (T_{WD})	1.00	1.60	2.25	sec	V_{IL} = 0.4 V, V_{IH} = V_{CC}×0.8,WDI = V_{CC}
WDI Pulse Width (T_{WP})	50			ns	
WATCHDOG INPUT					
WDI Input Threshold					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current	-1.0	-0.63	1.0	µA	WDI=0V
	-10	16.5	20	µA	WDI=V_{CC}
WDO OUTPUT VOLTAGE	V_{CC}-1.5			V	I_{SOURCE} = 800µA
			0.4	V	I_{SINK} = 1.2mA
MANUAL RESET INPUT					
MR Pull-Up Current	100	250	600	µA	MR = 0V
MR Pulse Width	150			ns	
MR INPUT THRESHOLD					
Logic Low			0.8	V	
Logic High	2.0			V	
MR TO RESET OUTPUT DELAY			250	ns	
POWER FAIL INPUT					
PFI Input Threshold	1.2	1.25	1.3	V	
PFI Input Current	-25	+0.01	+25	nA	
PFO OUTPUT VOLTAGE	V_{CC}-1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 3.2 mA

Pin Configurations

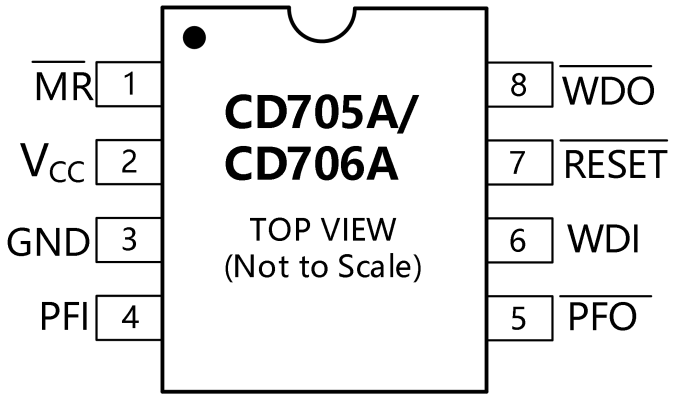


Figure 3. CD705A/CD706A PDIP/SOIC

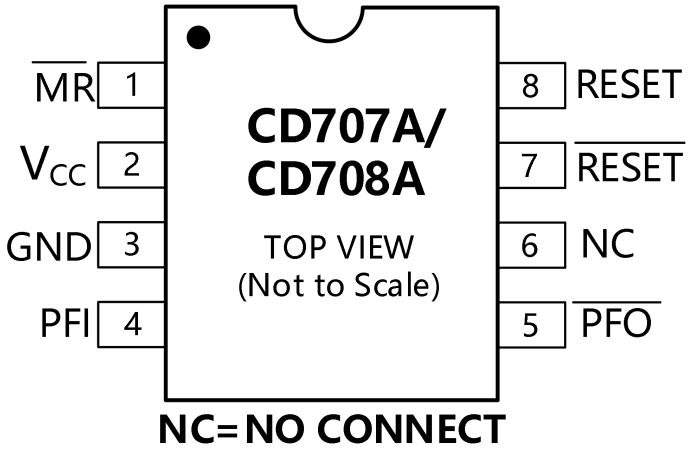


Figure 4. CD707A/CD708A PDIP/SOIC

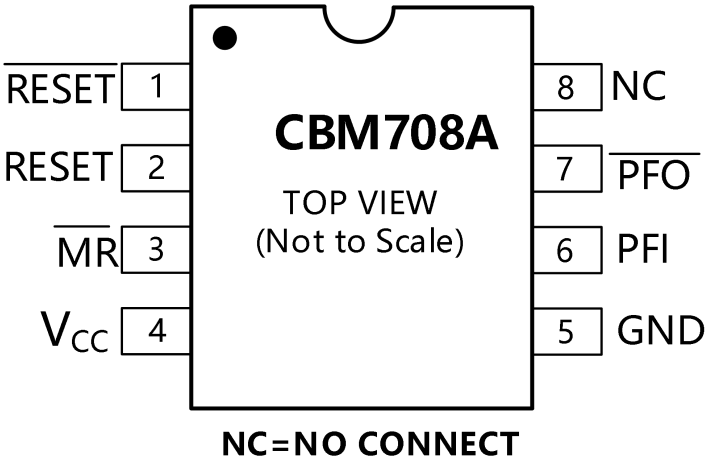


Figure 5. CD708A MSOP

Mnemonic	Pin Number			Description
	CD705A/ CD706A	CD707A/ CD708A	CD708A	
$\overline{MR}$	1	1	3	Manual Reset Input. When this pin is taken below 0.8V, a reset is generated. MR can be driven from TTL, CMOS logic, or from a manual reset switch as it is internally debounced. An internal 250μA pull-up current holds the input high when floating.
V_{CC}	2	2	4	5V Power Supply Input. Place a 0.1μF decoupling capacitor between the V_{CC} and GND pins.
GND	3	3	5	0V Ground Reference for All Signals.
PFI	4	4	6	Power Fail Input. PFI is the noninverting input to the power fail comparator. When PFI is less than 1.25V, PF goes low. If unused, PFI must be connected to GND.
PFO	5	5	7	Power Fail Output. PFO is the output from the power fail comparator. It goes low when PFI is less than 1.25V.
WDI	6	Not applicable	Not applicable	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, the watchdog output (WDO) goes low. The timer resets with each transition at the WDI input. Either a high to low or a low to high transition clears the counter. The internal timer is also cleared whenever reset is asserted. The watchdog timer is disabled when WDI is left floating or connected to a three-state buffer.
NC	Not applicable	6	8	No Connect.
$\overline{RESET}$	7	7	1	Logic Output. RESET goes low for 200ms when triggered. It can be triggered either by V_{CC} being below the reset threshold or by a low signal on the manual reset input (MR). RESET remains low whenever V_{CC} is below the reset threshold (4.65V in CD705A/CD707A, 4.40 V in CD706A/CD708A). It remains low for 200ms after V_{CC} goes above the reset threshold or MR goes from low to high. A watchdog timeout does not trigger RESET unless WDO is connected to MR.
WDO	8	Not applicable	Not applicable	Watchdog Output. WDO remains low until the watchdog timer is cleared. WDO also goes low during low line conditions. Whenever V_{CC} is below the reset threshold, WDO goes low if the internal WDO remains low. As soon as V_{CC} goes above the reset threshold, WDO goes high.
RESET	Not applicable	8	2	Logic Output. RESET is an active high output suitable for systems that use active high reset logic. It is the inverse of RESET.

Typical Characteristics

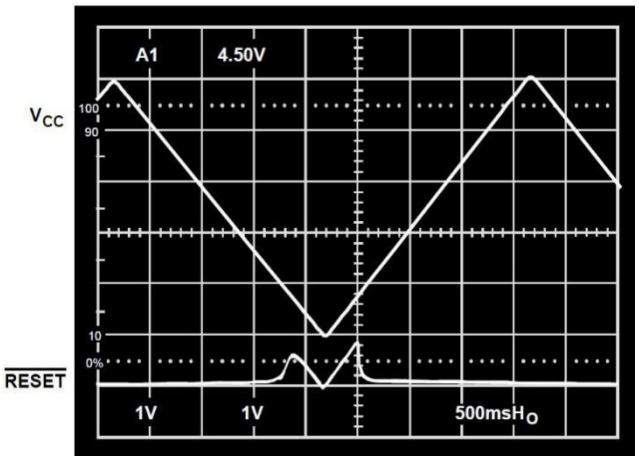


Figure 6. RESET Output Voltage vs. Supply Voltage

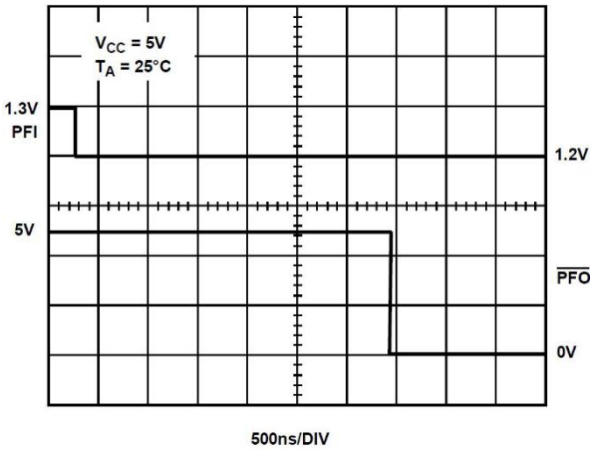


Figure 8. PFI Comparator Assertion Response Time

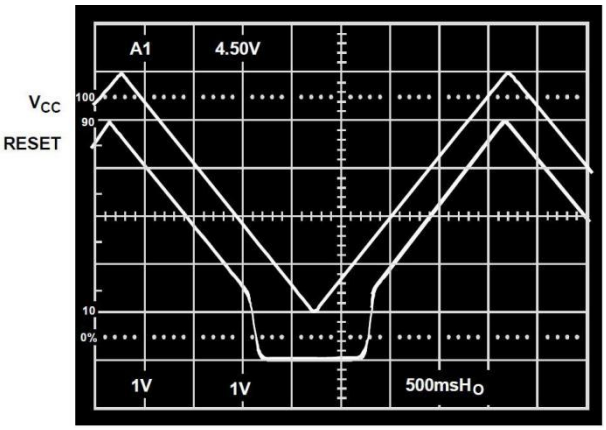


Figure 7. CD707/CD708 RESET Output vs.Supply Voltage

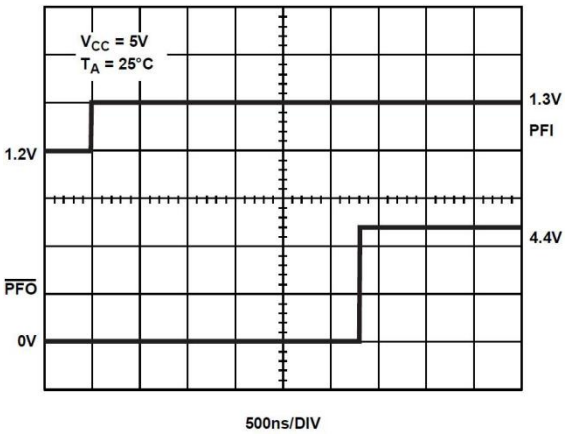


Figure 9. PFI Comparator Deassertion Voltage Response Time

Chinese version:CD705A_CD706A_CD707A_CD708A

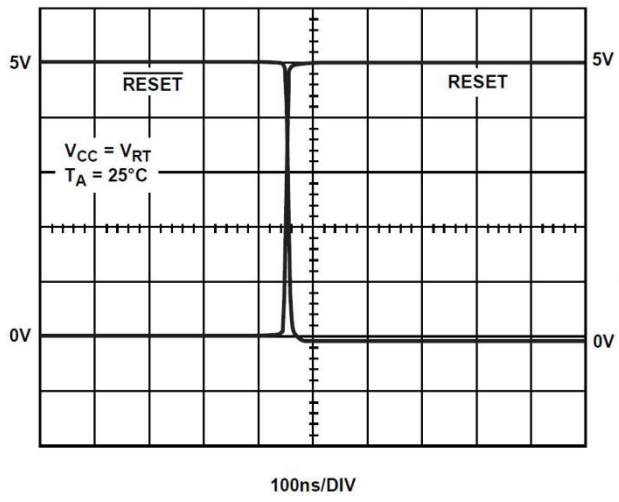


Figure 10. RESET ,RESET Assertion

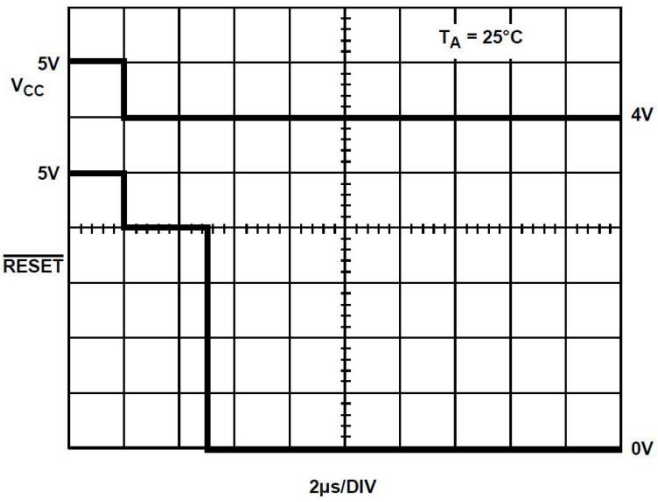


Figure 12. CD705A/CD707A RESET Response Time

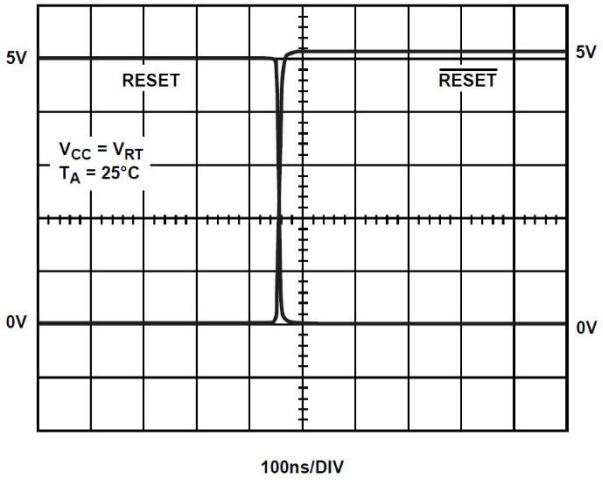


Figure 11. RESET, RESET Deassertion

Circuit Information

- **Power Fail Reset Output**

RESET is an active low output that provides a reset signal to the microprocessor whenever the VCC input is below the reset threshold. An internal timer holds RESET

low for 200 ms after the voltage on VCC rises above the threshold. This functions as a power-on reset signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. The RESET output is guaranteed to remain valid (low) with VCC as low as 1V. This sensures that the microprocessor is held in a stable shutdown condition as the power supply voltage ramps up.

In addition to RESET, an active high RESET output is also available on the CD707A/CD708A

.This is the complement of RESET and is useful for processors requiring an active high reset

signal.

- **Manual Reset**

The manual reset input (MR) allows other reset sources, such as a manual reset switch, to generate a processor reset. The input is effectively debounced by the timeout period (200 ms typically). The MR input is TTL-/CMOS-compatible, so it can also be driven by any logic reset output.

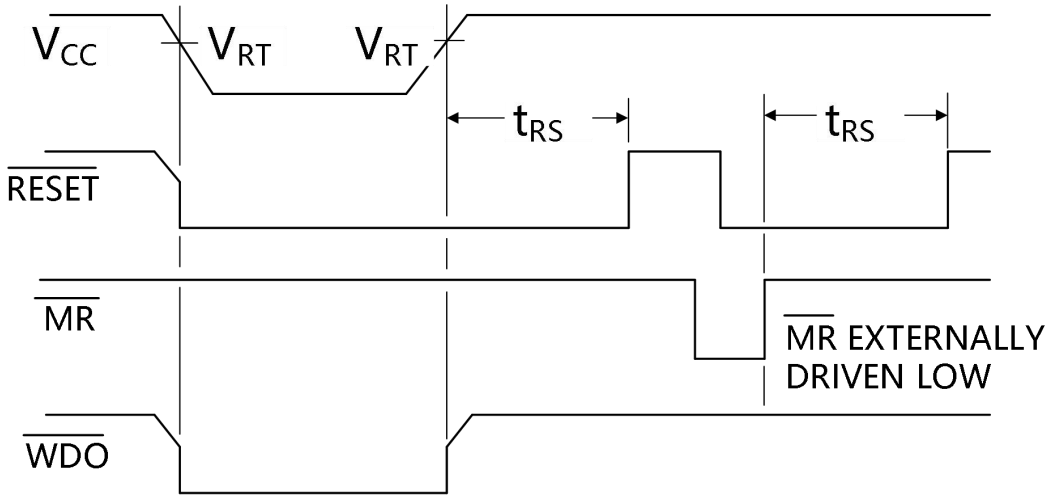


Figure 13. RESET, MR, and WDO Timing

- **Watchdog Timer (CD705A/CD706A)**

The watchdog timer circuit can monitor the activity of the micro-processor to check that it is not stalled in an indefinite loop. An output line on the processor toggles the watchdog input (WDI) line. If this line is not toggled within the timeout period (1.60 sec), then the watchdog output (WDO) goes low. The WDO

can be connected to a nonmaskable interrupt (NMI) on the processor; therefore, if the watchdog timer times out, an interrupt is gen-erated. The interrupt service routine then rectifies the problem.

If a RESET signal is required when a timeout occurs, the WDO must connect to the manual reset input (MR).

The watchdog timer is cleared by either a high to low or a low to high transition on WDI. It is also cleared by RESET going low; therefore, the watchdog timeout period begins after RESET goes high.

When VCC falls below the reset threshold, WDO is forced low, whether or not the watchdog timer has timed out. Normally, this generates an interrupt, but it is overridden by RESET going low.

The watchdog monitor can be deactivated by floating the WDI. The WDO can then be used as a low line output because it goes low only when VCC falls below the reset threshold.

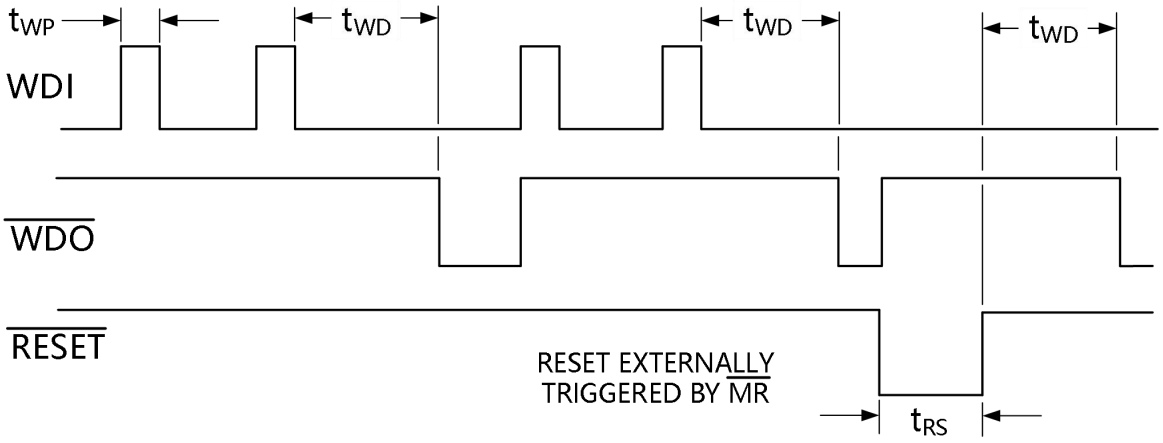


Figure 14. Watchdog Timing

- **Power Fail Comparator**

The power fail comparator is an independent comparator that can monitor the input power supply. The comparator inverting input is internally connected to a 1.25V reference voltage. The noninverting input is available at the PFI input. This input can monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25V, the comparator output (PFO) goes low, indicating a power failure. For early warning of power failure, the comparator monitors the preregulator input by choosing an appropriate resistive divider network. The PFO output can interrupt the processor so a shutdown procedure is implemented before power is lost.

As the voltage on the PFI pin is limited to V_{CC} + 0.3V, it is recommended to connect the PFI pin with a Schottky diode to the RESET pin as shown in Figure 15. This helps clamping the PFI pin voltage during device power up and operation.

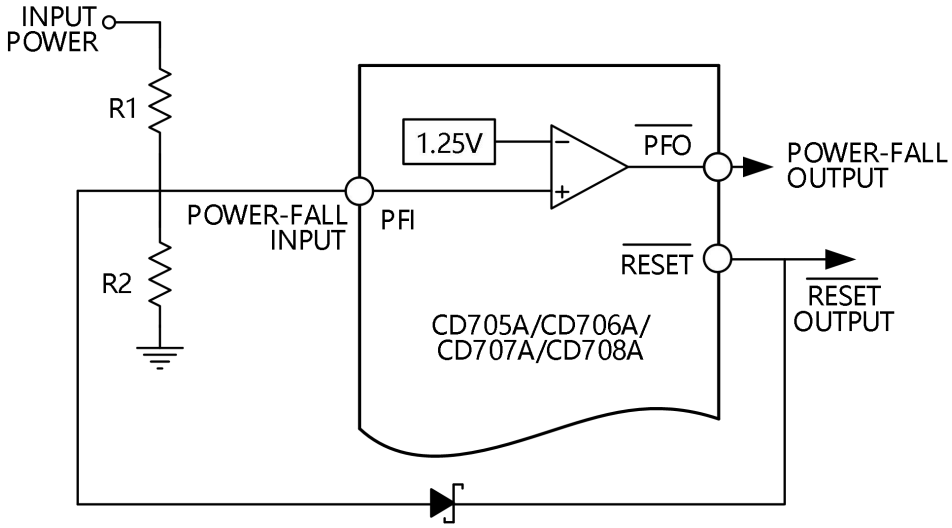


Figure 15. Power Fail Comparator

- **Adding Hysteresis to the Power Fail Comparator**

For increased noise immunity, hysteresis can be added to the power fail comparator. Because the comparator circuit is noninverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 16.

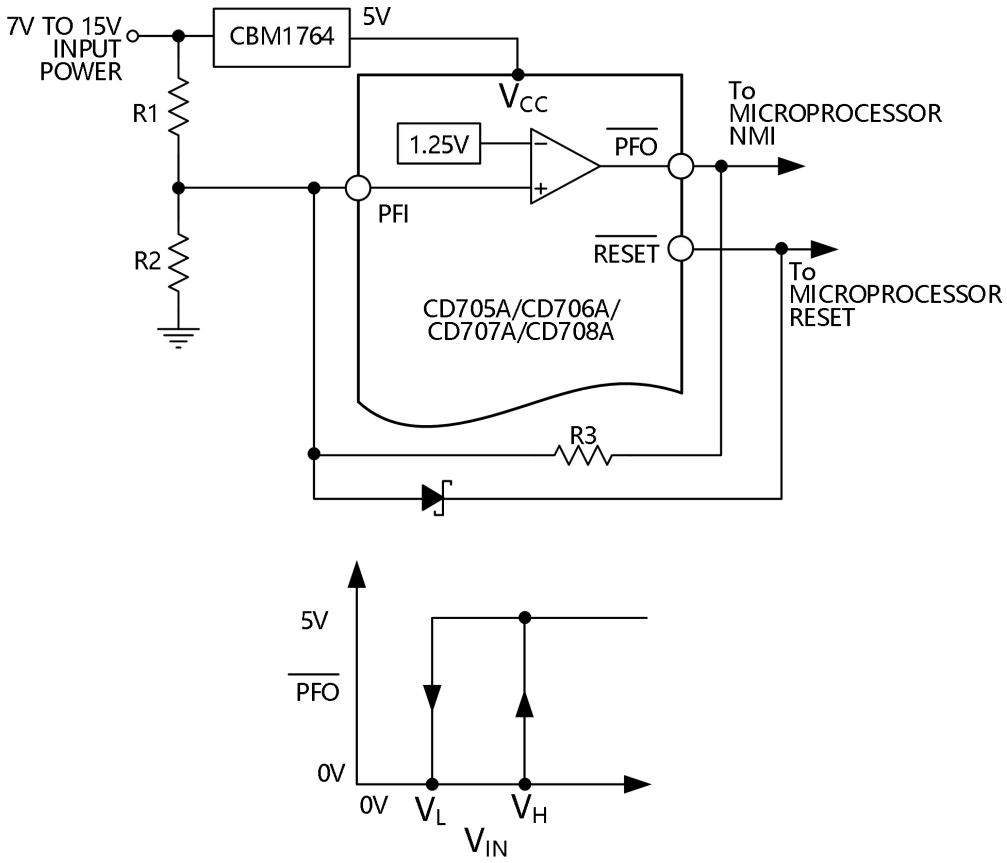


Figure 16. Adding Hysteresis to the Power Fail Comparator

When PFO is low, Resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, Resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity can be achieved by connecting a capacitor between PFI and GND. The equations calculate the hysteresis are as follows:

$$V_H = 1.25[1 + \left(\frac{R2 + R3}{R2 \times R3}\right) R1]$$

$$V_L = 1.25 + R1\left(\frac{1.25}{R2} - \frac{V_{CC} - 1.25}{R3}\right)$$

$$V_{MID} = 1.25(\frac{R1 + R2}{R2})$$

- **Valid Reset Below 1V V_{CC}**

The CD705A/CD706A/CD707A/CD708A are guaranteed to provide a valid reset level with V_{CC} as low as 1 V (see the Typical Performance Characteristics section). As V_{CC} drops below 1V,the internal transistor does not have sufficient drive to hold the voltage RESET at 0V. A pull-down resistor can connect externally, as shown in Figure 17, to hold the line low if required.

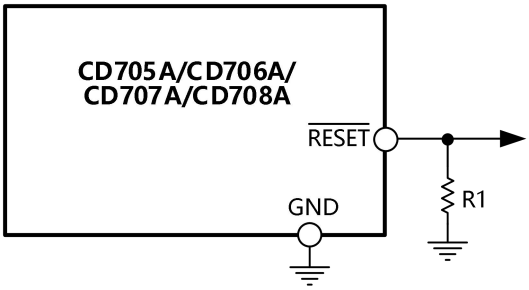


Figure 17. RESET Valid Below 1V

- **Applications Information**

A typical application circuit is shown in Figure 18. The un-regulated dc input supply is monitored using PFI via the resistive divider network. Resistor R1 and Resistor R2 must be selected so when the supply voltage drops below the desired level (such as 8V), the voltage on PFI drops below the 1.25V threshold, thereby generating an interrupt to the microprocessor. Monitoring the preregulator input provides additional time to execute an orderly shutdown procedure before power is lost.

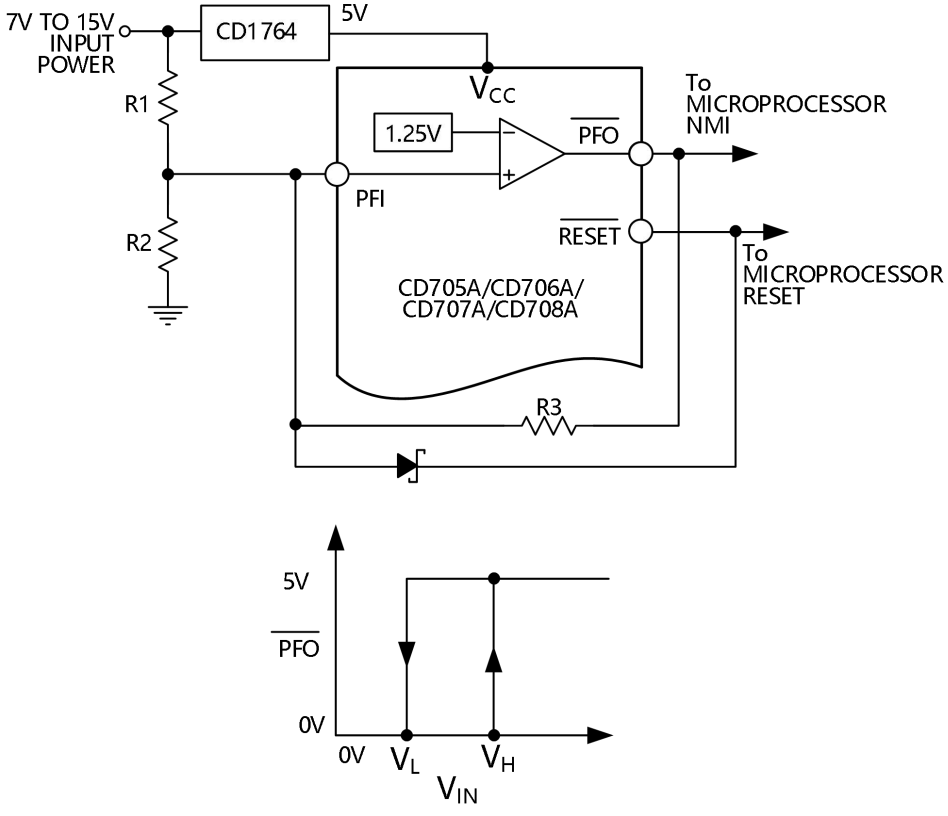


Figure 18. Typical Application Circuit

Microprocessor activity is monitored using WDI. This is driven using an output line from the processor. The software routines toggle this line at least once every 1.60 seconds. If a problem occurs and this line is not toggled, WDO goes low and a nonmaskable interrupt is generated.This interrupt routine can clear the problem.

If in the event of inactivity on the WDI line, a systeMReset is required, WDO must connect to MR as shown in Figure 19.

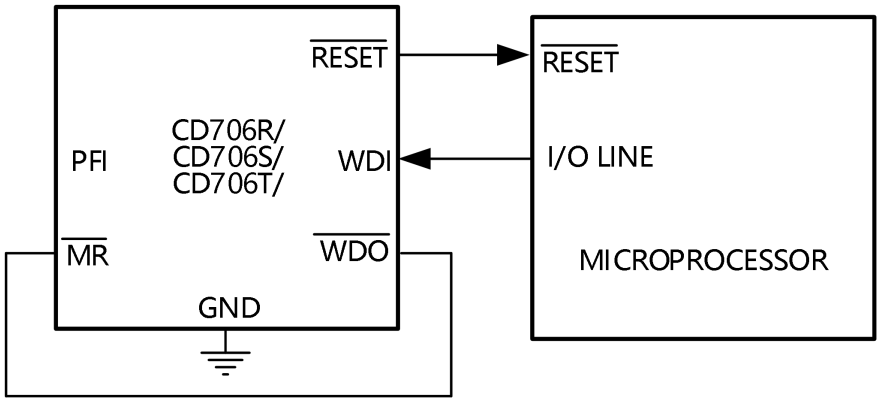


Figure 19. RESET From WDO

- **Monitoring Additional Supply Levels**

It is possible to use the power fail comparator to monitor a second supply as shown in Figure 20. The two sensing resistors, R1 and R2, are selected so the voltage on PFI drops below 1.25V at the minimum acceptable input supply.PFO can connect to MR so a reset is generated when the supply drops out of tolerance. In this case, if either supply drops out of tolerance, a reset is generated.

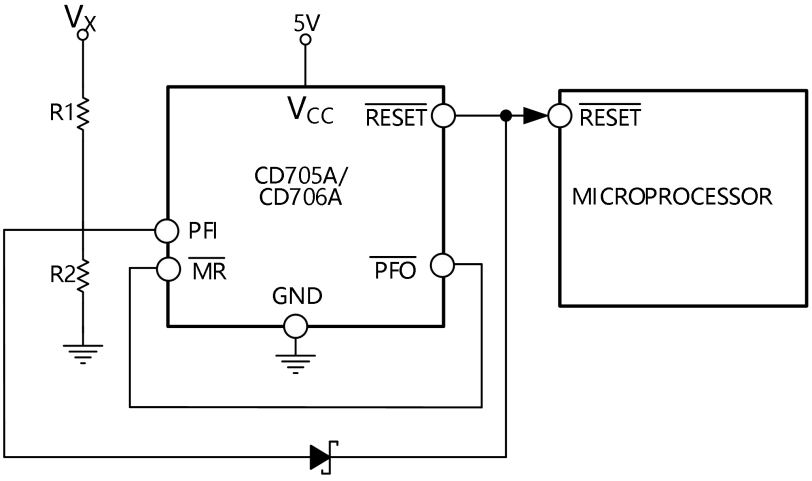


Figure 20. Monitoring 5 V and an Additional Supply, VX

- **Microprocessor With Bidirectional Reset**

To prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor must be inserted between the CD705A/ CD706A/ CD707A/ CD708A RESET output pin and the microprocessor RESET pin. This limits the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7kΩ. If the reset output is required for other uses, it must be buffered, as shown in Figure 21.

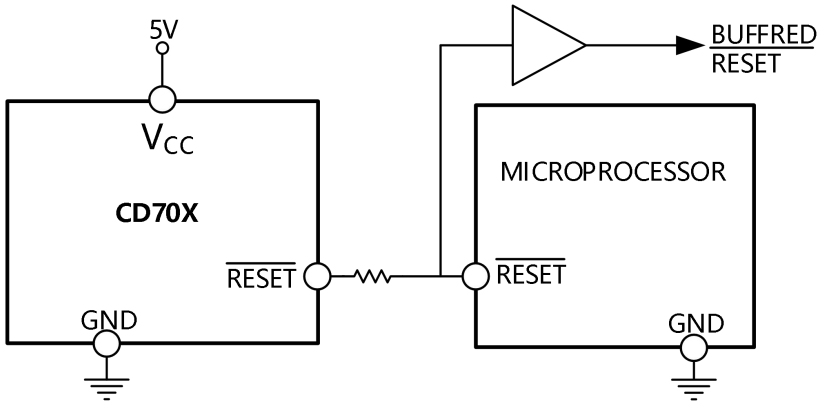
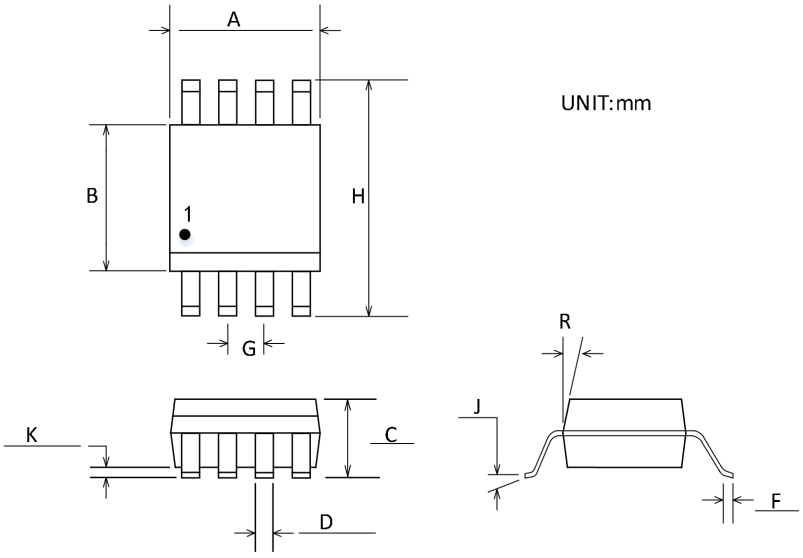


Figure 21. Bidirectional Input/Output RESET

Chinese version:CD705A_CD706A_CD707A_CD708A

Package Outline Dimensions

MSOP-8

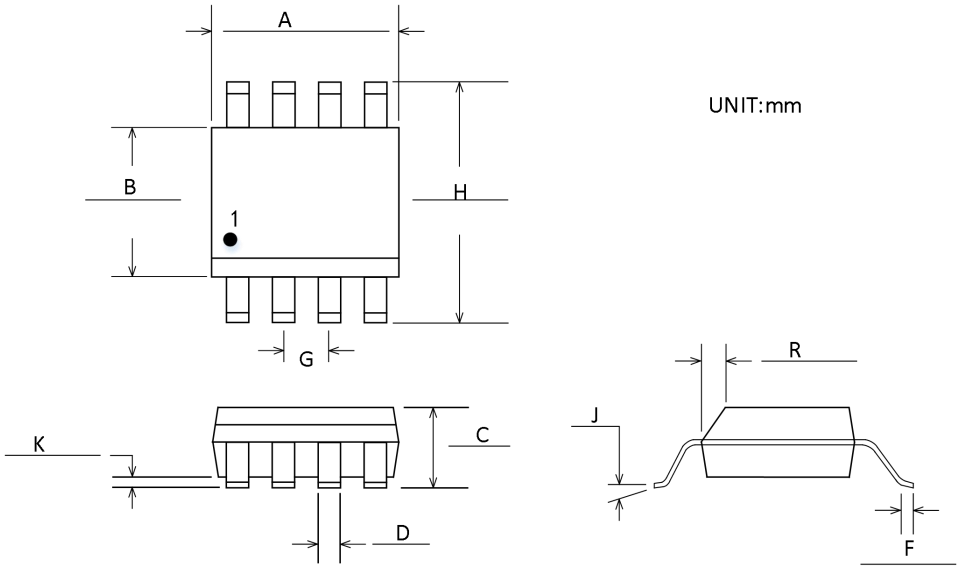


UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	2.80	3.20
B	2.80	3.20
C	1.10MAX	
D	0.25	0.40
F	0.40	0.80
G	0.65BSC	
H	4.65	5.15
J	0°	6°
K	0.05	0.15
R	15°MAX	

Chinese version:CD705A_CD706A_CD707A_CD708A

SOP-8



UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.31	0.51
F	0.40	1.27
G	1.27BSC	
H	5.80	6.20
J	0°	8°
K	0.10	0.25
R	0.25	0.50

Chinese version:CD705A_CD706A_CD707A_CD708A

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD705AS8	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 2500
CD705AS8-RL	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 3000
CD705AS8-REEL	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 4000
CD705AMS8	-40℃~85℃	MSOP-8	Tape and Reel,3000
CD706AS8	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 2500
CD706AS8-RL	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 3000
CD706AS8-REEL	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 4000
CD706AMS8	-40℃~85℃	MSOP-8	Tape and Reel,3000
CD707AS8	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 2500
CD707AS8-RL	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 3000
CD707AS8-REEL	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 4000
CD707AMS8	-40℃~85℃	MSOP-8	Tape and Reel,3000
CD708AS8	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 2500
CD708AS8-RL	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 3000
CD708AS8-REEL	-40℃~85℃	SOIC-8(SOP8)	Tape and Reel, 4000
CD708AMS8	-40℃~85℃	MSOP-8	Tape and Reel,3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.3	Initial version	Regular update	WW	LYL	

Chinese version:CD705A_CD706A_CD707A_CD708A