CoreadDvices
承芯微电子

CD803_CD809_CD810

Microprocessor Supervisory Circuit

Version: Rev 1.0.0 Date: 2025-6-3

Features

- Recision supply voltage monitor
  - 2.32V(CD803Z/CD809Z/CD810Z)
  - 2.63 V(CD803R/CD809R/CD810R)
  - 2.93 V(CD803S/CD809S/CD810S)
  - 3.08 V(CD803T/CD809T/CD810T)
  - 4.00 V(CD803J/CD809J/CD810J)
  - 4.38 V(CD803M/CD809M/CD810M)
  - 4.63 V(CD803L/CD809L/CD810L)
- 17 µA quiescent current
- Reset assertion down to 1 V VCC
- 140 ms minimum power-on reset
  - Open-drain RESET output (CD803X)
  - Push-pull RESET output (CD809X)
  - Push-pull RESET output (CD810X)

* X=L,M,J,T,S,R,Z

Application

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments

Description

The CD803X/CDM809X/CD810X supervisory circuits monitor the power supply voltage in microprocessor systems. They provide a reset output during power-up, power-down, and brownout conditions. On power-up, an internal timer holds reset asserted for 240 ms. This holds the microprocessor in a reset state until conditions have stabilized. The reset output remains operational with VCC as low as 1 V. The CD803X and CD809X provide an active low reset signal ($\overline{\text{RESET}}$), whereas the CD810X provides an active high signal (RESET) output. The CD809X and CD810X have push-pull outputs, whereas the CD803X has an open-drain output, which requires an external pull-up resistor.

Seven reset threshold voltage options are available, suitable for monitoring a variety of supply voltages (see Table 3).

The reset comparator features built-in glitch immunity, making it immune to fast transients on VCC.

The CD803X/CD809X/CD810X consume only 17 μA, making them suitable for low power, portable equipment. The CD803X is available in a 3-lead SC70; the CD809X/CD810X are available in 3-lead SOT-23 and 3-lead SC70 packages.

Contents

Functional Block Diagrams

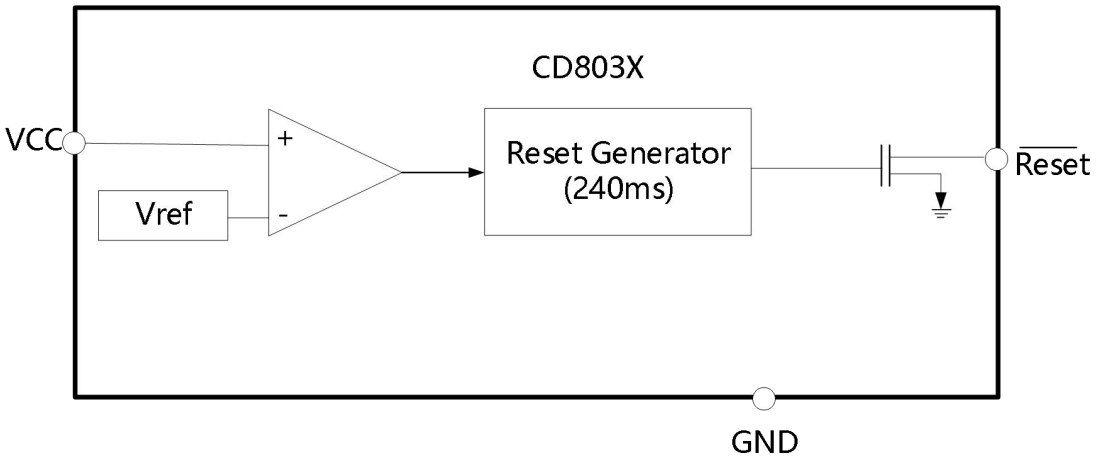
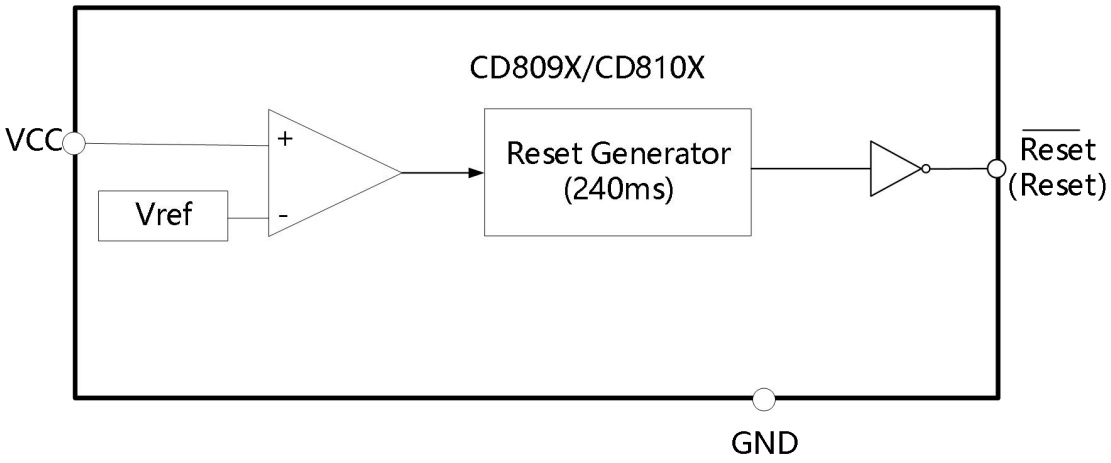


Figure1. CD803X Series product block diagram



*VREF (reference voltage) = seven monitoring voltage points, see Table 3 for details

Figure2. CD809X/CD810X Series product block diagram

Chinese version:CD803_CD809_CD810

Electrical characteristics

V_{CC} = full operating range, T_A=T_{MIN} to T_{MAX}, V_{CC} typical = 5 V for L/M/J models, 3.3 V for T/S models, 3 V for R models, and 2.5 V for Z models, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		24	35	μA	V_{CC} < 5.5V,CD8xxL/M/J
		17	30	μA	V_{CC} < 3.6V,CD8xxR/S/T/Z
LOGIC OUTPUT					
Reset Threshold(V_{RST})	4.56	4.63	4.70	V	CD803L/CD809L/CD810L
	4.31	4.38	4.45	V	CD803M/CD809M/CD810M
	3.93	4.00	4.06	V	CD803J/CD809J/CD810J
	3.04	3.08	3.11	V	CD803T/CD809T/CD810T
	2.89	2.93	2.96	V	CD803S/CD809S/CD810S
	2.59	2.63	2.66	V	CD803R/CD809R/CD810R
	2.28	2.32	2.35	V	CD803Z/CD809Z/CD810Z
Reset Active Timeout Period	140	240	460	ms	
$\overline{\text{RESET}}$ OUTPUT VOLTAGE LOW (CD803X/CD809X)					
V_{OL}			0.3	V	V_{CC} = V_{TH} min, I_{SINK} = 1.2 mA, CD803R/S/T/Z, CD809R/S/T/Z
			04	V	V_{CC} = V_{TH} min, I_{SINK} = 3.2 mA, CD803L/M/J, CD809L/M/J
			0.3	V	V_{CC} > 1.0 V, I_{SINK} = 50 μA
$\overline{\text{RESET}}$ OUTPUT VOLTAGE HIGH(CD809X)					
V_{OH}	0.8 V_{CC}			V	V_{CC} > V_{TH} max, I_{SOURCE} = 500 μA, CD809R/S/T/Z
	V_{CC} − 1.5			V	V_{CC} > V_{TH} max, I_{SOURCE} = 800 μA, CD809L/M/J
RESET OUTPUT VOLTAGE LOW (CD810X)					
V_{OL}			0.3	V	V_{CC} = V_{TH} min, I_{SINK} = 1.2 mA, CD810R/S/T/Z

			0.4	V	V_{CC} = V_{TH} min, I_{SINK} = 3.2 mA, CD810L/M/J
RESET OUTPUT VOLTAGE HIGH (CD810X)					
V_{OH}	0.8V_{CC}			V	1.8 V < V_{CC} < V_{TH} min, I_{SOURCE} = 150 µA
$\overline{\text{RESET}}$ OPEN-DRAIN OUTPUT (CD803X)					
Leakage Current			1	µA	V_{CC} > V_{TH}, $\overline{\text{RESET}}$ deasserted

Absolute Maximum Ratings

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Ratings
V_{CC}	−0.3 V to +6 V
RESET, $\overline{\text{RESET}}$ (Push-Pull)	−0.3V to VCC+0.5V
RESET (Open-Drain)	−0.3 V to +6.0 V
Input Current(V_{CC})	20mA
Output Current(RESET, $\overline{\text{RESET}}$)	20mA
Rate of Rise, V_{CC}	100 V/µs
θ_{JA} Thermal Impedance	146°C/W(SC70)
	270°C/W(SOT-23)
Lead Temperature (Soldering,10 sec)	300℃
Vapor Phase (60 sec)	215℃
Infrared (15 sec)	220℃
Storage Temperature Range	-65℃ to +150℃

Table 3.Reset Threshold Options

RESET Model	Threshold(V)
CD803L/CD809L/CD810L	4.63
CD803M/CD809M/CD810M	4.38
CD809J/CD810J	4.00
CD803T/CD809T/CD810T	3.08
CD803S/CD809S/CD810S	2.93

CD803R/CD809R/CD810R	2.63
CD803Z/CD809Z/CD810Z	2.32

Pin Configurations And Function Descriptions

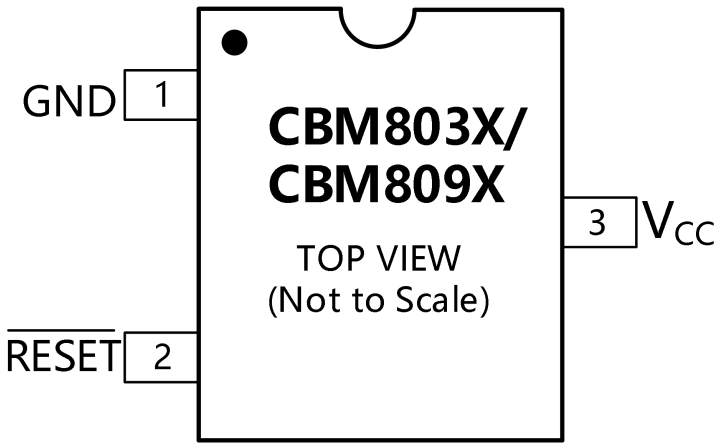


Figure 3. CD803X/CD809X

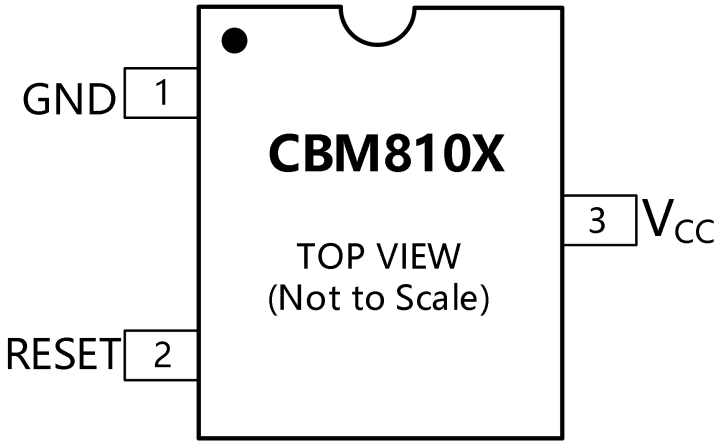


Figure 4. CD810X

Table4. Pin Function Descriptions

Pin No.		Mnemonic	Description
CD803X/CD809X	CD810X		
1	1	GND	Ground Reference for All Signals; 0 V.
N/A	2	RESET	Active High Logic Output. RESET remains high while V_{CC} is below the reset threshold and remains high for 240ms (typical) after V_{CC} rises above the reset threshold.
2	N/A	$\overline{RESET}$	Active Low Logic Output. RESET remains low while V_{CC} is below the reset threshold and remains low for 240ms

			(typical) after V_{CC} rises above the reset threshold.
3	3	V_{CC}	Supply Voltage Being Monitored.

Typical Characteristics

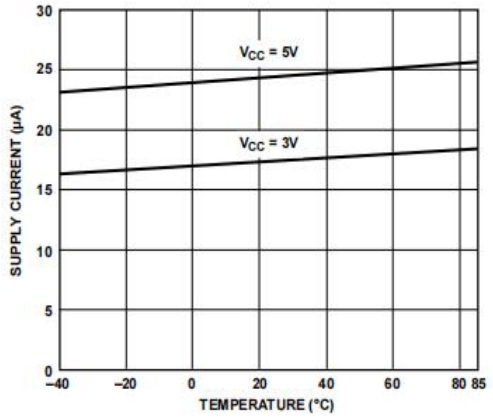


Figure 5. Supply Current vs. Temperature (No Load)

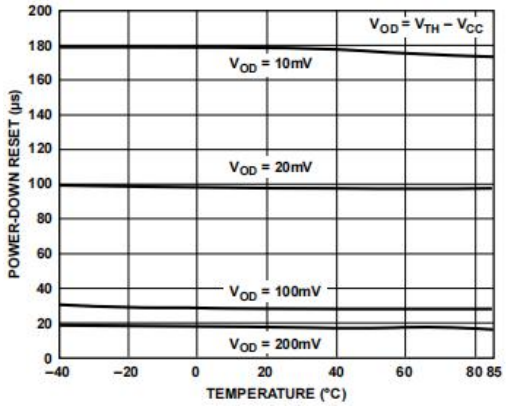


Figure 6. Power-Down Reset Delay vs. Temperature, CD8xxL/M/J

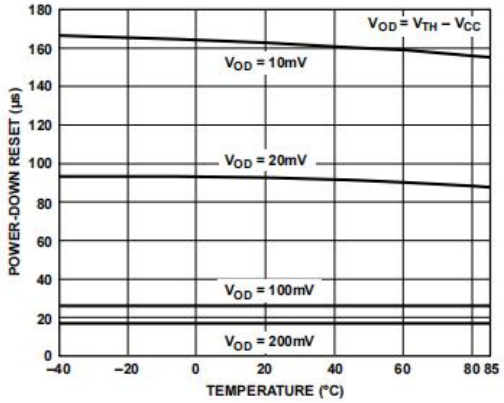


Figure 7. Power-Down Reset Delay vs. Temperature, CD8xxT/S/R/Z

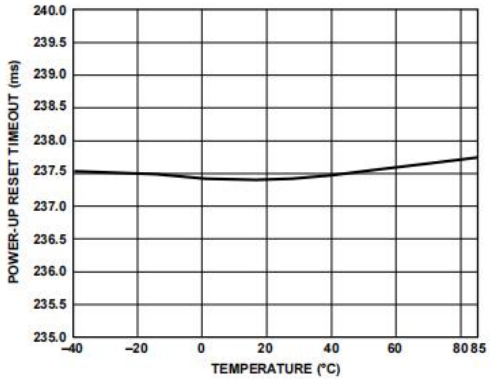


Figure 8. Power-Up Reset Timeout vs. Temperature, CD8xxR

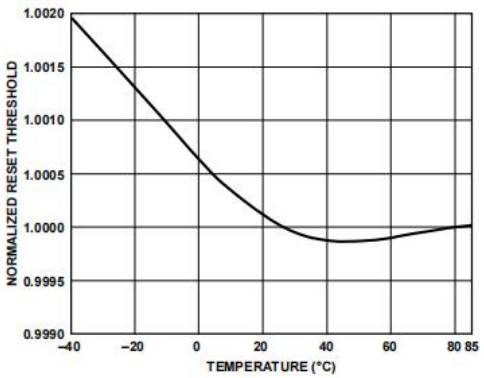


Figure 9. Normalized Reset Voltage Threshold vs. Temperature

Applications Information

The CD803X/CD809X/CD810X series is designed to integrate with as many devices as possible and, therefore, has a standard output dependent on VCC. This enables the parts to be used in both 3 V and 5 V, or any nominal voltage within the minimum and maximum specifications for V_{CC}. This design simplifies interfacing the CD803X/CD809X/CD810X to other devices.

- **Ensuring A Valid Reset Output Down To VCC=0**

When V_{CC} falls below 0.8 V, the CD803X/CD809X RESET no longer sinks current. A high impedance CMOS logic input connected to RESET may, therefore, drift to undetermined logic levels. To eliminate this problem, a 100 kΩ resistor should be connected from RESET to ground.

- **Benefits Of An Accurate Reset Threshold**

In other microprocessors, tolerances in supply voltages lead to an overall increase in reset tolerance levels due to the deterioration of the reset circuit' s power supply. In the CD803X/CD809X/CD810X, the possibility of a malfunction during a power failure is greatly reduced because the devices can operate effectively even when there are large degradations of the supply voltages. Another advantage is the very accurate internal voltage reference circuit of the CD803X/CD809X/CD810X. These benefits combine to produce an exceptionally reliable voltage monitor circuit.

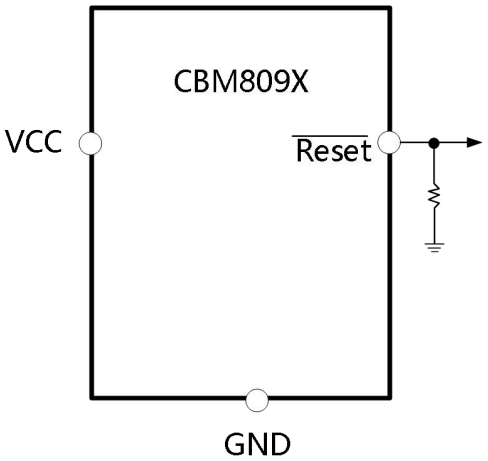
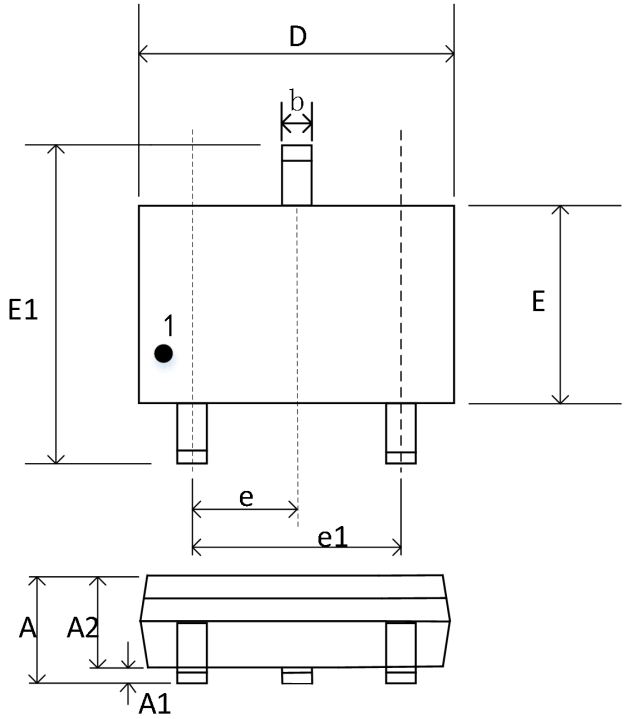


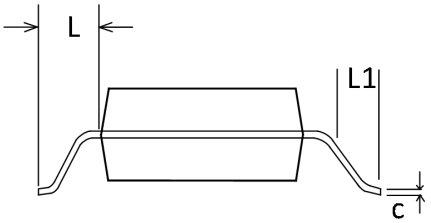
Figure 10. Ensuring a Valid Reset Output Down to VCC = 0 V

Package Outline Dimensions

SOT23-3

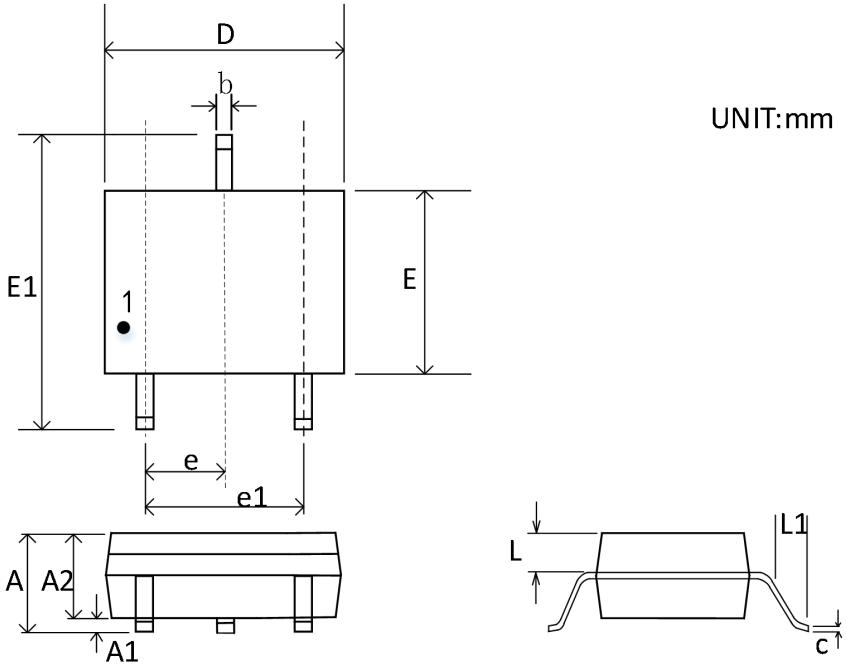


UNIT:mm



Symbol	Dimensions In Millimeters	
	Min	Max
A	0.89	1.12
A1	0.013	0.10
A2	0.88	1.02
b	0.37	0.51
c	0.085	0.180
D	2.80	3.04
E	1.20	1.40
E1	2.10	2.64
e	0.89	1.03
L	0.54REF	
L1	0.30	0.60

SC70-3



UNIT:mm

Symbol	Dimensions In Millimeters	
	Min	Max
A	0.80	1.10
A1	0.10MAX	
A2	0.80	1.00
b	0.25	0.40
c	0.10	0.26
D	1.80	2.20
E	1.15	1.35
E1	1.80	2.40
e	0.65BSC	
L	0.10	0.40
L1	0.10	0.30

Chinese version:CD803_CD809_CD810

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD803LSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD803MSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD803RSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD803SSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD803TSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD803ZSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD809JSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD809JST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD809LSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD809LST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD809MSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD809MST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD809RSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD809RST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD809SSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD809SST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD809TSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD809TST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD809ZSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD809ZST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD810JSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD810JST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD810LSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD810LST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD810MSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD810MST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000

CD810RSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD810RST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD810SSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD810SST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD810TSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD810TST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000
CD810ZSC3	-40℃~85℃	SC70-3	Tape and Reel, 3000
CD810ZST3	-40℃~85℃	SOT23-3	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.3	Initial version	Regular update	WW	LYL	