CoreadDvices
承芯微电子

# CD811_CD812

Microprocessor Supervisory Circuit

Version: Rev 1.0.0 Date: 2025-6-3

## Features

- Precision voltage monitor: 2.32 V(CD811Z/812Z) / 2.63 V (CD811R/812R) / 2.93 V (CD811S/812S) /3.08 V (CD811T/812T) / 4.38 V (CD811M/812M) / 4.63 V (CD811L/812L)
- Low power consumption: 5μA typical
- Reset assertion down to 1 VCC
- Power-on reset: 140 ms minimum
- Logic low $\overline{\text{RESET}}$ output (CD811)
- Logic high RESET output (CD812)
- Built-in manual reset

## Application

- Microprocessor systems
- Controllers
- Intelligent instruments
- Automotive systems
- Safety systems
- Portable instruments

## Description

The CD811/CD812 are reliable voltage monitoring devices suitable for use in most voltage monitoring applications. The CD811/CD812 are designed to monitor six different voltages.These voltages have been selected for the effective monitoring of 2.5 V, 3 V, 3.3 V, and 5 V supply voltage levels.

Included in this circuit is a debounced manual reset input. Reset can be activated using an electrical switch (or an input from another digital device) or by a degradation of the supply voltage. The manual reset function is very useful, especially if the circuit in which the CD811/CD812 are operating enters into a state that can only be detected by the user. Allowing the user to reset a system manually can reduce the damage or danger that could otherwise be caused by an out-of-control or locked system.



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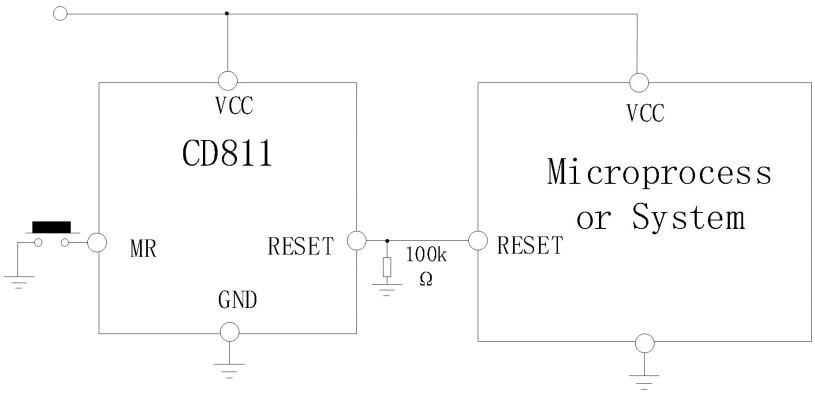
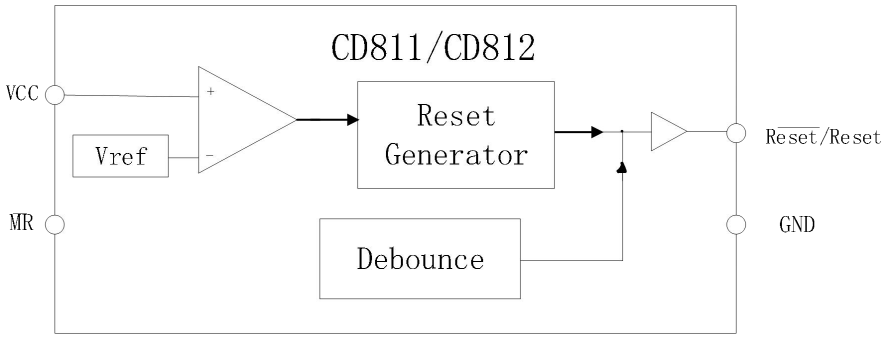


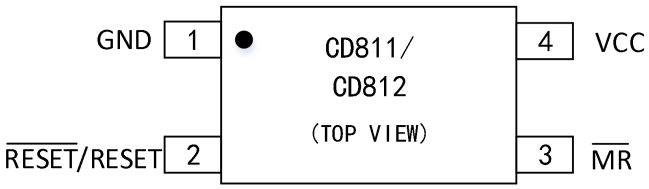

**Typical CD811 Operating Circuit**




**Functional Block Diagram**

# Contents

## Pin Configurations




**CD811/CD812 Pin Configuration**

### Pin Decscrition

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | GND | Ground Reference,0V |
| 2 | $\overline{\text{RESET}}$ | Active Low Logic Output. |
| | RESET | Active High Logic Output. |
| 3 | $\overline{\text{MR}}$ | Manual Reset. |
| 4 | $V_{CC}$ | Monitored Supply Voltage of 2.5 V, 3 V, 3.3 V, or 5 V. |

## Absolute Maximum Ratings

| Parameter | Range |
|---|---|
| Terminal Voltage (With Respect to Ground)$V_{CC}$ | −0.3 V to +6 V |
| All Other Inputs | −0.3 V to $V_{CC}$ + 0.3 V |
| $V_{CC}$ Input Current | 20 mA |
| $\overline{\text{MR}}$ Input Current | 20 mA |
| RESET Output Current | 20 mA |
| Power Dissipation ($T_A$ = 70°C)(SOT-143) | 200 mW |
| $\theta_{JA}$ Thermal Impedance | 330°C/W<br>4mW/°C（@70°C以上) |
| Storage Temperature Range | −65℃ to +160℃ |
| Operating Temperature Range | −40℃ to +85℃ |
| Lead Temperature (Soldering, 10 sec) | 300℃ |
| Vapor Phase(60s) | 215°C |
| Infrared (15s) | 220°C |
| ESD Rating | 3 kV |

## Electrical characteristics

(VCC = full operating range; TA = TMIN to TMAX; VCC typical = 5 V for L/M models, 3.3 V for T/S models, 3 V for R model, 2.5 V for Z models, unless otherwise noted.)

| PARAMETER | CONDITION | CD811/CD812 | | | |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | UNIT |
| **Supply** | | | | | |
| Voltage | | 1.0 | -- | 5.5 | V |
| Current | | -- | 8 | 15 | μA |
| **Reset Voltage Threshold** | | | | | |
| CD811L/CD812L | $T_A$ = 25°C | 4.54 | 4.63 | 4.72 | V |
| CD811L/CD812L | $T_A$ = −40°C to +85°C | 4.50 | -- | 4.75 | V |
| CD811M/CD812M | $T_A$ = 25°C | 4.30 | 4.38 | 4.46 | V |
| CD811M/CD812M | $T_A$ = −40°C to +85°C | 4.25 | -- | 4.50 | V |
| CD811T/CD812T | $T_A$ = 25°C | 3.03 | 3.08 | 3.14 | V |
| CD811T/CD812T | $T_A$ = −40°C to +85°C | 3.00 | -- | 3.15 | V |
| CD811S/CD812S | $T_A$ = 25°C | 2.88 | 2.93 | 2.98 | V |
| CD811S/CD812S | $T_A$ = −40°C to +85°C | 2.85 | -- | 3.00 | V |
| CD811R/CD812R | $T_A$ = 25°C | 2.58 | 2.63 | 2.68 | V |
| CD811R/CD812R | $T_A$ = −40°C to +85°C | 2.55 | -- | 2.70 | V |
| CD811Z/CD812Z | $T_A$ = 25°C | 2.28 | 2.32 | 2.35 | V |
| CD811Z/CD812Z | $T_A$ = −40°C to +85°C | 2.25 | -- | 2.38 | V |
| **RESET ACTIVE TIMEOUT PERIOD** | $V_{CC}$=$V_{TH(MAX)}$ | 140 | -- | 560 | ms |
| **Manual Reset** | | | | | |
| Minimum Pulse Width | | 10 | -- | -- | μs |
| Glitch Immunity | | -- | 100 | -- | ns |
| RESET/RESET Propagation Delay | | -- | 0.5 | -- | μs |
| Pull-Up Resistance | | 10 | 20 | 30 | kΩ |
| Reset Threshold Temperature Coefficient | | -- | 30 | -- | ppm/℃ |
| An Input Rising Above | $V_{CC}$ > $V_{TH(MAX)}$, CD811L/CD812L/CD811M/CD812M | 2.3 | -- | -- | V |
| An Input Falling Below | $V_{CC}$ > $V_{TH(MAX)}$, CD811L/CD812L/CD811M/CD812M | -- | -- | 0.8 | V |
| An Input Rising Above | $V_{CC}$ > $V_{TH(MAX)}$, CD811R/CD812R/CD811S/CD812S/ CD811T/CD812T/CD811Z/CD812Z | 0.7*$V_{CC}$ | -- | -- | V |
| An Input Falling Below | $V_{CC}$ > $V_{TH(MAX)}$, CD811R/CD812R/CD811S/CD812S/ | -- | -- | 0.25*$V_{CC}$ | V |



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| | | | | | |
|---|---|---|---|---|---|
| | CD811T/CD812T/CD811Z/CD812Z | | | | |
| $V_{CC}$ To Reset/Reset Delay | | -- | 40 | -- | μs |
| Reset Active Timeout Period | | 140 | -- | 560 | ms |
| **RESET/RESET Output Voltage** | | | | | |
| Low Voltage Output | $V_{CC}$ = $V_{TH(MAX)}$, $I_{SINK}$ = 1.2 mA(CD812R/CD812S/CD812T/CD812Z) | -- | -- | 0.3 | V |
| | $V_{CC}$ = $V_{TH(MAX)}$, $I_{SINK}$ = 3.2 mA(CD812L/CD812M) | -- | -- | 0.4 | V |
| | $V_{CC}$ = $V_{TH(MIN)}$, $I_{SINK}$ = 1.2 mA(CD811R/CD811S/CD811T/CD811Z) | -- | -- | 0.3 | V |
| | $V_{CC}$ = $V_{TH(MIN)}$, $I_{SINK}$ = 3.2 mA(CD811L/CD811M) | -- | -- | 0.4 | V |
| | $V_{CC}$ > 1.0 V, $I_{SINK}$ = 50 μA(CD811R/CD811S/CD811T/CD811Z/ CD811L/CD811M) | -- | -- | 0.3 | V |
| High Voltage Output | 1.8 V < $V_{CC}$ < $V_{TH(MIN)}$, $I_{SOURCE}$ = 150 μA (CD812R/CD812S/CD812T/CD812Z/ CD812L/ CD812M) | 0.8x$V_{CC}$ | -- | -- | V |
| | $V_{CC}$ > $V_{TH(MAX)}$, $I_{SOURCE}$ = 500 μA(CD811R/CD811S/CD811T/CD811Z) | 0.8x$V_{CC}$ | -- | -- | V |
| | $V_{CC}$ > $V_{TH(MAX)}$, $I_{SOURCE}$ = 800 μA(CD811L/CD811M) | $V_{CC}$ – 1.5 | -- | -- | V |

## Typical Characteristics

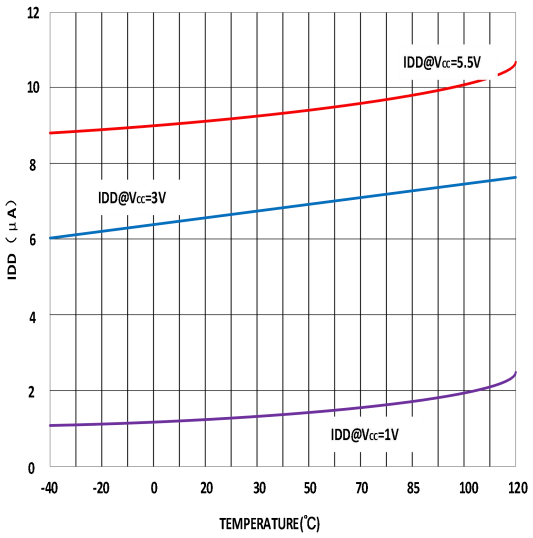


Figure1. Supply Current vs. Temperature

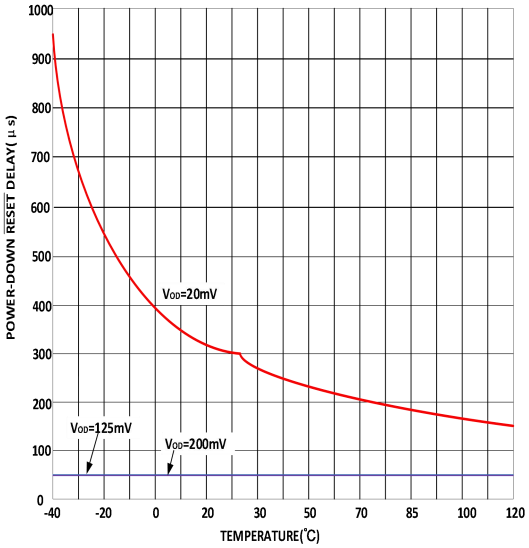


Figure2. Power-Down RESET Delay vs. Temperature

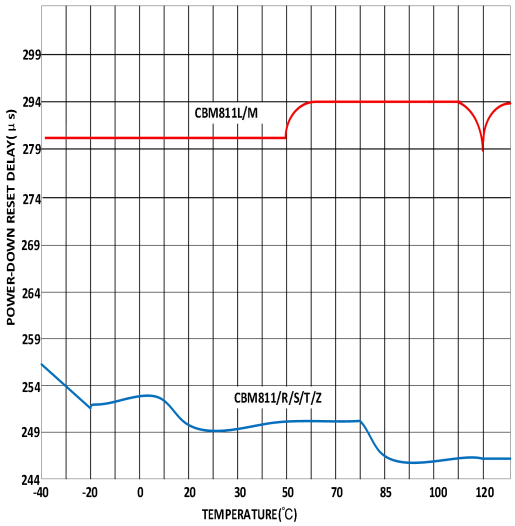


Figure3. Power-Up RESET Timeout vs. Temperature

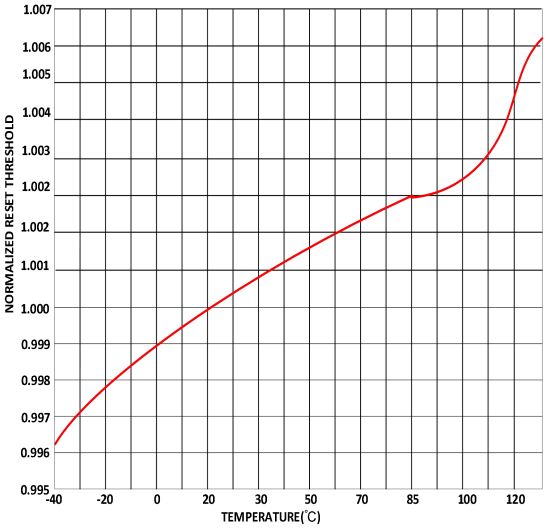


Figure4. RESET Threshold Deviation vs. Temperature



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## Applications Information

A reset output is provided to the microprocessor whenever the VCC input is below the reset threshold. The actual reset thresholddepends on whether an L, M, T, S, R, or Z suffix is used as follows:

| Model Reset | Threshold (V) |
|---|---|
| CD811L | 4.63 |
| CD811M | 4.38 |
| CD811T | 3.08 |
| CD811-3T | 3.08 |
| CD811S | 2.93 |
| CD811R | 2.63 |
| CD811Z | 2.32 |
| CD812L | 4.63 |
| CD812M | 4.38 |
| CD812T | 3.08 |
| CD812S | 2.93 |
| CD812R | 2.63 |
| CD812Z | 2.32 |

## Reset Output

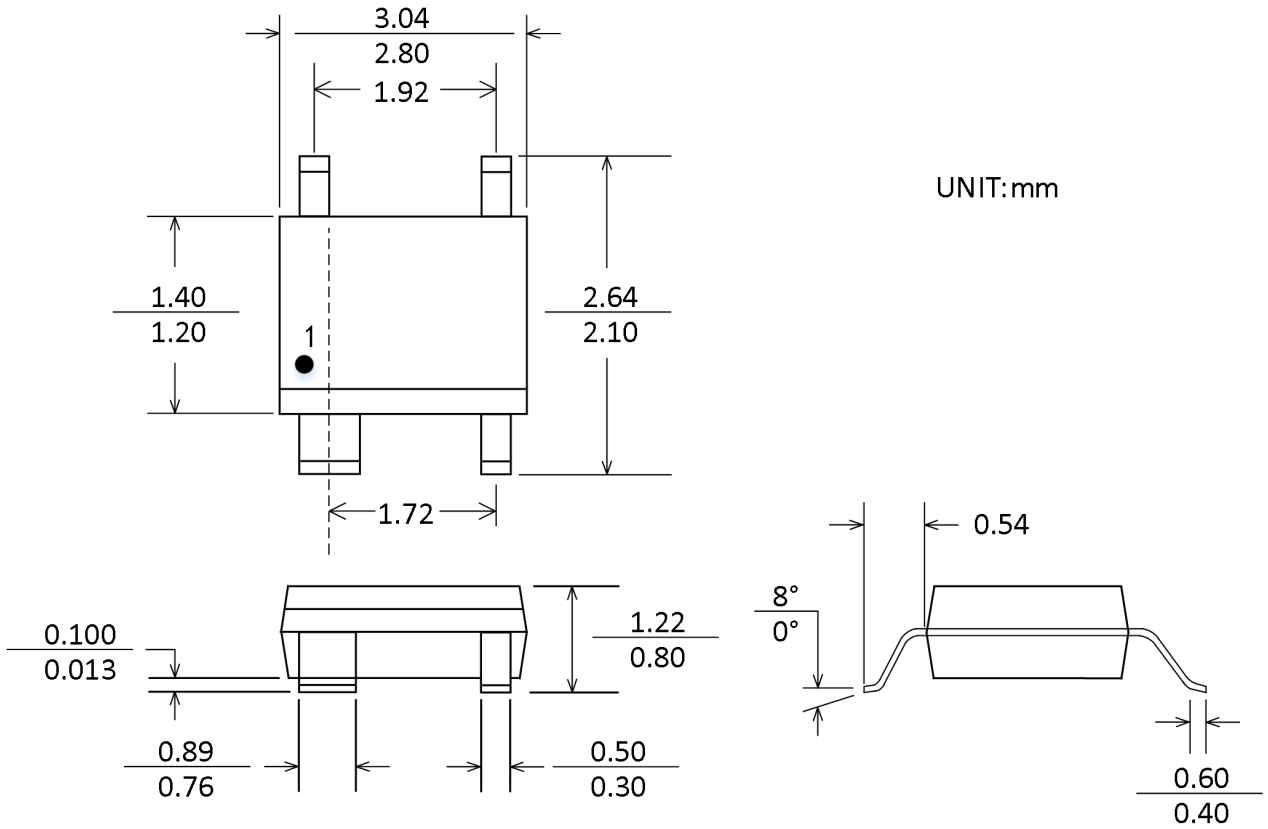
On power-up and after VCC rises above the reset threshold, an internal timer holds the reset output active for 240 ms (typical).This is intended as a power-on reset signal for the processor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset output is similarly activated and remains active for 240 ms (typical) after the supply recovers. This allows time for the power supply and microprocessor to stabilize.The CD811 provides an active low reset output (RESET) while the CD812 provides an active high output (RESET).During power-down of the CD811, the RESET output remains valid (low) with VCC as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the supply falls and also ensures that no spurious activity can occur via the microprocessor as it powers up.

## Manual Reset

The CD811/CD812 are equipped with a manual reset input. This input is designed to operate in a noisy environment where unwanted glitches could be induced. These glitches could be produced by the bouncing action of a switch contact, or where a manual reset switch may be located some distance away from the circuit (the cabling of which can pick up noise).The manual reset input is guaranteed to ignore logically valid inputs that are faster than 100 ns and to accept inputs longer induration than 10 µs.

## Package Outline Dimensions

**SOT143-4**



## Package/Ordering Information

| MODEL | TEMPERATURE | PACKAGE DESCRIPTION | PACKAGE OPTION |
|---|---|---|---|
| CD811LST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD811MST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD811TST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD811TST4-3.0 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD811SST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD811RST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD811ZST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD812LST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD812MST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD812TST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD812SST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD812RST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |
| CD812ZST4 | -40℃~85℃ | SOT143-4 | Tape and Reel, 3000 |

## Revision Log

| Version | Revision date | Change content | Reason for Change | Modified by | Reviewed By | Note |
|---|---|---|---|---|---|---|
| V1.0 | 2025.6.3 | Initial version | Regular update | WW | LYL | |



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