CoreadDvices
承芯微电子

CD9001

Embedded USB Host/Slave Controller

Version: Rev 1.0.0 Date: 2025-6-9

Features

- First USB Host/Slave controller for embedded systems in the market with a standard microprocessor bus interface
- Supports both full speed (12 Mbps) and low speed (1.5 Mbps) USB transfer in both master and slave modes
- Conforms to USB Specification 1.1 for full- and lowspeed
- Operates as a single USB host or slave under software control
- Automatic detection of either low- or full-speed devices
- 8-bit bidirectional data, port I/O(DMAsupportedinslavemode)
- On-chip SIE and USB transceivers
- On-chip single root HUB support
- 256-byte internal SRAM buffer
- Ping-pong buffers for improved performance
- Operates from 12 or 48 MHz crystal or oscillator (built-in DPLL)
- 5 V-tolerant interface
- Suspend/resume, wake up, and low-power modes are supported
- Auto-generation of SOF and CRC5/16
- Auto-address increment mode, saves memory READ/WRITE cycles
- Development kit including source code drivers is

Application

- Sensor applications
- Portable video devices
- Industrial cameras or video surveillance equipment
- Data collection system
- ATA interface, such as IDE hard drive
- Memory, card reader
- Scanner
- Laser engraving equipment
- Portable sound card or MP3 player device
- VGA video capture and transmission equipment, etc

- 3.3-V power source, 0.35 micron CMOS technology
- Available in 48-pin TQFP package

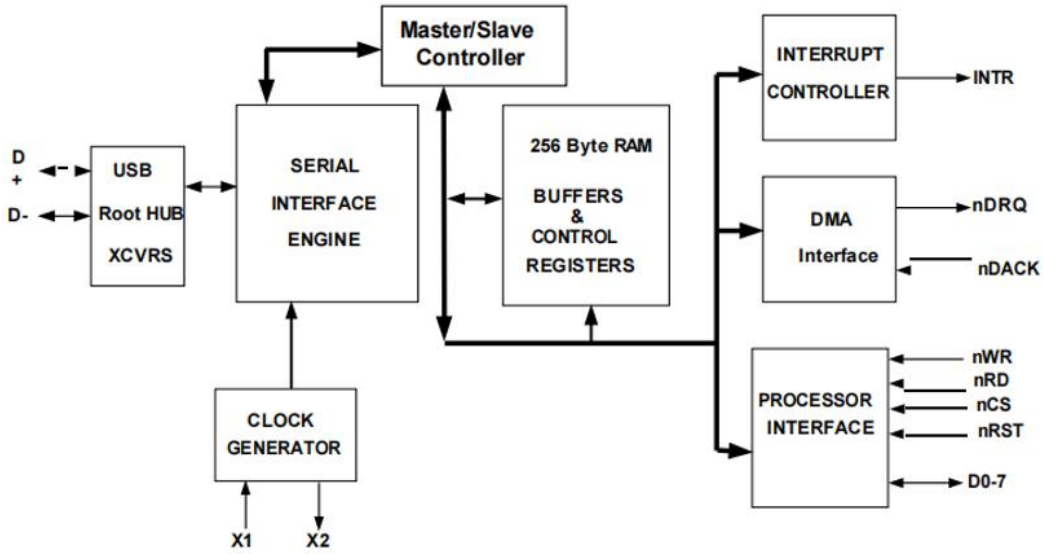
Description

The CD9001A is an Embedded USB Host/Slave Controller capable of communicating in either full speed or low speed. The CD9001A interfaces to devices such as microprocessors, micro-controllers, DSPs, or directly to a variety of buses such as ISA, PCMCIA, and others. The CD9001A USB Host Controller conforms to USB Specification 1.1. The CD9001A incorporates USB Serial Interface functionality along with internal full or low speed transceivers. The CD9001A supports and operates in USB full speed mode at 12 Mbps, or in low-speed mode at 1.5 Mbps. When in host mode, the CD9001A is the master and controls the USB bus and the devices that are connected to it. In peripheral mode, otherwise known as a slave device, the CD9001A operates as a variety of full- or low-speed devices.

The CD9001A data port and microprocessor interface provide an 8-bit data path I/O or DMA bidirectional, with interrupt support to allow easy interface to standard microprocessors or microcontrollers such as Motorola or Intel CPUs and many others. The CD9001A has 256 bytes of internal RAM, which is used for control registers and data buffers. The available Pb-free package is a 48-pin (CD9001A) package. All packages operate at 3.3 VDC. The I/O interface logic is 5 V-tolerant.

Contents

Logic Block Diagram



Pin Configurations

48-Pin TQFP Pin Layout

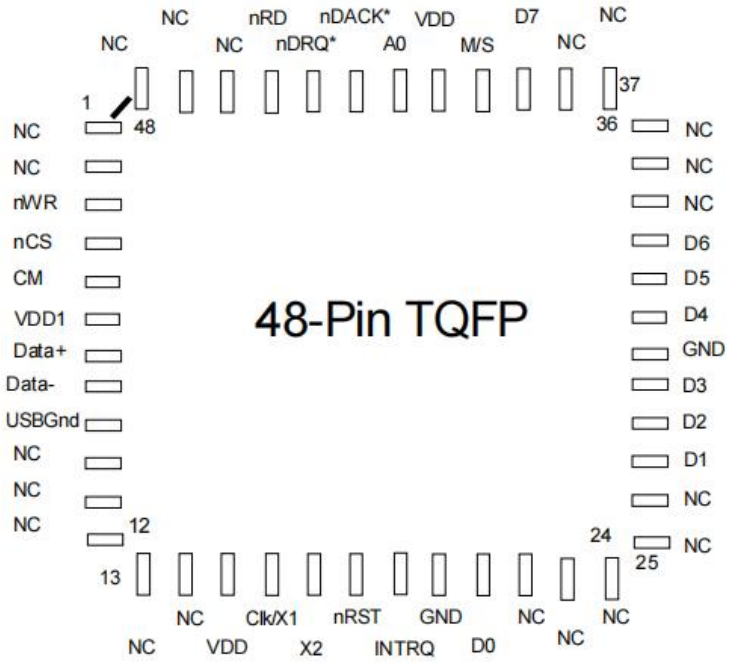


Figure 1. 48-pin TQFP USB Host/Slave Controller Pin Layout

Chinese version:CD9001

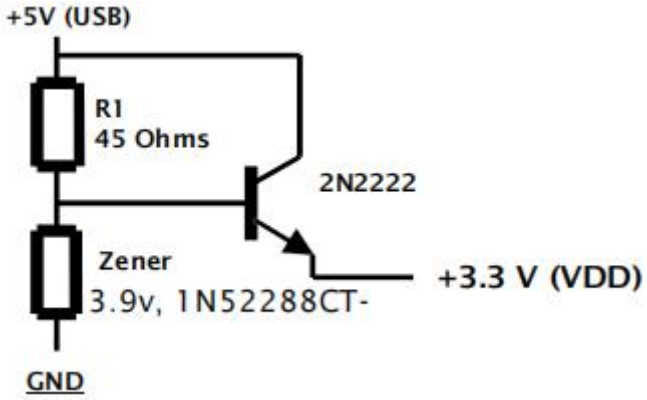


Figure 2. Sample VDD Generator

Note NC. Indicates No Connection. NC Pins must be left unconnected.

USB Host Controller Pins Description

The CD9001A is packaged in a 48-pin TQFP. These devices require a 3.3 VDC power source and an external 12 or 48 MHz crystal or clock.

Table 34. Pin and Signal Description for Pins

Pin NO	Pin Type	Pin Name	Pin Description
1	NC	NC	No connection.
2	NC	NC	No connection.
3	IN	nWR	Write Strobe Input. An active LOW input used with nCS to write to registers/data memory.
4	IN	nCS	Active LOW 48-Pin TQFP Chip select. Used with nRD and nWr when accessing the 48-Pin TQFP.
5	IN	CM	Clock Multiply. Select 12 MHz/48 MHz Clock Source.
6	VDD1	+3.3V DC	Power for USB Transceivers. VDD1 may be connected to VDD.
7	BIDIR	DATA+	USB Differential Data Signal HIGH Side.
8	BIDIR	DATA-	USB Differential Data Signal LOW Side.
9	GND	USB GND	Ground Connection for USB.
10	NC	NC	No connection.
11	NC	NC	No connection.
12	NC	NC	No connection.
13	NC	NC	No connection.
14	NC	NC	No connection.

15	VDD	+3.3V DC	Device VDD Power.
16	IN	CLK/X1	Clock orExternal Crystal X1 connection. TheX1/X2 Clock requires external 12 or 48 MHz matching crystal or clock source.
17	OUT	X2	External Crystal X2 connection.
18	IN	nRST	Device active low reset input.
19	OUT	INTRQ	Active HIGH Interrupt Request output to external controller.
20	GND	GND	Device Ground.
21	BIDIR	D0	Data 0. Microprocessor Data/Address Bus.
22	NC	NC	No connection.
23	NC	NC	No connection.
24	NC	NC	No connection.
25	NC	NC	No connection.
26	NC	NC	No connection.
27	BIDIR	D1	Data 1. Microprocessor Data/Address Bus.
28	BIDIR	D2	Data 2. Microprocessor Data/Address Bus.
29	BIDIR	D3	Data 3. Microprocessor Data/Address Bus.
30	GND	GND	Device Ground.
31	BIDIR	D4	Data 4. Microprocessor Data/Address Bus.
32	BIDIR	D5	Data 5. Microprocessor Data/Address Bus.
33	BIDIR	D6	Data 6. Microprocessor Data/Address Bus.
34	NC	NC	No connection.
35	NC	NC	No connection.
36	NC	NC	No connection.
37	NC	NC	No connection.
38	NC	NC	No connection.
39	BIDIR	D7	Data 7. Microprocessor Data/Address Bus.
40	IN	M/S	Master/Slave Mode Select. ‘1’ selects Slave. ‘0’ = Master.
41	VDD	+3.3V DC	Device VDD Power.
42	IN	A0	A0 = ‘0’. Selects address pointer. Register A0 = ‘1’. Selects data buffer or register.
43	IN	nDACK	DMA Acknowledge. An active LOW input used to interface to an

			external DMA controller. DMA is enabled only in slave mode. In host mode, the pin should be tied HIGH (logic ‘1’).
44	OUT	nDRQ	DMA Request. An active LOW output used withan external DMA controller. nDRQ and nDACK form the handshake for DMA data transfers. In host mode, leave the pin unconnected.
45	IN	nRD	Read Strobe Input. An active LOW input used with nCS to read registers/data memory.
46	NC	NC	No connection.
47	NC	NC	No connection.
48	NC	NC	No connection.

Absolute Maximum Ratings

This section lists the absolutemaximum ratings of the CD9001A. Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Description	Condition
Storage Temperature	–40 °C to 125 °C
Voltage on any pin with respect to ground	–0.3 V to 6.0 V
Power Supply Voltage (VDD)	4.0 V
Power Supply Voltage (VDD1)	4.0 V
Lead Temperature (10 seconds)	180°C

Recommended Operating Conditions

Parameter	Min	Typical	Max
Power Supply Voltage, VDD	3.0V	3.3V	3.45V
Power Supply Voltage, VDD1	3.0V	--	3.45V
Operating Temperature	0℃	--	65℃
(Crystal Requirements, (X1, X2)	Min	Typical	Max
Operating Temperature Range	0℃		65℃
Parallel Resonant Frequency		48MHz	
Frequency Drift over Temperature			±50 ppm

Accuracy of Adjustment			±30 ppm
Series Resistance			100 Ohms
Shunt Capacitance	3 pF		6 pF
Load Capacitance		20 pF	
Drive Level	20μW		5mW
Mode of Vibration Third Overtone[5]			

External Clock Input Characteristics (X1)

Parameter	Min	Typical	Max
Clock Input Voltage at X1 (X2 Open)	1.5V		
Clock Frequency[6]		48MHz	

Notes

5. Fundamental mode for 12 MHz Crystal.

6. The CD9001A can use a 12 MHz Clock Source.

DC Characteristics

Parameter	Description	Min	Typical	Max
V_{IL}	Input Voltage LOW	-0.3V		0.8V
V_{IH}	Input Voltage HIGH (5 V Tolerant I/O)	2.0V		6.0V
V_{OL}	Output Voltage LOW (IOL = 4 mA)			0.4V
V_{OH}	Output Voltage HIGH (IOH = –4 mA)	2.4V		
I_{OH}	Output Current HIGH	4mA		
I_{OL}	Output Current LOW	4mA		
I_{LL}	Input Leakage			±1μA
C_{IN}	Input Capacitance			10pF
I_{CC} (7)	Supply Current (VDD) inc USB at FS		21mA	25mA
I_{CCSUS1} (8)	Supply Current (VDD) Suspend w/Clk & Pll Enb		4.2mA	5mA
I_{CCSUS2} (9)	Supply Current (VDD) Suspend no Clk & Pll Dis		50μA	60μA
I_{USB}	Supply Current (VDD1)			10mA
I_{USBSUS}	Transceiver Supply Current in Suspend			10μA

USB Host Transceiver Characteristics

Parameter	Description	Min	Typical	Max
V_{IHYS}	Differential Input Sensitivity (Data+, Data–)	0.2V	--	200mV
V_{USBIH}	USB Input Voltage HIGH Driven	2.0V	--	--
V_{USBIL}	USB Input Voltage LOW	0.8V	--	--
V_{USBOH}	USB Output Voltage HIGH	2.0V	--	--
V_{USBOL}	USB Output Voltage LOW	0.0V	--	0.3V
Z_{USBH} (11)	Output Impedance HIGH STATE	36Ω	--	42Ω
Z_{USBL} (11)	Output Impedance LOW STATE	36Ω	--	42Ω
I_{USB}	Transceiver Supply p-p Current (3.3 V)	--	--	10 mA (在全速下)

Every VDD pin, including USB VDD, must have a decoupling capacitor to ensure clean VDD (free of high frequency noise) at the chip input point (pin) itself.

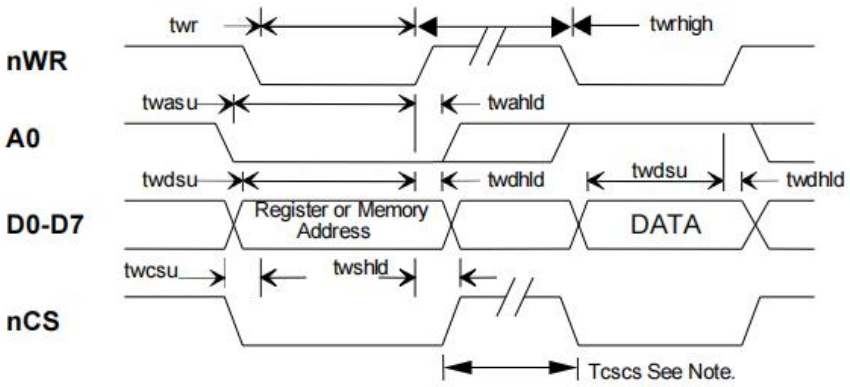
The best way to do this is to connect a ceramic capacitor (0.1 µF, 6 V) between the pin itself and a good ground. Keep capacitor leads as short as possible. Use surface mount capacitors with the shortest traces possible (the use of a ground plane is strongly recom mended).

Notes

7. ICC measurement includes USB Transceiver current (IUSB) operating at full speed.
8. ICCsus1 measured with 12 MHz Clock Input and Internal PLL enabled. Suspend set –(USB transceiver and internal Clocking disabled).
9. ICCsus2 measured with external Clock, PLL disabled, and Suspend set. For absolute minimum current consumption, ensure that all inputs to the device are at
static logic level.
10. All typical values are VDD = 3.3 V and TAMB= 25°C.
11. ZUSBX impedance values includes an external resistor of 24 Ohms ± 1% (CD9001A revision 1.2 requires external resistor values of 33 Ohms ±1%).

Bus Interface Timing Requirements

I/O Write Cycle

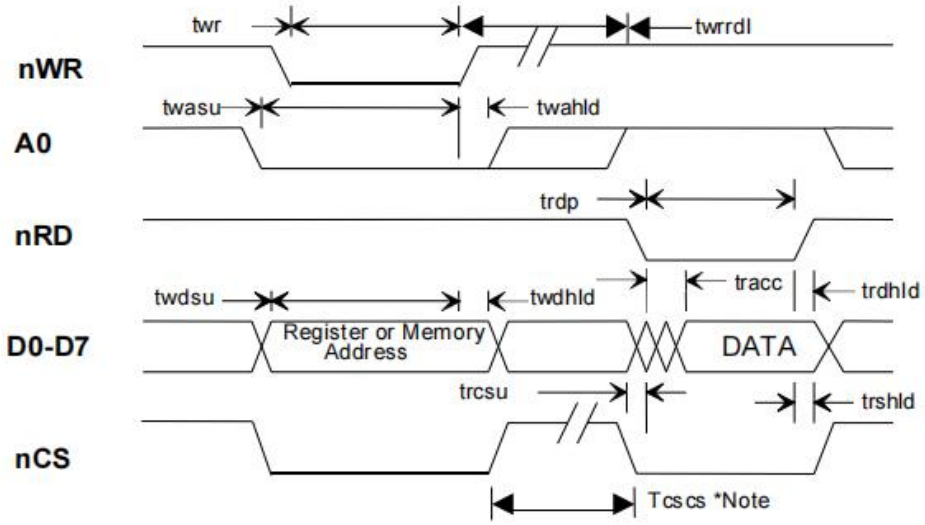


I/O Write Cycle to Register or Memory Buffer

Parameter	Description	Min	Typical	Max
t_{WR}	Write pulse width	85ns	--	--
t_{WCSU}	Chip select set-up to nWR LOW	0ns	--	--
t_{WSHLD}	Chip select hold time After nWR HIGH	0ns	--	--
t_{WASU}	A0 address setup time	85ns	--	--
t_{WAHLD}	A0 address hold time	10ns	--	--
t_{WDSU}	Data to Write HIGH set-up time	85ns	--	--
t_{WDHLD}	Data hold time after Write HIGH	5ns	--	--
t_{CSCS}	nCS inactive to nCS* asserted	85ns	--	--
t_{WRHIGH}	NWR HIGH	85ns	--	--

Note: nCS an be held LOW for multiple Write cycles provided nWR is cycled. Write Cycle Time for Auto Inc Mode Writes is 170 ns
minimum.

I/O Read Cycle

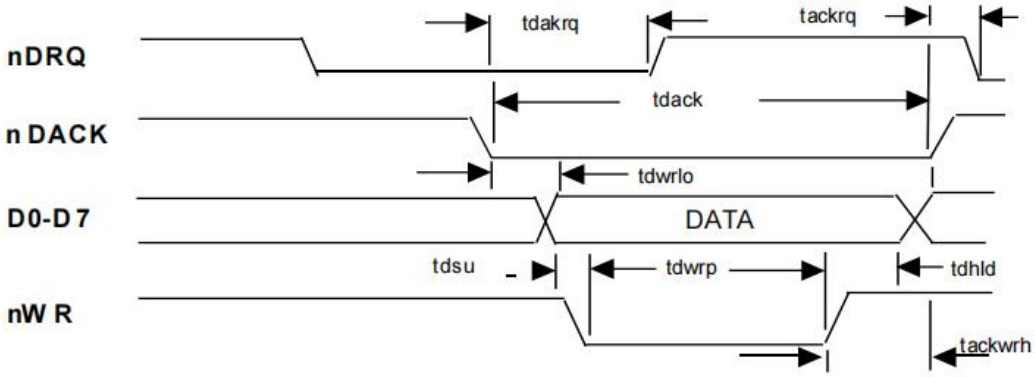


I/O Read Cycle from Register or Memory Buffer

Parameter	Description	Min	Typical	Max
t_{WR}	Write pulse width	85ns	--	--
t_{RD}	Read pulse width	85ns	--	--
t_{WCSU}	Chip select set-up to nWR	0ns	--	--
t_{WASU}	A0 address set-up time	85ns	--	--
t_{WAHLD}	A0 address hold time	10ns	--	--
t_{WDSU}	Data to Write HIGH set-up time	85ns	--	--
t_{WDHLD}	Data hold time after Write HIGH	5ns	--	--
t_{RACC}	Data valid after Read LOW	25ns	--	--
t_{RDHLD}	Data hold after Read HIGH	40ns	--	--
t_{RCSU}	Chip select LOW to Read LOW	0ns	--	--
t_{RSHLD}	NCS hold after Read HIGH	0ns	--	--
t_{CSCS}	nCS inactive to nCS *asserted	85ns	--	--
t_{WRRDL}	nWR HIGH to nRD LOW	85ns	--	--

Note: nCS can be kept LOW during multiple Read cycles provided nRD is cycled. Rd Cycle Time for Auto Inc Mode Reads is 170 ns minimum.

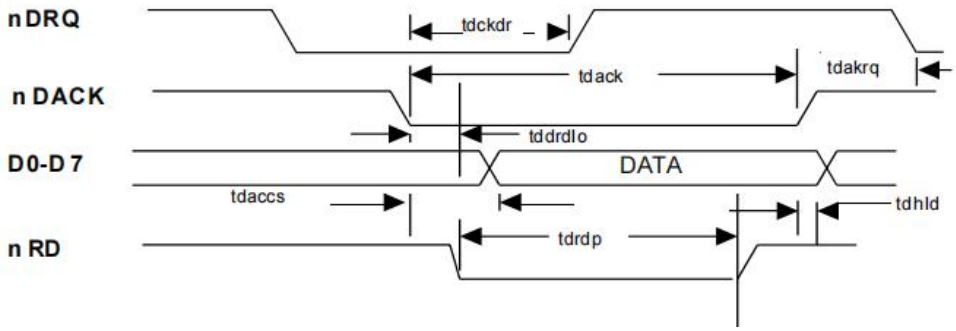
DMA Write Cycle



Parameter	Description	Min	Typical	Max
t_{DACK}	nDACK low	80ns	--	--
t_{DWRLO}	nDACK to nWR low delay	5ns	--	--
t_{DAKRQ}	nDACK low to nDRQ high delay	5ns	--	--
t_{DWRP}	nWR pulse width	65ns	--	--
t_{DHLD}	Data hold after nWR high	5ns	--	--
t_{DSU}	Data set-up to nWR strobe low	60ns	--	--
t_{ACKRQ}	NDACK high to nDRQ low	5ns	--	--
t_{ACKWRH}	NDACK high to nDRQ low	5ns	--	--
$t_{WRCYCLE}$	DMA Write Cycle Time	150ns	--	--

Note nWR must go low after nDACK goes low in order for nDRQ to clear. If this sequence is not implemented as requested, the next nDRQ is not inserted.

DMA Read Cycle

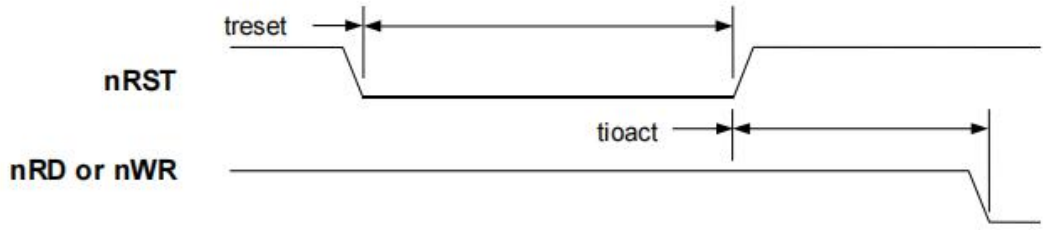


Parameter	Description	Min	Typical	Max
t_{DACK}	nDACK low	100ns	--	--
t_{DDRDLO}	nDACK to nRD low delay	0ns	--	--

t_{DCKDR}	nDACK low to nDRQ high delay	5ns	--	--
t_{DRDP}	nRD pulse width	90ns	--	--
t_{DHLD}	Date hold after nDACK high	5ns	--	--
t_{DDACCS}	Data access from nDACK low	85ns	--	--
t_{DRDACK}	nRD high to nDACK high	0ns	--	--
t_{DAKRQ}	nDRQ low after nDACK high	5ns	--	--
$t_{RDCYCLE}$	DMA Read Cycle Time	150ns	--	--

Note: Data is held until nDACK goes high regardless of state of nREAD.

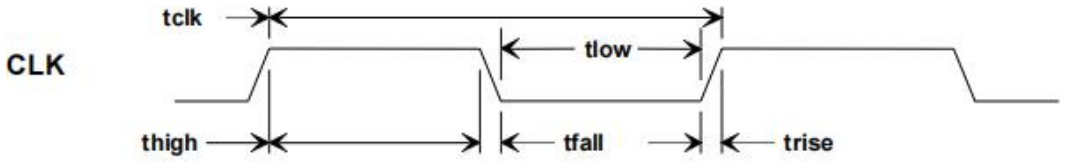
Reset Timing



Parameter	Description	Min	Typical	Max
t_{RESET}	nRst Pulse width	16 clocks	--	--
t_{IOACT}	从 nRst 高到 nRD 或 nWR 激活	16 clocks	--	--

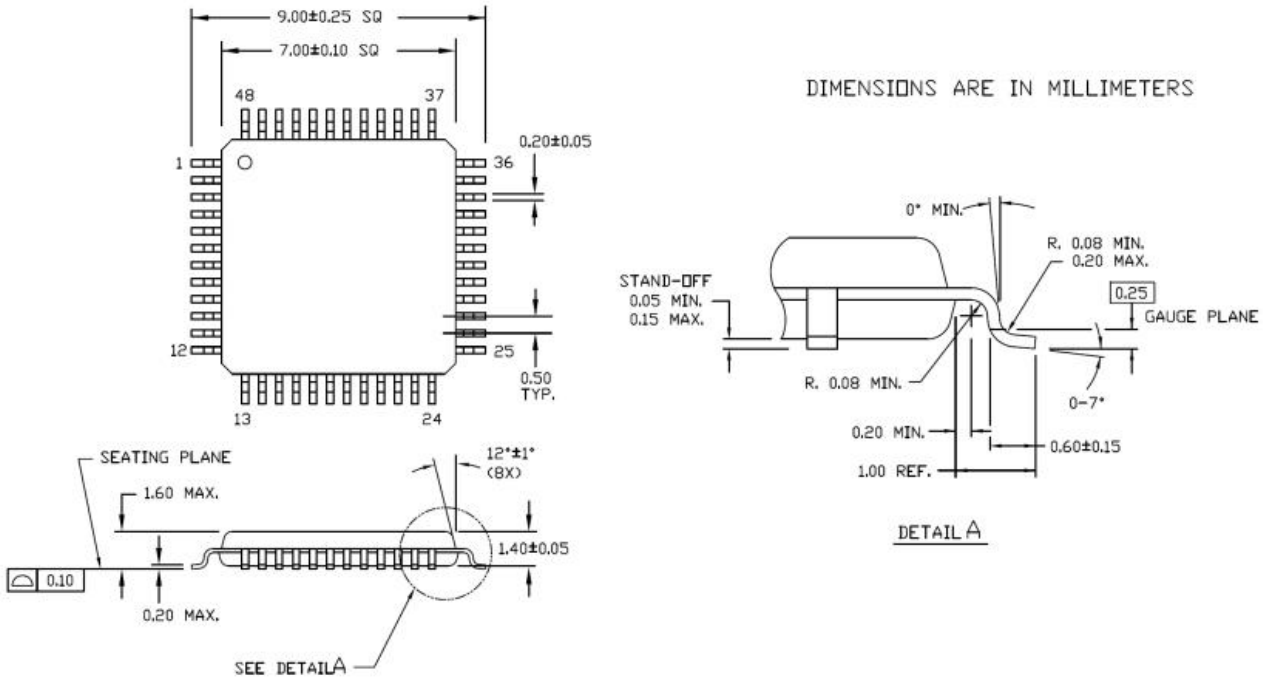
Note Clock is 48 MHz nominal.

Clock Timing Specifications



Parameter	Description	Min	Typical	Max
t_{CLK}	Clock Period (48 MHz)	20ns	20.8ns	--
t_{HIGH}	Clock HIGH Time	9ns	--	11ns
t_{LOW}	Clock LOW Time	9ns	--	11ns
t_{RISE}	Clock Rise Time	--	--	5.0ns
t_{FALL}	Clock Fall Time	--	--	5.0ns
	Clock Duty Cycle	45%	--	55%

Package Outline Dimensions



Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD9001A-48AG	-40℃~85℃	TQFP-48	Tray, 1000

Chinese version:CD9001

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.9	Initial version	Regular update	WW	LYL	

Chinese version:CD9001