CDuD1400_CDuD1401_CDuD1402

Dual-Channel Digital Isolator

Version: Rev 1.0.0 Date: 2025-6-12

Features

- Low power operation

  @5 V operation

  1.0 mA（max）/channel at 0 Mbps to 2 Mbps

  3.5 mA（max）/channel at 10 Mbps

  31 mA（max）/channel at 90 Mbps

  @3 V operation

  0.7 mA（max）/channel at 0 Mbps to 2 Mbps

  2.1 mA（max）/channel at 10 Mbps

  20 mA（max）/channel at 90 Mbps
- Bidirectional communication
- 3 V/5 V level translation
- High temperature operation: 125°C
- High data rate: dc to 90 Mbps (NRZ)
- Precise timing characteristics

  2 ns maximum pulse width distortion

  2 ns maximum channel-to-channel matching
- High common-mode transient immunity: >25 kV/μs
- Output enable function
- 16-lead SOP package
- RoHS-compliant models available
- Safety and regulatory approvals

  UL recognition: 2500 V rms for 1 minute per UL 1577

  CSA Component Acceptance Notice 5A

  VDE Certificate of Conformity

  DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

  V_{IORM} = 560 V peak

TÜV approval: IEC/EN/UL/CSA 61010-1

Application

- General-purpose multichannel
- SPI interface/data converter
- RS-232/RS-422/RS-485
- Industrial field bus isolation
- Automotive systems

Description

The CDuD1400/CDuD1401/CDuD1402 are quad-channel digital isolators. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, Devices remove the design difficulties commonly associated with opto-couplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple digital interfaces and stable performance characteristics.

The need for external drivers and other discrete components is eliminated with these products. Furthermore, Devices consume one tenth to one sixth of the power of optocouplers at comparable signal data rates.

The CDuD1400/CDuD1401/CDuD1402 isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the CDuD1400/ CDuD1401/CDuD1402 provide low pulse width distortion and tight channel-to-channel matching. Unlike other optocoupler alternatives, the CDuD1400/CDuD1401/CDuD1402 isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and when power is not applied to one of the supplies.

Contents

Pin Configurations

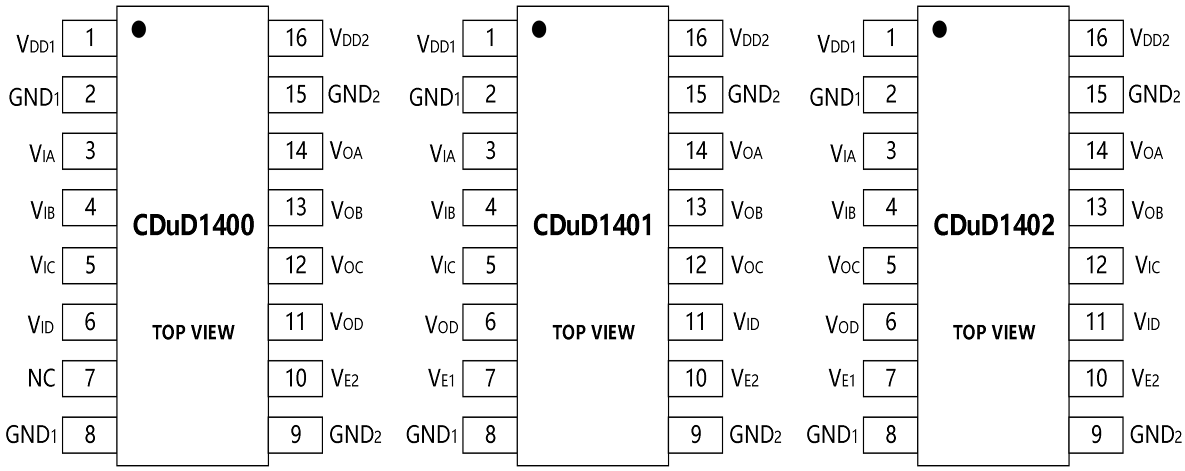


Figure 1. WSOP16 Pin Configuration

Table 1. Pin description

Pin Name	Pin. no (CDuD1400)	Pin. no (CDuD1401)	Pin. no (CDuD1402)	Description
V_{DD1}	1	1	1	Supply Voltage for Isolator Side 1.
GND_1	2,8	2,8	2,8	Ground 1. Ground reference for Isolator Side 1.
V_{IA}	3	3	3	Logic Input A.
V_{IB}	4	4	4	Logic Input B.
V_{IC}	5	5	12	Logic Input C.
V_{ID}	6	11	11	Logic Input D.
V_{E1}	--	--	7	Output Enable 1. Active high logic input. V_{OD} output is enabled when VE1 is high or disconnected. V_{OD} is disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.

NC	7	--	--	No Connect.
GND_2	9,15	9,15	9,15	Ground 1. Ground reference for Isolator Side 2.
V_{E2}	10	10	10	Output Enable 2. Active high logic input. V_{OA}, V_{OB}, VOC, and VOD outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
V_{OD}	11	6	6	Logic Output D.
V_{OC}	12	12	5	Logic Output C.
V_{OB}	13	13	13	Logic Output B.
V_{OA}	14	14	14	Logic Output A.
V_{DD2}	16	16	16	Supply Voltage for Isolator Side 2.

Functional Block diagram

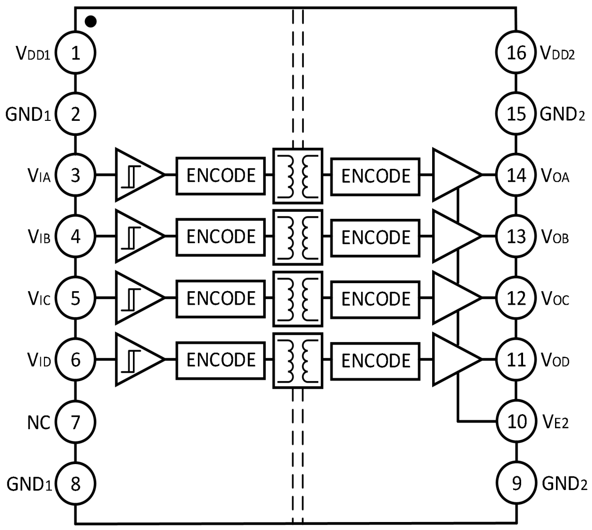


Figure 2. CDuD1400

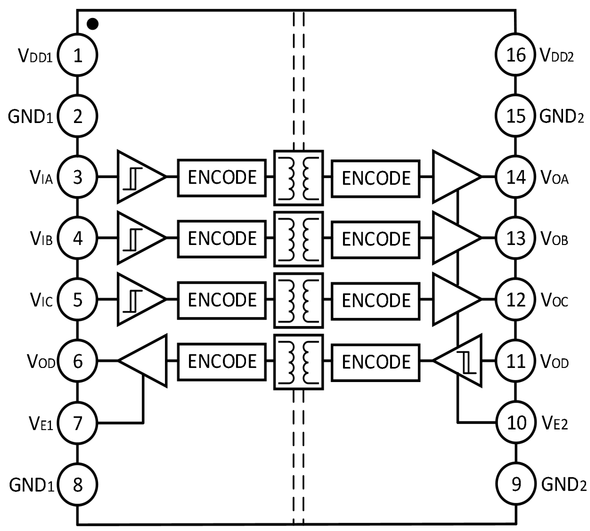


Figure 3. CDuD1401

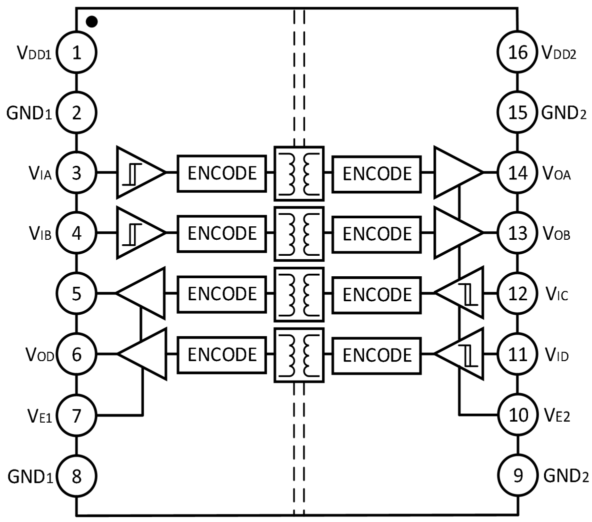


Figure 4. CDuD1402

Table 2. Truth Table(Positive Logic)

VIXINPUT	VEXINPUT	VDDI State	VDDO State	VOX OUTPUT	Notes
H	H or NC	Powered	Powered	H	OFF
L	H or NC	Powered	Powered	L	ON
X	L	Powered	Powered	Z	--
X	H or NC	Unpowered	Powered	H	Outputs return to the input state within 1 μs of V_{DDI} power restoration.
X	L	Unpowered	Powered	Z	-
X	X	Powered	Unpowered	Indeterminate	Outputs return to the input state within 1 μs of V_{DDI} power restoration.

Absolute Maximum Ratings

Parameter	Range
Supply Voltages(V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltage(V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2})	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin :	Side 1 (I_{O1}) : −18 mA to +18 mA Side 2 (I_{O2}) : −22 mA to +22 mA
Storage Temperature Range	−65°C to +150°C
Ambient Operating Temperature	−40℃ to +105℃
Common-Mode Transients	−100 kV/μs to +100 kV/μs
Maximum Continuous Working Voltage	(1) AC Voltage, Bipolar Waveform : 565V peak (2) AC Voltage, Unipolar Waveform

	Basic Insulation : 1131V peak Reinforced Insulation : 560V peak
	(3) DC Voltage Basic Insulation : 1131V peak Reinforced Insulation : 560V peak

Electrical characteristics

4.5 V ≤ VDD1 ≤ 5.5 V, 4.5 V ≤ VDD2 ≤ 5.5 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at TA = 25°C, VDD1 = VDD2 = 5 V.

Table 3.

PARAMETER	Symbol	TA=+25℃			Test Conditions	UNIT
		Min	Typ	Max		
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI\ (Q)}$	--	0.50	0.53		mA
Output Supply Current per Channel, Quiescent	$I_{DDO(Q)}$	--	0.19	0.21		mA
CDuD1400 Total Supply Current, Four Channels						
V_{DD1} Supply Current,DC to 2 Mbps	$I_{DD1(Q)}$	--	2.2	2.8	DC to 1 MHz logic signal freq.	mA
V_{DD2} Supply Current,DC to 2 Mbps	$I_{DD2(Q)}$	--	0.9	1.4	DC to 1 MHz logic signal freq.	mA
V_{DD1} Supply Current, 10 Mbps	$I_{DD1(10)}$	--	8.6	10.6	5 MHz logic signal freq.	mA
V_{DD2} Supply Current, 10 Mbps	$I_{DD2(10)}$	--	2.6	3.5	5 MHz logic signal freq.	mA
V_{DD1} Supply Current, 90 Mbps	$I_{DD1(90)}$	--	70	100	45 MHz logic signal freq.	mA
V_{DD2} Supply Current, 90 Mbps	$I_{DD2(90)}$	--	18	25	45 MHz logic signal freq.	mA
CDuD1401 Total Supply Current, Four Channels						
V_{DD1} Supply Current,DC to 2 Mbps	$I_{DD1(Q)}$	--	1.8	2.4	DC to 1 MHz logic signal freq.	mA
V_{DD2} Supply Current,DC to	$I_{DD2(Q)}$	--	1.2	1.8	DC to 1 MHz logic signal freq.	mA

2 Mbps						
V_{DD1} Supply Current, 10 Mbps	$I_{DD1(10)}$	--	7.1	9.0	5 MHz logic signal freq.	mA
V_{DD2} Supply Current, 10 Mbps	$I_{DD2(10)}$	--	4.1	5.0	5 MHz logic signal freq.	mA
V_{DD1} Supply Current, 90 Mbps	$I_{DD1(90)}$	--	57	82	45 MHz logic signal freq.	mA
V_{DD2} Supply Current, 90 Mbps	$I_{DD2(90)}$	--	31	43	45 MHz logic signal freq.	mA
CDuD1402 Total Supply Current, Four Channels						
V_{DD1} Supply Current,DC to 2 Mbps	$I_{DD1(Q)}$,$I_{DD2(Q)}$	--	1.5	2.1	DC to 1 MHz logic signal freq.	mA
V_{DD1} Supply Current, 10 Mbps	$I_{DD1(10)}$,$I_{DD2(10)}$	--	5.6	7.0	5 MHz logic signal freq.	mA
V_{DD1} Supply Current, 90 Mbps	$I_{DD1(90)}$,$I_{DD2(90)}$	--	44	62	45 MHz logic signal freq.	mA
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	-10	+0.01	+10	0 V ≤ V_{IA}, V_{IB}, V_{IC}, V_{ID} ≤ V_{DD1} or V_{DD2}, 0 V ≤ V_{E1}, V_{E2} ≤ V_{DD1} or V_{DD2}	μA
Logic High Input Threshold	V_{IH}, V_{EH}	2.0	--	--		V
Logic Low Input Threshold	V_{IL}, V_{EL}	--	--	0.8		V
Logic High Output Voltages	V_{OAH},V_{OBH}, V_{OCH},V_{ODH}	(V_{DD1} or V_{DD2}) − 0.1	5.0	--	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}	V
	V_{IL}, V_{EL}	(V_{DD1} or V_{DD2}) − 0.4	4.8	--	I_{Ox} = −3.2mA, V_{Ix} = V_{IxH}	V
Logic Low Output Voltages	V_{OAL},V_{OBL}, V_{OCL},V_{ODL}	--	0.0	0.1	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}	V
		--	0.04	0.1	I_{Ox} = 400μA, V_{Ix} = V_{IxL}	V
		--	0.2	0.4	I_{Ox} = 3.2mA, V_{Ix} = V_{IxL}	V
SWITCHING SPECIFICATIONS	CDuD1400A/CDuD1401A/CDuD1402A					
Minimum Pulse Width	PW	--	--	1000	C_L = 15 pF, CMOS signal levels	ns
Maximum Data Rate	--	1	--	--	C_L = 15 pF, CMOS signal levels	Mbps

Propagation Delay	t_{PHL}, t_{PLH}	50	70	100	C_L = 15 pF, CMOS signal levels	ns
Pulse Width Distortion, |tPLH － tPHL|	PWD	--	--	40	C_L = 15 pF, CMOS signal levels	ns
Change vs. Temperature		--	11	--	C_L = 15 pF, CMOS signal levels	ps/℃
Propagation Delay Skew6	t_{PSK}	--	--	50	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching7	t_{PSKCD}/t_{PSKOD}	--	--	50	C_L = 15 pF, CMOS signal levels	ns
	CDuD1400B/CDuD1401B/CDuD1402B					
Minimum Pulse Width	PW	--	--	100	C_L = 15 pF, CMOS signal levels	ns
Maximum Data Rate	--	10	--	--	C_L = 15 pF, CMOS signal levels	Mbps
Propagation Delay	t_{PHL}, t_{PLH}	15	35	50	C_L = 15 pF, CMOS signal levels	ns
Pulse Width Distortion, |tPLH － tPHL|	PWD	--	--	3	C_L = 15 pF, CMOS signal levels	ns
Change vs. Temperature		--	5	--	C_L = 15 pF, CMOS signal levels	ps/℃
Propagation Delay Skew6	t_{PSK}	--	--	22	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching Codirectional Channels	t_{PSKCD}	--	--	3	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching,Opposing-Directional Channels	t_{PSKOD}	--	--	6	C_L = 15 pF, CMOS signal levels	ns
	CDuD1400C/CDuD1401C/CDuD1402C					
Minimum Pulse Width	PW	--	8.3	11.1	C_L = 15 pF, CMOS signal levels	ns
Maximum Data Rate	--	90	120	--	C_L = 15 pF, CMOS signal levels	Mbps
Propagation Delay	t_{PHL}, t_{PLH}	20	30	40	C_L = 15 pF, CMOS signal levels	ns
Pulse Width Distortion, |tPLH － tPHL|	PWD	--	0.5	2	C_L = 15 pF, CMOS signal levels	ns
Change vs. Temperature		--	3	--	C_L = 15 pF, CMOS signal levels	ps/℃
Propagation Delay Skew6	t_{PSK}	--	--	14	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching Codirectional Channels	t_{PSKCD}	--	--	2	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching,Opposing-Directional Channels	t_{PSKOD}	--	--	5	C_L = 15 pF, CMOS signal levels	ns

For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ},t_{PLH}	--	6	8	C_L = 15 pF, CMOS signal levels	ns
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH},t_{PZL}	--	6	8	C_L = 15 pF, CMOS signal levels	ns
Output Rise/Fall Time (10% to 90%)	t_R/t_F					
5 V/3 V Operation		--	3.0	--	C_L = 15 pF, CMOS signal levels	ns
3 V/5 V Operation		--	2.5	--	C_L = 15 pF, CMOS signal levels	ns
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35	--	V_{IX}= V_{DD1} or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V	kv/μs
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35	--	V_{IX} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V	kv/μs
Refresh Rate	fr					
5 V/3 V Operation		--	1.2	--		Mbps
3 V/5 V Operation		--	1.1	--		Mbps
Input Dynamic Supply Current per Channel9	$I_{DDI(D)}$					
5 V/3 V Operation		--	0.19	--		mA/Mbps
3 V/5 V Operation		--	0.10	--		mA/Mbps
Output Dynamic Supply Current per Channel	$I_{DDO(D)}$					
5 V/3 V Operation		--	0.03	--		mA/Mbps

3 V/5 V Operation		--	0.05	--		mA/Mbps

2.7 V ≤ VDD1 ≤ 3.6 V, 2.7 V ≤ VDD2 ≤ 3.6 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at TA = 25°C, VDD1 = VDD2 = 3 V.

Table 4.

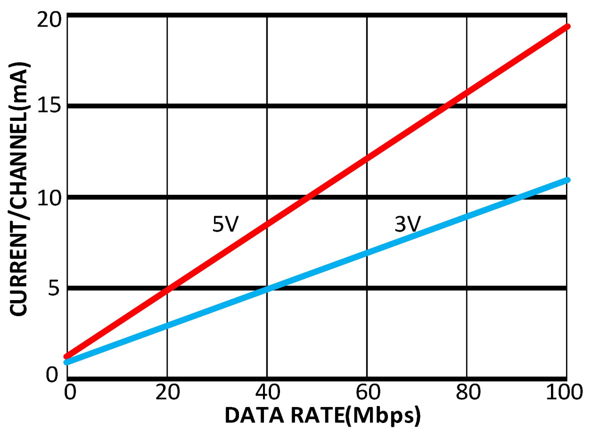
PARAMETER	Symbol	TA=+25℃			Test Conditions	UNIT
		Min	Typ	Max		
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI\ (Q)}$	--	0.26	0.31		mA
Output Supply Current per Channel, Quiescent	$I_{DDO(Q)}$	--	0.11	0.14		mA
CDuD1400 Total Supply Current, Four Channels						
V_{DD1} Supply Current,DC to 2 Mbps	$I_{DD1(Q)}$	--	1.2	1.9	DC to 1 MHz logic signal freq.	mA
V_{DD2} Supply Current,DC to 2 Mbps	$I_{DD2(Q)}$	--	0.5	0.9	DC to 1 MHz logic signal freq.	mA
V_{DD1} Supply Current, 10 Mbps	$I_{DD1(10)}$	--	4.5	6.5	5 MHz logic signal freq.	mA
V_{DD2} Supply Current, 10 Mbps	$I_{DD2(10)}$	--	1.4	2.0	5 MHz logic signal freq.	mA
V_{DD1} Supply Current, 90 Mbps	$I_{DD1(90)}$	--	37	65	45 MHz logic signal freq.	mA
V_{DD2} Supply Current, 90 Mbps	$I_{DD2(90)}$	--	11	15	45 MHz logic signal freq.	mA
CDuD1401 Total Supply Current, Four Channels						
V_{DD1} Supply Current,DC to 2 Mbps	$I_{DD1(Q)}$	--	1.0	1.6	DC to 1 MHz logic signal freq.	mA
V_{DD2} Supply Current,DC to 2 Mbps	$I_{DD2(Q)}$	--	0.7	1.2	DC to 1 MHz logic signal freq.	mA
V_{DD1} Supply Current, 10 Mbps	$I_{DD1(10)}$	--	3.7	5.4	5 MHz logic signal freq.	mA
V_{DD2} Supply Current, 10 Mbps	$I_{DD2(10)}$	--	2.2	3.0	5 MHz logic signal freq.	mA

V_{DD1} Supply Current, 90 Mbps	$I_{DD1(90)}$	--	30	52	45 MHz logic signal freq.	mA
V_{DD2} Supply Current, 90 Mbps	$I_{DD2(90)}$	--	18	27	45 MHz logic signal freq.	mA
CDuD1402 Total Supply Current, Four Channels						
V_{DD1} Supply Current,DC to 2 Mbps	$I_{DD1(Q)}$,$I_{DD2(Q)}$	--	0.9	1.5	DC to 1 MHz logic signal freq.	mA
V_{DD1} Supply Current, 10 Mbps	$I_{DD1(10)}$,$I_{DD2(10)}$	--	3.0	4.2	5 MHz logic signal freq.	mA
V_{DD1} Supply Current, 90 Mbps	$I_{DD1(90)}$,$I_{DD2(90)}$	--	24	39	45 MHz logic signal freq.	mA
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	-10	+0.01	+10	0 V $\leq$ V_{IA}, V_{IB}, V_{IC}, V_{ID} $\leq$ V_{DD1} or V_{DD2}, 0 V $\leq$ V_{E1}, V_{E2} $\leq$ V_{DD1} or V_{DD2}	μA
Logic High Input Threshold	V_{IH}, V_{EH}	1.6	--	--		V
Logic Low Input Threshold	V_{IL}, V_{EL}	--	--	0.4		V
Logic High Output Voltages	V_{OAH},V_{OBH}, V_{OCH},V_{ODH}	(V_{DD1} or V_{DD2}) − 0.1	3.0	--	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}	V
	V_{IL}, V_{EL}	(V_{DD1} or V_{DD2}) − 0.4	2.8	--	I_{Ox} = −3.2mA, V_{Ix} = V_{IxH}	V
Logic Low Output Voltages	V_{OAL},V_{OBL}, V_{OCL},V_{ODL}	--	0.0	0.1	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}	V
		--	0.04	0.1	I_{Ox} = 400μA, V_{Ix} = V_{IxL}	V
		--	0.2	0.4	I_{Ox} = 3.2mA, V_{Ix} = V_{IxL}	V
SWITCHING SPECIFICATIONS	CDuD1400A/CDuD1401A/CDuD1402A					
Minimum Pulse Width	PW	--	--	1000	C_L = 15 pF, CMOS signal levels	ns
Maximum Data Rate	--	1	--	--	C_L = 15 pF, CMOS signal levels	Mbps
Propagation Delay	t_{PHL}, t_{PLH}	50	75	100	C_L = 15 pF, CMOS signal levels	ns
Pulse Width Distortion, |tPLH − tPHL|	PWD	--	--	40	C_L = 15 pF, CMOS signal levels	ns
Change vs. Temperature		--	11	--	C_L = 15 pF, CMOS signal levels	ps/℃

Propagation Delay Skew6	t_{PSK}	--	--	50	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching7	t_{PSKCD}/t_{PSKOD}	--	--	50	C_L = 15 pF, CMOS signal levels	ns
	CDuD1400B/CDuD1401B/CDuD1402B					
Minimum Pulse Width	PW	--	--	100	C_L = 15 pF, CMOS signal levels	ns
Maximum Data Rate	--	10	--	--	C_L = 15 pF, CMOS signal levels	Mbps
Propagation Delay	t_{PHL}, t_{PLH}	20	38	50	C_L = 15 pF, CMOS signal levels	ns
Pulse Width Distortion, |tPLH － tPHL|	PWD	--	--	3	C_L = 15 pF, CMOS signal levels	ns
Change vs. Temperature		--	5	--	C_L = 15 pF, CMOS signal levels	ps/℃
Propagation Delay Skew6	t_{PSK}	--	--	22	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching Codirectional Channels	t_{PSKCD}	--	--	3	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching,Opposing-Directional Channels	t_{PSKOD}	--	--	6	C_L = 15 pF, CMOS signal levels	ns
	CDuD1400C/CDuD1401C/CDuD1402C					
Minimum Pulse Width	PW	--	8.3	11.1	C_L = 15 pF, CMOS signal levels	ns
Maximum Data Rate	--	90	120	--	C_L = 15 pF, CMOS signal levels	Mbps
Propagation Delay	t_{PHL}, t_{PLH}	20	34	45	C_L = 15 pF, CMOS signal levels	ns
Pulse Width Distortion, |tPLH － tPHL|	PWD	--	0.5	2	C_L = 15 pF, CMOS signal levels	ns
Change vs. Temperature		--	3	--	C_L = 15 pF, CMOS signal levels	ps/℃
Propagation Delay Skew6	t_{PSK}	--	--	16	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching Codirectional Channels	t_{PSKCD}	--	--	2	C_L = 15 pF, CMOS signal levels	ns
Channel-to-Channel Matching,Opposing-Directional Channels	t_{PSKOD}	--	--	5	C_L = 15 pF, CMOS signal levels	ns
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ},t_{PLH}	--	6	8	C_L = 15 pF, CMOS signal levels	ns

Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH},t_{PZL}	--	6	8	C_L = 15 pF, CMOS signal levels	ns
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		C_L = 15 pF, CMOS signal levels	ns
Common-Mode Transient Immunity at Logic High Output	$\|CM_H\|$	25	35	--	V_{IX}= V_{DD1} or V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V	kv/μs
Common-Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	25	35	--	V_{IX} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V	kv/μs
Refresh Rate	fr	--	1.1	--		
Input Dynamic Supply Current per Channel9	$I_{DDI(D)}$	--	0.10	--		mA/Mbps
Output Dynamic Supply Current per Channel	$I_{DDO(D)}$	--	0.03	--		mA/Mbps

Typical Characteristics



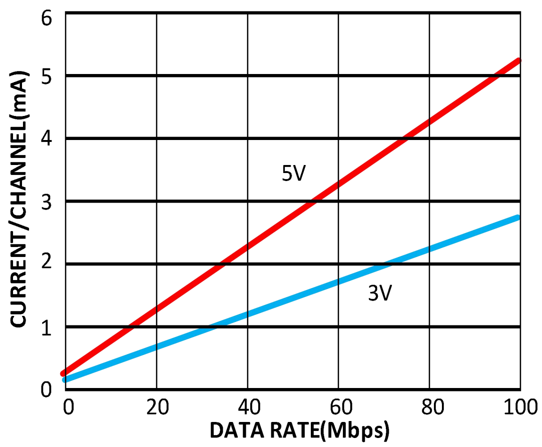
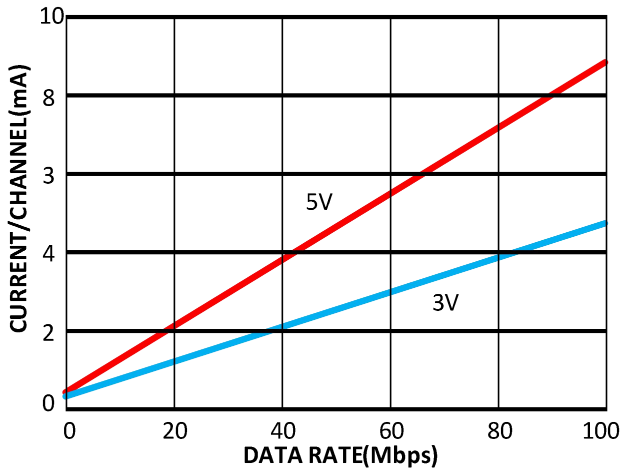


Figure 5. Typical Input Supply Current per Channel vs. Data Rate for 5V and 3V Operation

Figure 6. Typical Output Supply Current per Channel vs. Data Rate for 5V and 3V Operation (No Output Load)



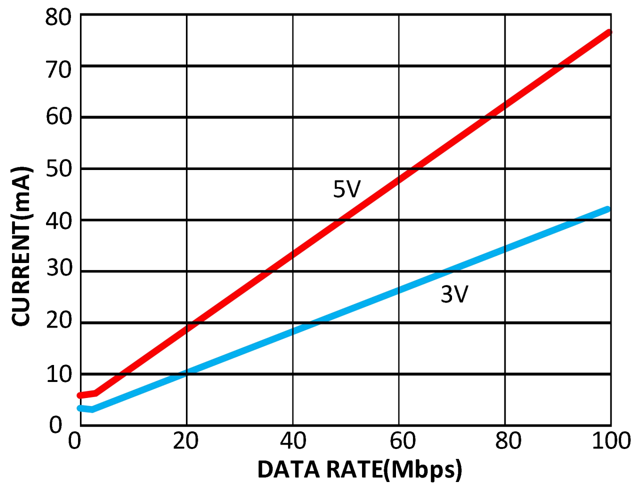
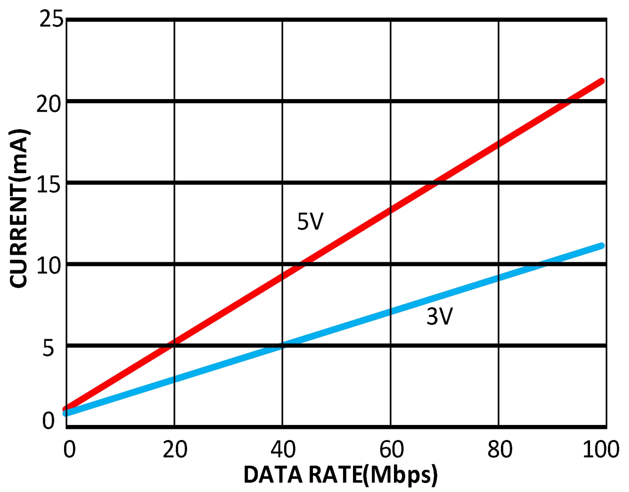


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3V Operation (15 pF Output Load)

Figure 8. Typical CDuD1400 V_{DD1} Supply Current vs. Data Rate for 5V and 3V Operation



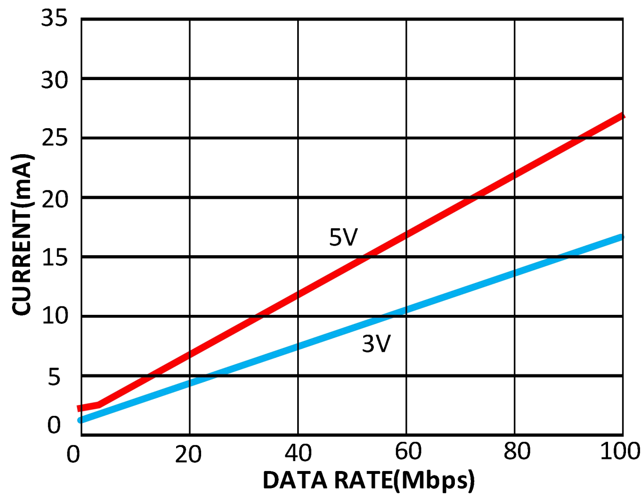
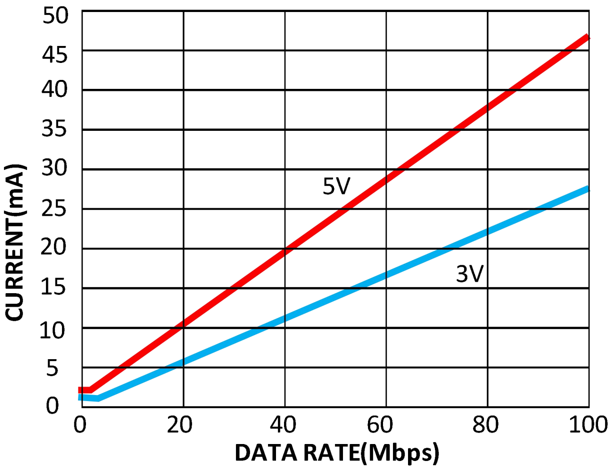


Figure 9. Typical CDuD1400 V_{DD2} Supply Current vs. Data Rate for 5V and 3V Operation

Figure 10. Typical CDuD1401 V_{DD1} Supply Current vs. Data Rate for 5V and 3V Operation



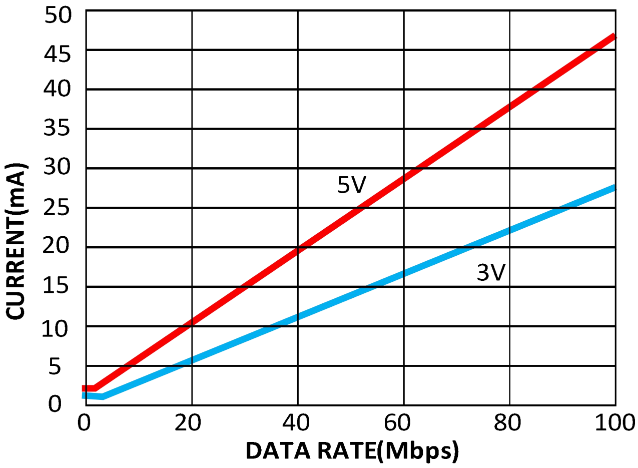


Figure 11. Typical CDuD1401 V_{DD2} Supply Current vs. Data Rate for 5V and 3V Operation

Figure 12. Typical CDuD1402 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5V and 3V Operation

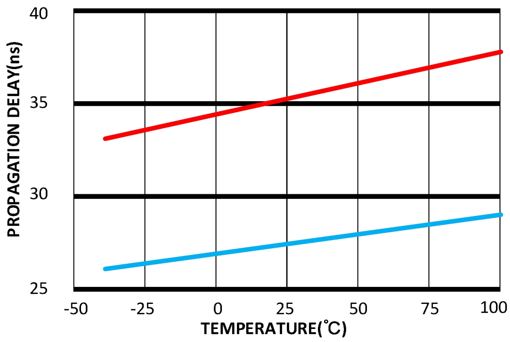


Figure 13. Propagation Delay vs. Temperature

Package Outline Dimensions

WSOP-16

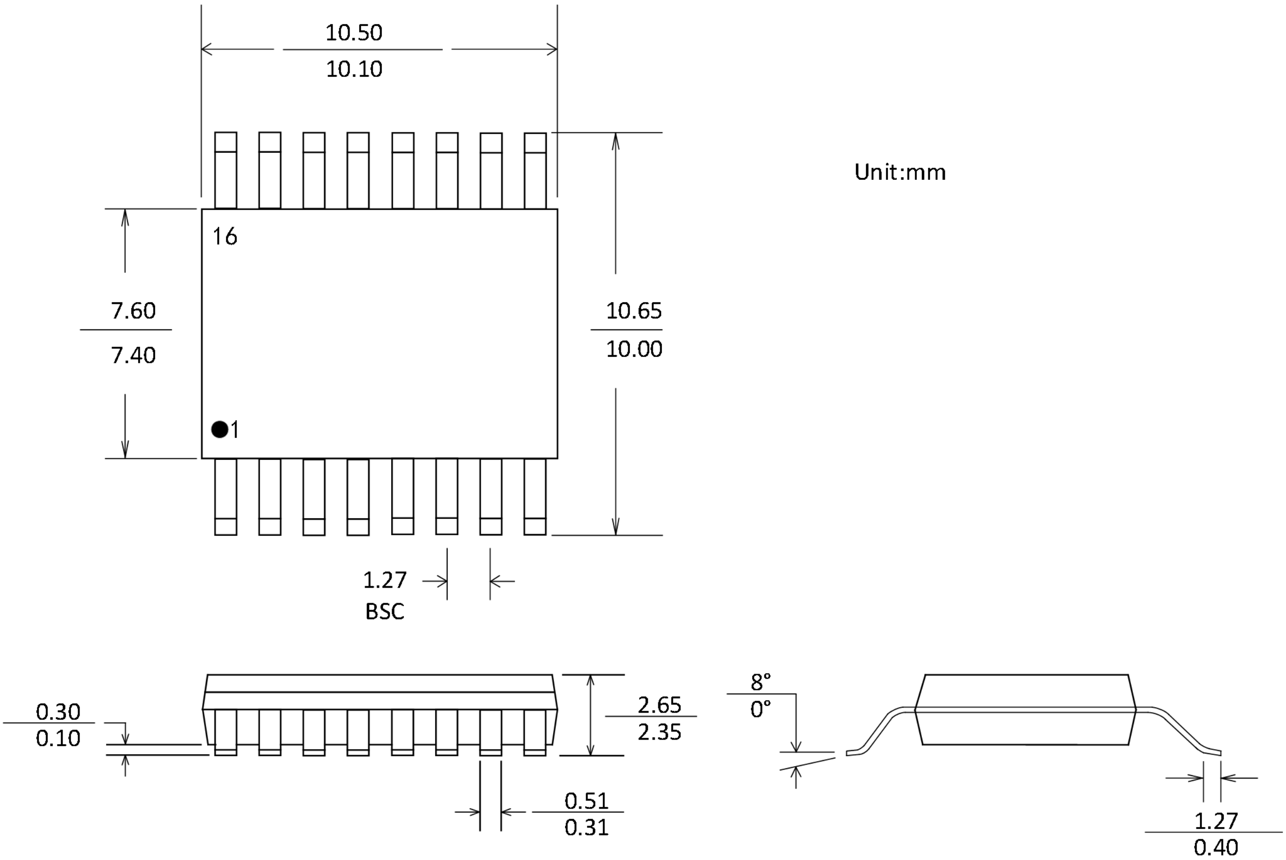


Figure 11. 16-Lead Outline Package Wide body [WSOP]

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CDuD1400HAS16	-40℃~105℃	WSOP-16	Tape and Reel, 2500
CDuD1400LAS16	-40℃~105℃	WSOP-16	Tape and Reel, 2500
CDuD1401HAS16	-40℃~105℃	WSOP-16	Tape and Reel, 2500
CDuD1401LAS16	-40℃~105℃	WSOP-16	Tape and Reel, 2500
CDuD1402HAS16	-40℃~105℃	WSOP-16	Tape and Reel, 2500
CDuD1402LAS16	-40℃~105℃	WSOP-16	Tape and Reel, 2500

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.6.3	Initial version	Regular update	WW	LYL	
V1.0	2025.6.12	Update the dimension drawing and description of WSOP16.	Error update	WW	LYL	