CoreadDvices
承芯微电子

# CD76AD06

8-Channel DAS with 16-Bit, Bipolar Input, Simultaneous Sampling ADC

Version: Rev 1.0.0 Date: 2025-10-15

## Features

- 8 simultaneously sampled inputs
- True bipolar analog input ranges: ±10 V, ±5 V
- 5 V analog power supply and 2.3 V to 5 V digital power supply
- Analog input clamp protection
- Input buffer with 1 MΩ analog input
- Second-order antialiasing analog filter
- On-chip accurate reference and reference
- 16-bit ADC with 200 kSPS on all channels
- Oversampling capability with digital filter
- Flexible parallel/serial interface
- SPI/QSPI™/MICROWIRE™/DSP compatible
- 7 kV ESD rating on analog input channels
- 93.5 dB SNR, −107 dB THD
- ±0.3 LSB INL, ±0.5 LSB DNL
- Low power: 130 mW
- Standby mode: 24.6 mW
- Temperature range: −40°C to +85°C
- 64-lead LQFP package

## Application

- Semiconductor Automatic Test
- Power-line monitoring and protection systems
- Multiphase motor control
- Instrumentation and control systems
- Multiaxis positioning systems
- Data acquisition systems

## Description

The CD76AD06 is 16-bit, simultaneous sampling, analog-to-digital data acquisition systems (DAS) with eight channels. Each channel contains analog input clamp protection, a second-order antialiasing filter, a track-and-hold amplifier, a 16-bit charge redistribution successive approximation analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces. The CD76AD06 operate from a single 5 V supply and can accommodate ±10 V and ±5 V true bipolar input signals while sampling at throughput rates up to 200 kSPS for all channels. The input clamp protection circuitry can tolerate voltages up to ±16.5 V. Each channel has 1 MΩ analog input impedance regardless of sampling frequency. The single supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies. The CD76AD06 antialiasing filter has a 3 dB cutoff frequency of 22 kHz and provides 40 dB antialias rejection when sampling at 200 kSPS. The flexible digital filter is pin driven, yields
improvements in SNR, and reduces the 3 dB bandwidth.

# Contents

## Block Diagram

This product adopts LQFP-64 package. It is specified over the −40°C to +85°C

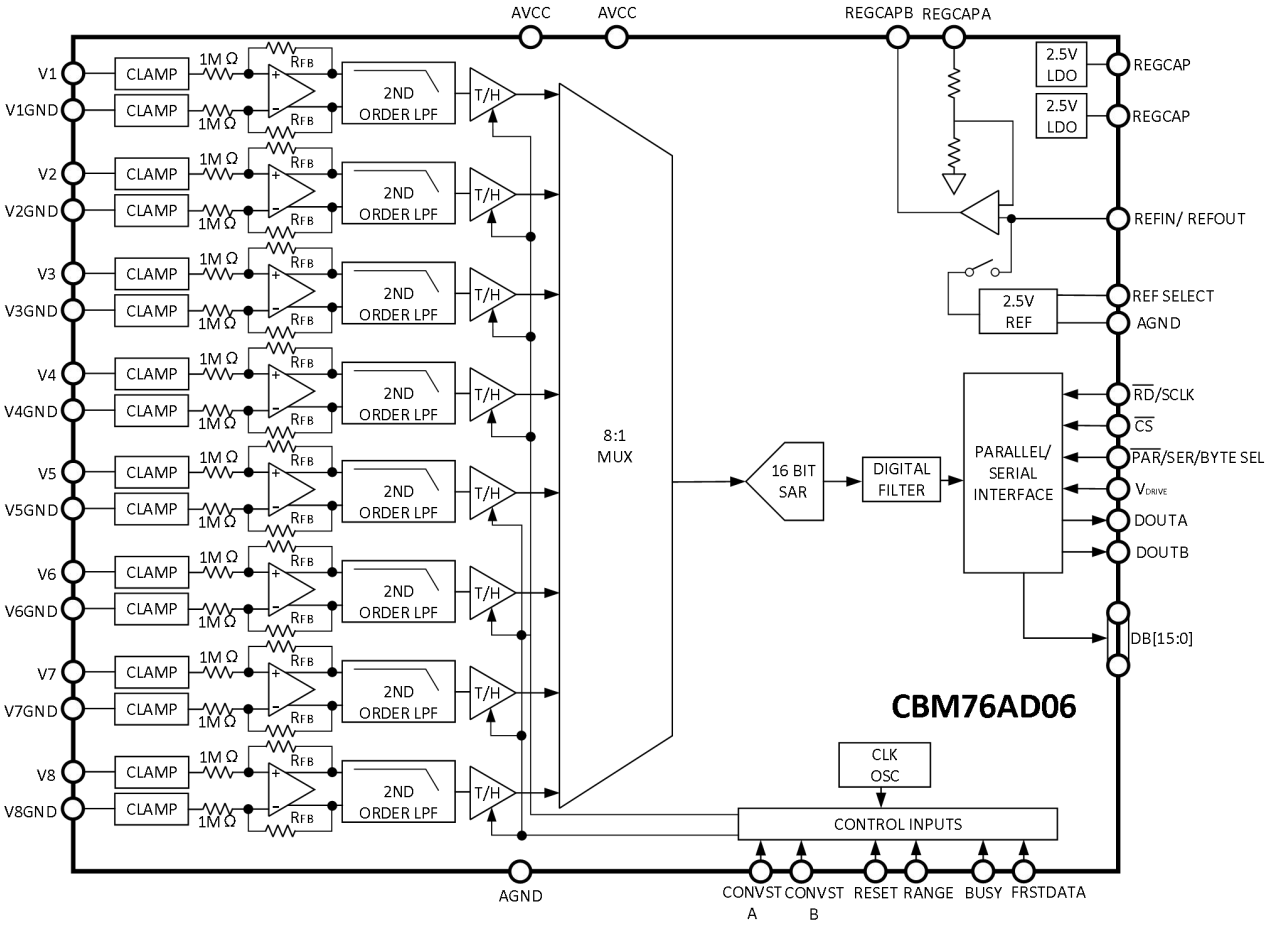


Figure 1. Functional Block Diagram

## Electrical characteristics

VREF = 2.5 V external/internal, $A_{VCC}$ = 4.75 V to 5.25 V, $V_{DRIVE}$ = 2.3 V to 5.25 V, $f_{SAMPLE}$ = 200 kSPS, $T_A$ = −40°C to +85°C, unless otherwise noted.

Table1.

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE** | $f_{IN}$ = 1 kHz sine wave | -- | -- | -- | -- |
| Signal-to-Noise Ratio(SNR)[1, 2] | Oversampling by 16; ±10 V range; $f_{IN}$ = 130 Hz | 91.3 | 93.5 | -- | dB |
| | Oversampling by 16; ±5 V range; | 91.6 | 93.5 | -- | dB |



Chinese version:CD76AD06

| | | | | | |
|---|---|---|---|---|---|
| | $f_{IN}$ = 130 Hz | | | | |
| | No oversampling; ±10 V Range | 87 | 89.7 | -- | dB |
| | No oversampling; ±5 V range | 87.2 | 89 | -- | dB |
| Signal-to-(Noise +Distortion) (SINAD)[1] | No oversampling; ±10 V range | 87 | 89 | -- | dB |
| | No oversampling; ±5 V range | 87.1 | 89 | -- | dB |
| Dynamic Range | No oversampling; ±10 V range | -- | 90.5 | -- | dB |
| | No oversampling; ±5 V range | -- | 90 | -- | dB |
| Total Harmonic Distortion (THD)[1] | | -- | -107 | -95 | dB |
| Peak Harmonic or Spurious Noise (SFDR)[1] | | -- | -108 | -- | dB |
| Intermodulation Distortion (IMD) 1 | fa = 1 kHz, fb = 1.1 kHz | | | | |
| Second-Order Terms | | -- | -107 | -- | dB |
| Third-Order Terms | | -- | -103 | -- | dB |
| Channel-to-Channel Isolation1 | $f_{IN}$ on unselected channels up to 160 kHz | -- | -95 | -- | dB |
| **ANALOG INPUT FILTER** | | | | | |
| Full Power Bandwidth | −3 dB, ±10 V range | -- | 23 | -- | kHz |
| | −3 dB, ±5 V range | -- | 15 | -- | kHz |
| | −0.1 dB, ±10 V range | -- | 10 | -- | kHz |
| | −0.1 dB, ±5 V range | -- | 5 | -- | kHz |
| $t_{GROUP\ DELAY}$ | ±10 V range | -- | 11 | -- | µs |
| | ±5 V range | -- | 15 | -- | µs |
| **DC ACCURACY** | | | | | |
| Resolution | No missing codes | 16 | -- | -- | Bits |
| Differential Nonlinearity[1] | | -- | ±0.3 | ±1.1 | LSB[3] |
| Integral Nonlinearity[1] | | -- | ±0.5 | ±2.3 | LSB |
| Total Unadjusted Error (TUE) | ±10 V range | -- | ±6 | -- | LSB |
| | ±5 V range | -- | ±12 | -- | LSB |
| Positive Full-Scale Error 1, 4 | External reference | -- | ±8.6 | ±33 | LSB |
| | Internal reference | -- | ±8.6 | -- | LSB |
| Positive Full-Scale Error Drift | External reference | -- | ±2 | -- | ppm/℃ |
| | Internal reference | -- | ±7 | -- | ppm/℃ |
| Positive Full-Scale Error | ±10 V range | -- | 5 | 32 | LSB |

| | | | | | |
|---|---|---|---|---|---|
| Matching[1] | ±5 V range | -- | 16 | 40 | LSB |
| Bipolar Zero Code Error[1, 5] | ±10 V range | -- | ±1 | ±6 | LSB |
| | ±5 V range | -- | ±3 | ±12 | LSB |
| Bipolar Zero Code Error Drift | ±10 V range | -- | 10 | -- | μV/℃ |
| | ±5 V range | -- | 5 | -- | μV/℃ |
| Bipolar Zero Code Error Matching[1] | ±10 V range | -- | 1 | 8 | LSB |
| | ±5 V range | -- | 6 | 22 | LSB |
| Negative Full-Scale Error[1, 4] | External reference | -- | ±8 | ±32 | LSB |
| | Internal reference | -- | ±8 | -- | LSB |
| Negative Full-Scale Error Drift | External reference | -- | ±4 | -- | ppm/℃ |
| | Internal reference | -- | ±8 | -- | ppm/℃ |
| Negative Full-Scale Error Matching[1] | ±10 V range | -- | 5 | 32 | LSB |
| | ±5 V range | -- | 15 | 38 | LSB |
| **ANALOG INPUT** | | | | | |
| Input Voltage Ranges | RANGE = 1 | -- | -- | ±10 | V |
| | RANGE = 0 | -- | -- | ±5 | V |
| Analog Input Current | 10V | -- | 5.2 | -- | μA |
| | 5V | -- | 2.2 | -- | μA |
| Input Capacitance[6] | -- | -- | 5 | -- | pF |
| Input Impedance | See the Analog Input section | -- | 1 | -- | MΩ |
| **REFERENCE INPUT/OUTPUT** | | | | | |
| Reference Input Voltage Range | See the ADC Transfer Function section | 2.475 | 2.5 | 2.525 | V |
| DC Leakage Current | | -- | -- | ±1 | μA |
| Input Capacitance[6] | REF SELECT = 1 | -- | 7.5 | -- | pF |
| Reference Output Voltage | REFIN/REFOUT | -- | 2.49/ 2.505 | -- | V |
| Reference Temperature Coefficient | -- | -- | ±10 | -- | ppm/°C |
| **LOGIC INPUTS** | | | | | |
| Input High Voltage ($V_{INH}$) | -- | 0.7 × $V_{DRIVE}$ | -- | -- | V |
| Input Low Voltage ($V_{INL}$) | -- | -- | -- | 0.3 × VDRIVE | V |
| Input Current ($I_{IN}$) | -- | -- | -- | ±2.3 | μA |

| | | | | | |
|---|---|---|---|---|---|
| Input Capacitance ($C_{IN}$) [6] | -- | -- | 5 | -- | pF |
| **CONVERSION RATE** | | | | | |
| Conversion Time | All eight channels included; see Table 2 | -- | 4 | -- | µs |
| Track-and-Hold Acquisition Time | -- | -- | 1 | -- | µs |
| Throughput Rate | Per channel, all eight channels included | -- | -- | 200 | kSPS |
| **POWER REQUIREMENTS** | | | | | |
| $AV_{CC}$ | -- | 4.75 | -- | 5.25 | V |
| $V_{DRIVE}$ | -- | 2.3 | -- | 5.25 | V |
| $I_{TOTAL}$ | Digital inputs = 0 V or $V_{DRIVE}$ | | | | |
| Normal Mode (Static) | -- | -- | 16.4 | 25 | mA |
| Normal Mode (Operational)[7] | $f_{SAMPLE}$ = 200 kSPS | -- | 22 | 28 | mA |
| Standby Mode | -- | -- | 5 | 10 | mA |
| Shutdown Mode | -- | -- | 1.8 | 8 | µA |
| **Power Dissipation** | | | | | |
| Normal Mode (Static) | -- | -- | 81.7 | 115.5 | mW |
| Normal Mode (Operational) | fSAMPLE = 200 kSPS | -- | 100 | 142 | mW |
| Standby Mode | -- | | 25 | 42 | mW |
| Shutdown Mode | -- | | 10 | 31.5 | µW |

[1] See the Terminology section.

[2] This specification applies when reading during a conversion or after a conversion. If reading during a conversion in parallel mode with VDRIVE = 5 V, SNR typically reduces by 1.5 dB and THD by 3 dB.

[3] LSB means least significant bit. With ±5 V input range, 1 LSB = 152.58 µV. With ±10 V input range, 1 LSB = 305.175 µV.

[4] These specifications include the full temperature range variation and contribution from the internal reference buffer but do not include the error contribution from the external reference.

[5] Bipolar zero code error is calculated with respect to the analog input voltage. See the Analog Input Clamp Protection section.

[6] Sample tested during initial release to ensure compliance.

[7] Operational power/current figure includes contribution when running in oversampling mode.

## Timing Specifications

$A_{VCC}$ = 4.75 V to 5.25 V, $V_{DRIVE}$ = 2.3 V to 5.25 V, VREF = 2.5 V external reference/internal reference, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.1

Table 2.

| Parameter | Limit at TMIN, TMAX (0.1 × VDRIVE and 0.9 × VDRIVE Logic Input Levels) | | | Limit at TMIN, TMAX (0.3 × VDRIVE and 0.7 × VDRIVE Logic Input Levels) | | | Unit | Description |
|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | | |
| PARALLEL/SERIAL/BYTE MODE | | | | | | | | |
| $t_{CYCLE}$ | -- | -- | -- | -- | -- | -- | -- | 1/throughput rate |
| | -- | -- | 5 | -- | -- | 5 | μs | Parallel mode, reading during or after conversion; or serial mode: $V_{DRIVE}$ = 3.3 V to 5.25 V, reading during a conversion using $D_{OUT}$A and $D_{OUT}$B lines |
| | -- | -- | -- | -- | -- | 9.4 | μs | Serial mode reading after a conversion; VDRIVE = 2.7 V |
| | -- | -- | 9.7 | -- | -- | 10.7 | μs | Serial mode reading after a conversion; VDRIVE = 2.3 V, $D_{OUT}$A and $D_{OUT}$B lines |
| $t_{CONV}$[2] | | | | | | | | Conversion time |
| $t_{CONV}$[2] | 3.45 | 4 | 4.2 | 3.45 | 4 | 4.2 | μs | Oversampling off; |
| | -- | 3 | -- | -- | 3 | -- | -- | Oversampling off; |
| | -- | 2 | -- | -- | 2 | -- | -- | Oversampling off; |
| | 7.87 | -- | 9.1 | 7.87 | -- | 9.1 | μs | Oversampling by 2; |
| | 16.05 | -- | 18.8 | 16.05 | -- | 18.8 | μs | Oversampling by 4; |
| | 33 | -- | 39 | 33 | -- | 39 | μs | Oversampling by 8; |
| | 66 | -- | 78 | 66 | -- | 78 | μs | Oversampling by 16; |
| | 133 | -- | 158 | 133 | -- | 158 | μs | Oversampling by 32; |
| | 257 | -- | 315 | 257 | -- | 315 | μs | Oversampling by 64; |
| $t_{WAKE-UP\ STANDBY}$ | -- | -- | 100 | -- | -- | 100 | μs | $\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from standby mode |
| $t_{WAKE-UP\ SHUTDOWN}$ | | | | | | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Internal Reference | -- | -- | 30 | -- | -- | 30 | ms | $\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from shutdown mode |
| External Reference | -- | -- | 13 | -- | -- | 13 | ms | $\overline{STBY}$ rising edge to CONVST x rising edge; power-up time from shutdown mode |
| $t_{RESET}$ | 50 | -- | -- | 50 | -- | -- | ns | RESET high pulse width |
| $t_{OS\_SETUP}$ | 20 | -- | -- | 20 | -- | -- | ns | BUSY to OS x pin setup time |
| $t_{OS\_HOLD}$ | 20 | -- | -- | 20 | -- | -- | ns | BUSY to OS x pin hold time |
| $t_1$ | | -- | 40 | -- | -- | 45 | ns | CONVST x high to BUSY high |
| $t_2$ | 25 | -- | -- | 25 | -- | -- | ns | Minimum CONVST x low pulse |
| $t_3$ | 25 | -- | -- | 25 | -- | -- | ns | Minimum CONVST x high pulse |
| $t_4$ | 0 | -- | -- | 0 | -- | -- | ns | BUSY falling edge to $\overline{CS}$ falling edge setup time |
| $t_5$[3] | -- | -- | 0.5 | -- | -- | 0.5 | ms | Maximum delay allowed between CONVST A, CONVST B rising edges |
| $t_6$ | -- | -- | 25 | -- | -- | 25 | ns | Maximum time between last $\overline{CS}$ rising edge and BUSY falling edge |
| $t_7$ | -- | 25 | -- | -- | 25 | -- | ns | Minimum delay between RESET low to CONVST x high |
| PARALLEL/BYTE READ OPERATION | | | | | | | | |
| $t_8$ | 0 | | | 0 | | | ns | $\overline{CS}$ to $\overline{RD}$ setup time |
| $t_9$ | 0 | | | 0 | | | ns | $\overline{CS}$ to $\overline{RD}$ hold time |
| $t_{10}$ | -- | -- | -- | -- | -- | -- | -- | $\overline{RD}$ low pulse width |
| | 16 | -- | -- | 19 | -- | -- | ns | VDRIVE above 4.75 V |
| | 21 | -- | -- | 24 | -- | -- | ns | VDRIVE above 3.3 V |
| | 25 | -- | -- | 30 | -- | -- | ns | VDRIVE above 2.7 V |
| | 32 | -- | -- | 37 | -- | -- | ns | VDRIVE above 2.3 V |
| $t_{11}$ | 15 | -- | -- | 15 | -- | -- | ns | $\overline{RD}$ high pulse width |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $t_{12}$ | 22 | -- | -- | 22 | -- | -- | ns | $\overline{CS}$ high pulse width (see Figure 5); $\overline{CS}$ and $\overline{RD}$ linked |
| $t_{13}$ | -- | -- | -- | -- | -- | -- | -- | Delay from $\overline{CS}$ until DB[15:0] three-state disabled |
| | -- | -- | 16 | -- | -- | 19 | ns | VDRIVE above 4.75 V |
| | -- | -- | 20 | -- | -- | 24 | ns | VDRIVE above 3.3 V |
| | -- | -- | 25 | -- | -- | 30 | ns | VDRIVE above 2.7 V |
| | -- | -- | 30 | -- | -- | 37 | ns | VDRIVE above 2.3 V |
| $t_{14}$[4] | -- | -- | | -- | -- | -- | -- | Data access time after $\overline{RD}$ falling edge |
| | -- | -- | 16 | -- | -- | 19 | ns | VDRIVE above 4.75 V |
| | -- | -- | 21 | -- | -- | 24 | ns | VDRIVE above 3.3 V |
| | -- | -- | 25 | -- | -- | 30 | ns | VDRIVE above 2.7 V |
| | -- | -- | 32 | -- | -- | 37 | ns | VDRIVE above 2.3 V |
| $t_{15}$ | 6 | -- | -- | 6 | -- | -- | ns | Data hold time after $\overline{RD}$ falling edge |
| $t_{16}$ | 6 | -- | -- | 6 | -- | -- | ns | $\overline{CS}$ to DB[15:0] hold time |
| $t_{17}$ | -- | -- | 22 | -- | -- | 22 | ns | Delay from $\overline{CS}$ rising edge to DB[15:0] three-state enabled |
| SERIAL READ OPERATION | | | | | | | | |
| $f_{SCLK}$ | -- | -- | -- | -- | -- | -- | -- | Frequency of serial read clock |
| | -- | -- | 23.5 | -- | -- | 20 | MHz | VDRIVE above 4.75 V |
| | -- | -- | 17 | -- | -- | 15 | MHz | VDRIVE above 3.3 V |
| | -- | -- | 14.5 | -- | -- | 12.5 | MHz | VDRIVE above 2.7 V |
| | -- | -- | 11.5 | -- | -- | 10 | MHz | VDRIVE above 2.3 V |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $t_{18}$ | -- | -- | -- | -- | -- | -- | -- | Delay from $\overline{CS}$ until DOUTA/DOUTB three-state disabled/delay from $\overline{CS}$ until MSB valid |
| | -- | -- | 15 | -- | -- | 18 | ns | VDRIVE above 4.75 V |
| | -- | -- | 20 | -- | -- | 23 | ns | VDRIVE above 3.3 V |
| | -- | -- | 30 | -- | -- | 35 | ns | VDRIVE above 2.7 V |
| $t_{19}$[4] | -- | -- | -- | -- | -- | -- | -- | Data access time after SCLK rising edge |
| | -- | -- | 17 | -- | -- | 20 | ns | VDRIVE above 4.75 V |
| | -- | -- | 23 | -- | -- | 26 | ns | VDRIVE above 3.3 V |
| | -- | -- | 27 | -- | -- | 32 | ns | VDRIVE above 2.7 V |
| | -- | -- | 34 | -- | -- | 39 | ns | VDRIVE above 2.3 V |
| $t_{20}$ | 0.4 $t_{SCLK}$ | -- | -- | 0.4 $t_{SCLK}$ | -- | -- | ns | SCLK low pulse width |
| $t_{21}$ | 0.4 $t_{SCLK}$ | -- | -- | 0.4 $t_{SCLK}$ | -- | -- | ns | SCLK high pulse width |
| $t_{22}$ | 7 | -- | -- | 7 | -- | -- | | SCLK rising edge to DOUTA/DOUTB valid hold time |
| $t_{23}$ | -- | -- | 22 | -- | -- | 22 | ns | $\overline{CS}$ rising edge to DOUTA/DOUTB three-state enabled |
| $t_{24}$ | | | | | | | ns | Delay from $\overline{CS}$ falling edge until FRSTDATA three-state disabled |
| | -- | -- | 15 | -- | -- | 18 | ns | VDRIVE above 4.75 V |
| | -- | -- | 20 | -- | -- | 23 | ns | VDRIVE above 3.3 V |
| | -- | -- | 25 | -- | -- | 30 | ns | VDRIVE above 2.7 V |
| | -- | -- | 30 | -- | -- | 35 | ns | VDRIVE above 2.3 V |
| $t_{25}$ | -- | -- | -- | -- | -- | -- | ns | Delay from $\overline{RD}$ falling edge to FRSTDATA high |
| | -- | -- | 15 | -- | -- | 18 | ns | VDRIVE above 4.75 V |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | -- | -- | 20 | -- | -- | 23 | ns | VDRIVE above 3.3 V |
| | -- | -- | 25 | -- | -- | 30 | ns | VDRIVE above 2.7 V |
| | -- | -- | 30 | -- | -- | 35 | ns | VDRIVE above 2.3 V |
| $t_{26}$ | -- | -- | -- | -- | -- | -- | -- | Delay from $\overline{RD}$ falling edge to FRSTDATA high |
| | -- | -- | 16 | -- | -- | 19 | ns | VDRIVE above 4.75 V |
| | -- | -- | 20 | -- | -- | 23 | ns | VDRIVE above 3.3 V |
| | -- | -- | 25 | -- | -- | 30 | ns | VDRIVE above 2.7 V |
| | -- | -- | 30 | -- | -- | 35 | ns | VDRIVE above 2.3 V |
| $t_{27}$ | -- | -- | -- | -- | -- | -- | -- | Delay from $\overline{RD}$ falling edge to FRSTDATA low |
| | -- | -- | 19 | -- | -- | 22 | ns | VDRIVE = 3.3 V to 5.25V |
| | -- | -- | 24 | -- | -- | 29 | ns | VDRIVE = 2.3 V to 2.7V |
| $t_{28}$ | -- | -- | -- | -- | -- | -- | -- | Delay from 16th SCLK falling edge to FRSTDATA low |
| | -- | -- | 17 | -- | -- | 20 | ns | VDRIVE = 3.3 V to 5.25V |
| | -- | -- | 22 | -- | -- | 27 | ns | VDRIVE = 2.3 V to 2.7V |
| $t_{29}$ | -- | -- | 24 | -- | -- | 29 | ns | Delay from $\overline{CS}$ rising edge until FRSTDATA three-state enabled |

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tR = tF = 5 ns (10% to 90% of VDRIVE) and timed from a voltage level of 1.6 V.

[2] In oversampling mode, typical tCONV for the CD76AD06 can be calculated using ((N × tCONV) + ((N −1) × 1 µs)).

[3] The delay between the CONVST x signals was measured as the maximum time allowed while ensuring a <10 LSB performance matching between channel sets.

[4] A buffer is used on the data output pins for these measurements, which is equivalent to a load of 20 pF on the output pins.

## Timing Sequence Diagram

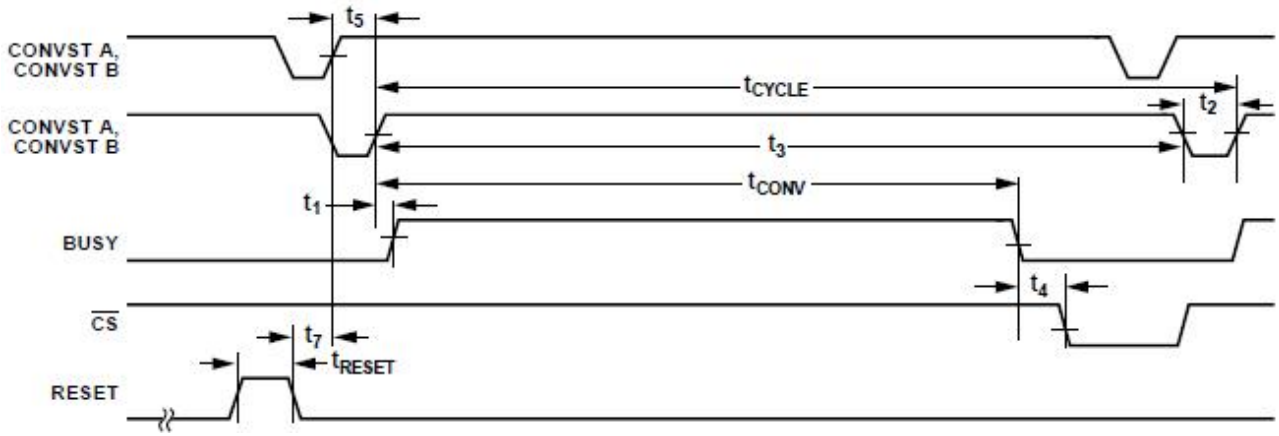


Figure 2. CONVST Timing—Reading After a Conversion

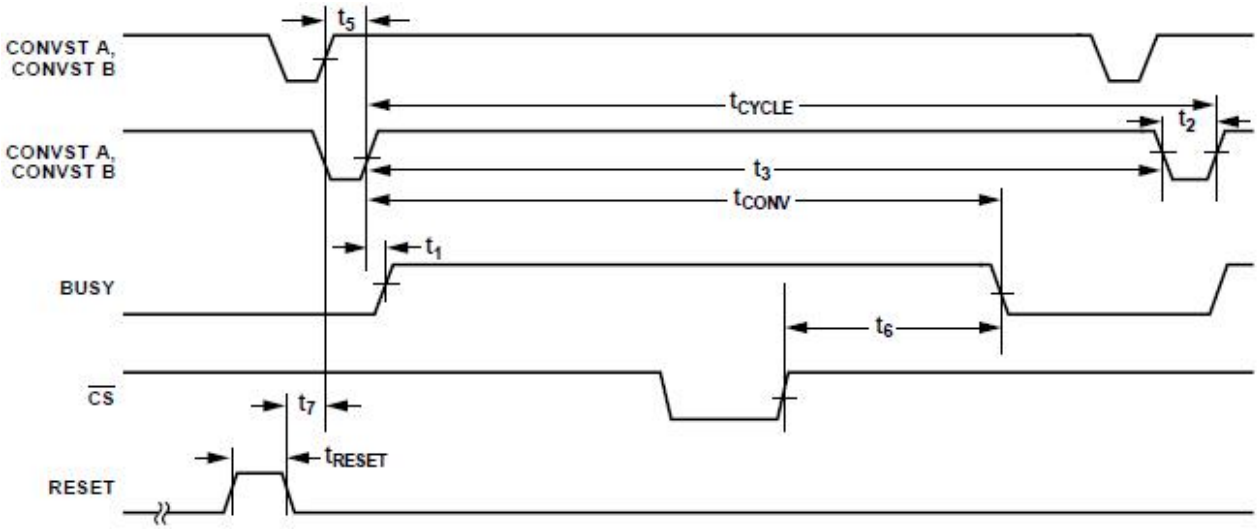


Figure 3. CONVST Timing—Reading During a Conversion

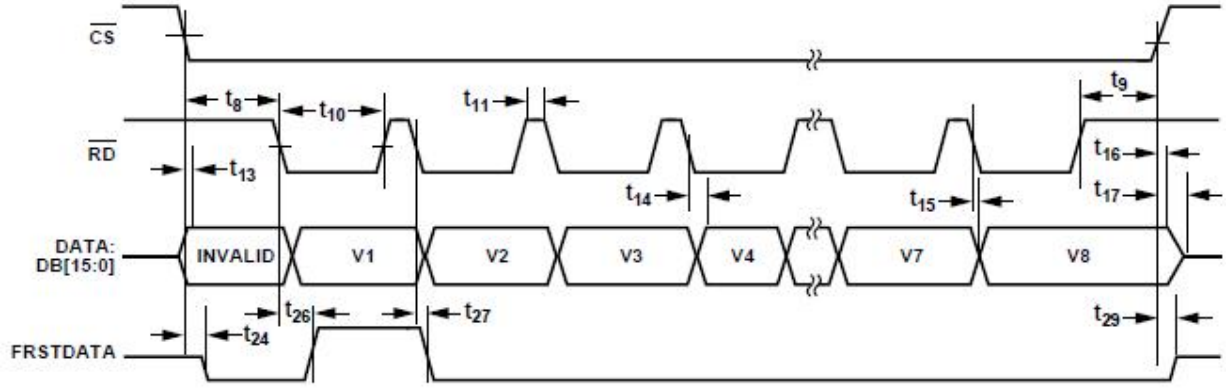


Figure 4. Parallel Mode, Separate $\overline{CS}$ and $\overline{RD}$ Pulses

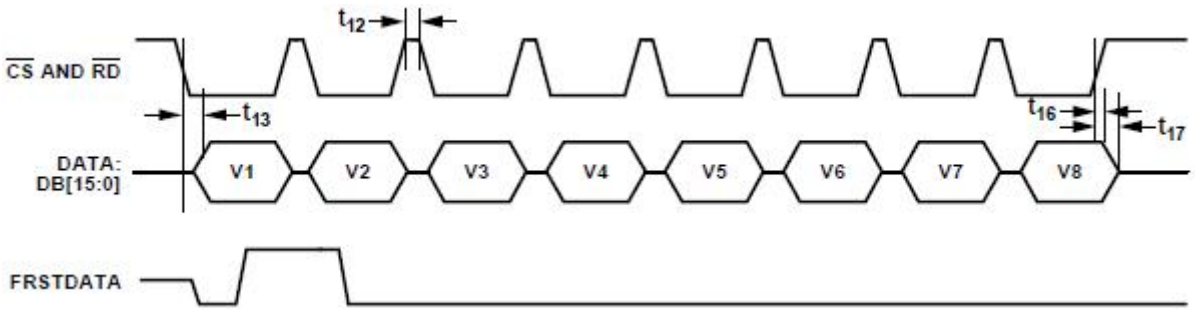


Figure 5. $\overline{CS}$ and $\overline{RD}$, Linked Parallel Mode

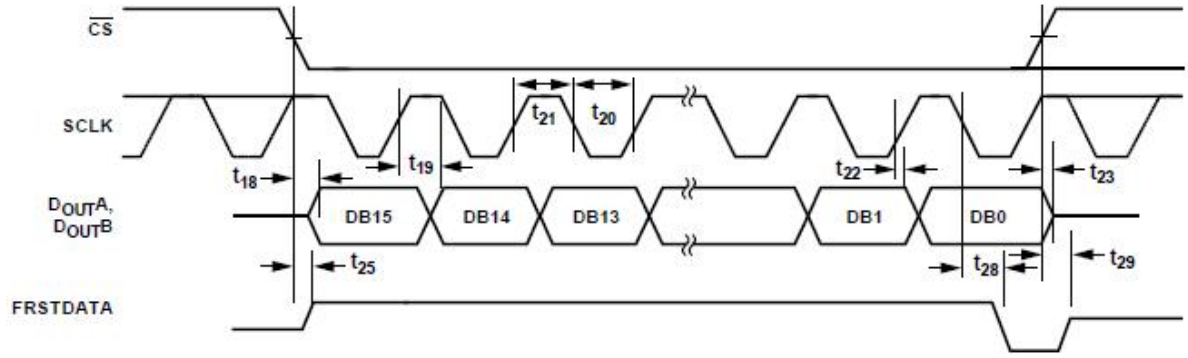


Figure 6. Serial Read Operation (Channel 1)

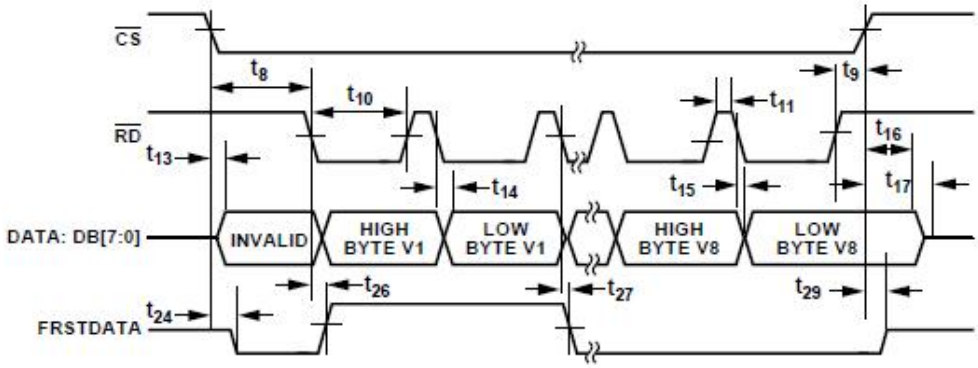


Figure 7. BYTE Mode Read Operation

## Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| $AV_{CC}$ to AGND | −0.3 V to +7 V |
| $V_{DRIVE}$ to AGND | −0.3 V to $AV_{CC}$+0.3 V |
| Analog Input Voltage to AGND[1] | ±16.5 V |
| Digital Input Voltage to AGND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| Digital Output Voltage to AGND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| REFIN to AGND | −0.3 V to $AV_{CC}$ + 0.3 V |

| | |
|---|---|
| Input Current to Any Pin Except Supplies1 | ±10 mA |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| Pb/SN Temperature, Soldering Reflow (10 sec to 30 sec) | 240 (+0)°C |
| Pb-Free Temperature, Soldering Reflow | 260 (+0)°C |
| ESD (All Pins Except Analog Inputs) | 2 kV |
| ESD (Analog Input Pins Only) | 7 kV |

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**THERMAL RESISTANCE**: $\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. These specifications apply to a 4-layer board.

| Package Type | θ JA | θ JC | Unit |
|---|---|---|---|
| 64-Lead LQFP | 45 | 11 | **(°C/W)[1]** |

## Pin Description

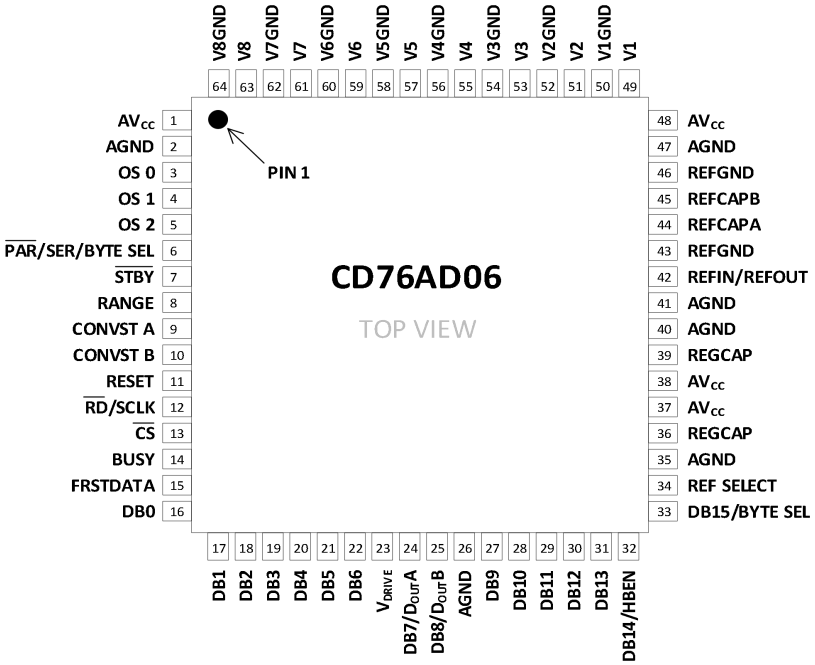


Figure 8. Pin Configuration, Top View

Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1,37,38,48 | $AV_{CC}$ | Analog Supply Voltage, 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. These supply pins should be decoupled to AGND. |
| 2,26,35,40,41,47 | AGND | Analog Ground. These pins are the ground reference points for all analog circuitry on the CD76AD06. All analog input signals and external reference signals should be referred to these pins. All six of these AGND pins should connect to the AGND plane of a system. |
| 5,4,3 | OS [2:0] | Oversampling Mode Pins. Logic inputs. These inputs are used to select the oversampling ratio. OS 2 is the MSB control bit, and OS 0 is the LSB control bit. See the Digital Filter section for more details about the oversampling mode of operation and Table 5 for oversampling bit decoding. |
| 6 | $\overline{PAR}$/SER/ BYTE SEL | Parallel/Serial/Byte Interface Selection Input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. Parallel byte interface mode is selected when this pin is logic high and DB15/BYTE |

| | | |
|---|---|---|
| | | SEL is logic high (see Table 4).In serial mode, the $\overline{RD}$/SCLK pin functions as the serial clock input. The DB7/DOUTA pin and the DB8/DOUTB pin function as serial data outputs. When the serial interface is selected, the DB[15:9] and DB[6:0] pins should be tied to ground. In byte mode, DB15, in conjunction with $\overline{PAR}$/SER/BYTE SEL, is used to select the parallel byte mode of operation (see Table 4). DB14 is used as the HBEN pin. DB[7:0] transfer the 16-bit conversion results in two $\overline{RD}$ operations, with DB0 as the LSB of the data transfers. |
| 7 | $\overline{STBY}$ | Standby Mode Input. This pin is used to place the CD76AD06 into one of two power-down modes: standby mode or shutdown mode. The power-down mode entered depends on the state of the RANGE pin, as shown in Table 3. When in standby mode, all circuitry, except the on-chip reference, regulators, and regulator buffers, is powered down. When in shutdown mode, all circuitry is powered down. |
| 8 | RANGE | Analog Input Range Selection. Logic input. The polarity on this pin deter-mines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ±10 V for all channels. If this pin is tied to a logic low, the analog input range is ±5 V for all channels. A logic change on this pin has an immediate effect on the analog input range. Changing this pin during a conversion is not recommended for fast throughput rate applications. See the Analog Input section for more information. |
| 9,10 | CONVST A, CONVST B | Conversion Start Input A, Conversion Start Input B. Logic inputs. These logic inputs are used to initiate conversions on the analog input channels.<br>For simultaneous sampling of all input channels, CONVST A and CONVST B can be shorted together, and a single convert start signal can be applied.<br>Alternatively, CONVST A can be used to initiate simultaneous sampling: V1, V2, V3, and V4 for the CD76AD06; CONVST B can be used to initiate simultaneous sampling on the other analog inputs: V5, |

| | | |
|---|---|---|
| | | V6, V7, and V8 for the CD76AD06; This is possible only when oversampling is not switched on. When the CONVST A or CONVST B pin transitions from low to high, the front-end track-and-hold circuitry for the respective analog inputs is set to hold. |
| 11 | RESET | Reset Input. When set to logic high, the rising edge of RESET resets the CD76AD06. The device should receive a RESET pulse directly after power-up. The RESET high pulse should typically be 50 ns wide. If a RESET pulse is applied during a conversion, the conversion is aborted. If a RESET pulse is applied during a read, the contents of the output registers reset to all zeros. |
| 12 | $\overline{RD}$/SCLK | Parallel Data Read Control Input When the Parallel Interface Is Selected ($\overline{RD}$)/ Serial Clock Input When the Serial Interface Is Selected (SCLK). When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the output bus is enabled. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{CS}$ falling edge takes the DOUTA and DOUTB data output lines out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the DOUTA and DOUTB serial data outputs. For more information, see the Conversion Control section. |
| 13 | $\overline{CS}$ | Chip Select. This active low logic input frames the data transfer. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode, the DB[15:0] output bus is enabled and the conversion result is output on the parallel data bus lines.<br>In serial mode, $\overline{CS}$ is used to frame the serial read transfer and clock out the MSB of the serial output data. |
| 14 | BUSY | Busy Output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of BUSY |

| | | |
|---|---|---|
| | | signals that the conversion data is being latched into the output data registers and is available to read after a Time t4. Any data read while BUSY is high must be completed before the falling edge of BUSY occurs. Rising edges on CONVST A or CONVST B have no effect while the BUSY signal is high. |
| 15 | FRSTDATA | Digital Output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on the parallel, byte, or serial interface. When the $\overline{CS}$ input is high, the FRSTDATA output pin is in three-state. The falling edge of $\overline{CS}$ takes FRSTDATA out of three-state. In parallel mode, the falling edge of $\overline{RD}$ corresponding to the result of V1 then sets the FRSTDATA pin high, indicating that the result from V1 is available on the output data bus. The FRSTDATA output returns to a logic low following the next falling edge of $\overline{RD}$. In serial mode, FRSTDATA goes high on the falling edge of $\overline{CS}$ because this clocks out the MSB of V1 on DOUTA. It returns low on the 16th SCLK falling edge after the $\overline{CS}$ falling edge. See the Conversion Control section for more details. |
| 22 to 16 | DB[6:0] | Parallel Output Data Bits, DB6 to DB0. When $\overline{PAR}$ /SER/BYTE SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB6 to DB0 of the conversion result. When $\overline{PAR}$ /SER/BYTE SEL = 1, these pins should be tied to AGND. When operating in parallel byte interface mode, DB[7:0] outputs the 16-bit con-version result in two $\overline{RD}$ operations. DB7 (Pin 24) is the MSB; DB0 is the LSB. |
| 23 | $V_{DRIVE}$ | Logic Power Supply Input. The voltage (2.3 V to 5.25 V) |

| | | |
|---|---|---|
| | | supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (that is, DSP and FPGA). |
| 24 | DB7/DOUTA | Parallel Output Data Bit 7 (DB7)/Serial Interface Data Output Pin (DOUTA). When $\overline{PAR}$/SER/BYTE SEL = 0, this pins acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB7 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, this pin functions as DOUTA and outputs serial conversion data (see the Conversion Control section for more details). When operating in parallel byte mode, DB7 is the MSB of the byte. |
| 25 | DB8/DOUTB | Parallel Output Data Bit 8 (DB8)/Serial Interface Data Output Pin (DOUTB).When $\overline{PAR}$/SER/BYTE SEL = 0, this pin acts as a three-state parallel digital input/output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB8 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, this pin functions as DOUTB and outputs serial conversion data (see the Conversion Control section for more details). |
| 31 to 27 | DB[13:9] | Parallel Output Data Bits, DB13 to DB9. When $\overline{PAR}$/SER/BYTE SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{CS}$ and $\overline{RD}$ are low, these pins are used to output DB13 to DB9 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, these pins should be tied to AGND. |
| 32 | DB14/ HBEN | Parallel Output Data Bit 14 (DB14)/High Byte Enable (HBEN). When $\overline{PAR}$/ SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{CS}$ and |

| | | |
|---|---|---|
| | | $\overline{RD}$ are low, this pin is used to output DB14 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1, the CD76AD06 operate in parallel byte interface mode. In parallel byte mode, the HBEN pin is used to select whether the most significant byte (MSB) or the least significant byte (LSB) of the conversion result is output first.When HBEN = 1, the MSB is output first, followed by the LSB. When HBEN = 0, the LSB is output first, followed by the MSB.In serial mode, this pin should be tied to GND. |
| 33 | DB15/ BYTE SEL | Parallel Output Data Bit 15 (DB15)/Parallel Byte Mode Select (BYTE SEL). When $\overline{PAR}$/SER/BYTE SEL = 0, this pin acts as a three-state parallel digital output pin. When $\overline{CS}$ and $\overline{RD}$ are low, this pin is used to output DB15 of the conversion result. When $\overline{PAR}$/SER/BYTE SEL = 1, the BYTE SEL pin is used to select between serial interface mode and parallel byte interface mode (see Table 4). When $\overline{PAR}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 0, the CD76AD06 operates in serial interface mode. When $\overline{PAR}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1, the CD76AD06 operates in parallel byte interface mode. |
| 34 | REF SELECT | Internal/External Reference Selection Input. Logic input. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. |
| 36,39 | REGCAP | Decoupling Capacitor Pin for Voltage Output from Internal Regulator.These output pins should be decoupled separately to AGND using a 1 μF capacitor. The voltage on these pins is in the range of 2.5 V to 2.7 V. |
| 42 | REFIN/REFOUT | Reference Input (REFIN)/Reference Output (REFOUT). The on-chip reference of 2.5 V is available on this pin for external use if the REF SELECT pin is set to logic high. |

| | | |
|---|---|---|
| | | Alternatively, the internal reference can be disabled by setting the REF SELECT pin to logic low, and an external reference of 2.5 V can be applied to this input (see the Internal/External Reference section). Decoupling is required on this pin for both the internal and external reference options. A 10 µF capacitor should be applied from this pin to ground close to the REFGND pins. |
| 43,46 | REFGND | Reference Ground Pins. These pins should be connected to AGND. |
| 44,45 | REFCAPA, REFCAPB | Reference Buffer Output Force/Sense Pins. These pins must be connected together and decoupled to AGND using a low ESR, 10 µF ceramic capacitor. The voltage on these pins is typically 4.5 V. |
| 49 | V1 | Analog Input. This pin is a single-ended analog input. The analog input range of this channel is determined by the RANGE pin. |
| 50,52 | V1GND, V2GND | Analog Input Ground Pins. These pins correspond to Analog Input Pin V1 and Analog Input Pin V2. All analog input AGND pins should connect to the AGND plane of a system. |
| 51 | V2 | Analog Input. This pin is a single-ended analog input. The analog input range of this channel is determined by the RANGE pin. |
| 53 | V3 | Analog Input 3.this is an AGND pin. |
| 54 | V3GND | Analog Input Ground Pin.this is an AGND pin. |
| 55 | V4 | Analog Input 4.this is an AGND pin. |
| 56 | V4GND | Analog Input Ground Pins. All analog input AGND pins should connect to the AGND plane of a system. |
| 57 | V5 | Analog Inputs. These pins are single-ended analog inputs. The analog input range of these channels is determined by the RANGE pin. |
| 58 | V5GND | Analog Input Ground Pins. All analog input AGND pins should connect to the AGND plane of a system. |
| 59 | V6 | Analog Inputs. These pins are single-ended analog inputs. |
| 60 | V6GND | Analog Input Ground Pins. All analog input AGND pins should connect to the AGND plane of a system. |
| 61 | V7 | Analog Input Pin. this is an AGND pin. |

| | | |
|---|---|---|
| 62 | V7GND | Analog Input Ground Pin. this is an AGND pin. |
| 63 | V8 | Analog Input Pin. this is an AGND pin. |
| 64 | V8GND | Analog Input Ground Pin. this is an AGND pin. |

## Performance Parameter Characteristics

Temperature range is from −40°C to +85°C. The CD76AD06 is functional up to 105°C with throughput rates < 160 kSPS. Specifications are guaranteed for the operating temperature range of −0°C to +85°C only.

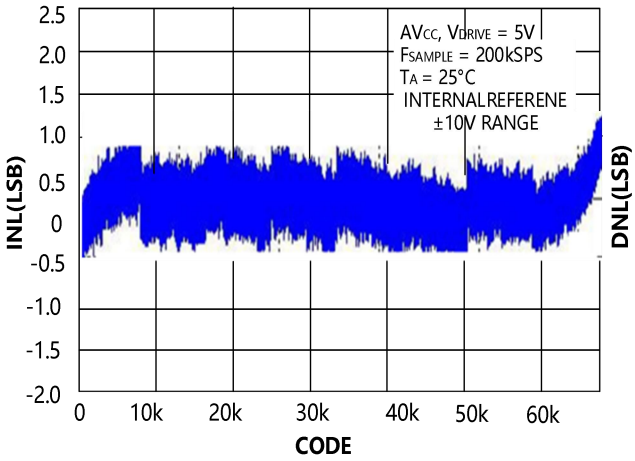


Figure 9. CD76AD06 Typical INL, ±10 V Range

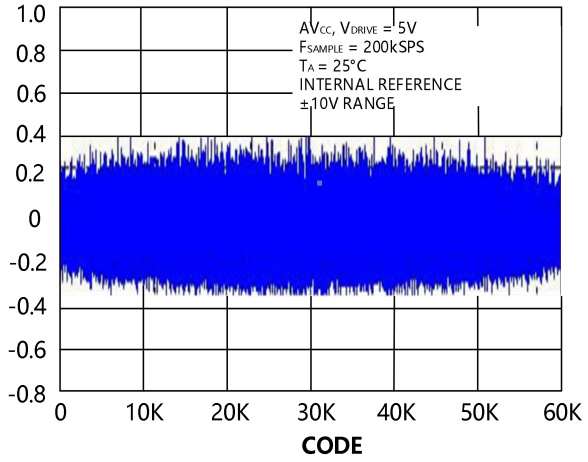


Figure 10. CD76AD06 Typical DNL, ±10 V Range

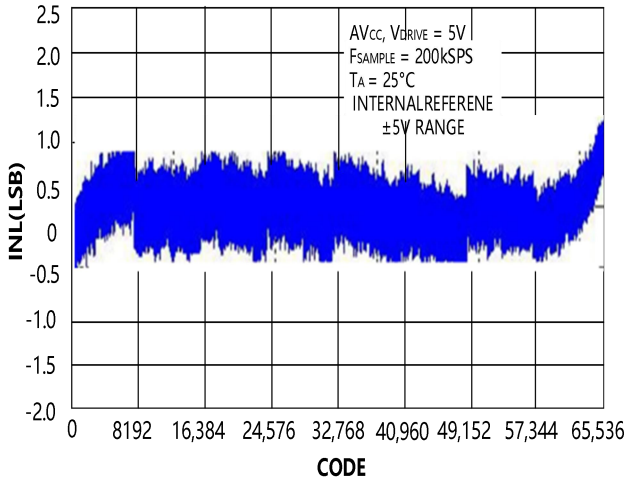


Figure 11.CD76AD06 Typical INL, ±5V Range

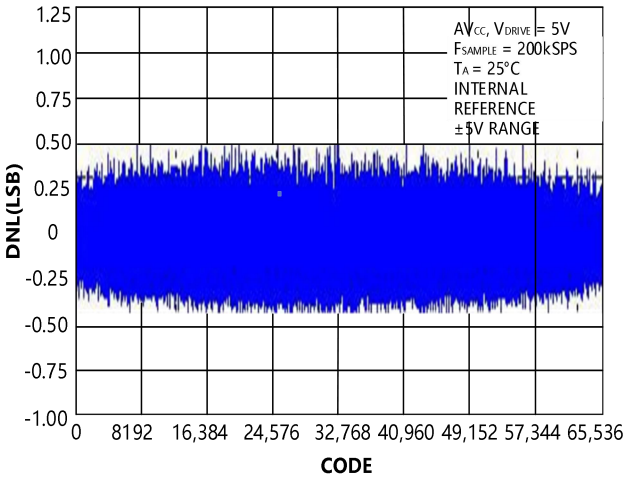


Figure 12.CD76AD06 Typical DNL, ±5 V Range

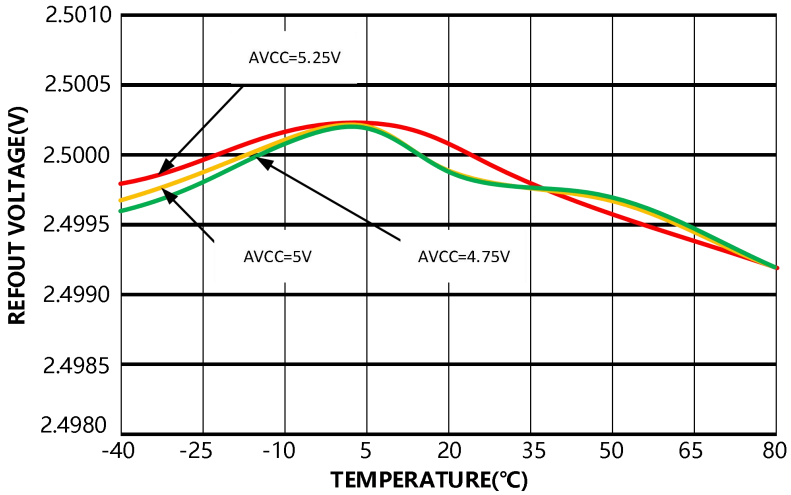


Figure 13.Reference Output Voltage vs. Temperature for Different Supply Voltages

## Application Information

### INTERNAL/EXTERNAL REFERENCE

The CD76AD06 contain an on-chip 2.5 V band gap reference. The REFIN/REFOUT pin allows access to the 2.5 V reference that generates the on-chip 4.5 V reference internally, or it allows an external reference of 2.5 V to be applied to the CD76AD06. An externally applied reference of 2.5 V is also gained up to 4.5 V, using the internal buffer. This 4.5 V buffered reference is the reference used by the SAR ADC.

The REF SELECT pin is a logic input pin that allows the user to select between the internal reference and an external reference. If this pin is set to logic high, the internal reference is selected and enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After a reset, the CD76AD06 operate in the reference mode selected by the REF SELECT pin. Decoupling is required on the REFIN/REFOUT pin for both the internal and external reference options. A 10 μF ceramic capacitor is required on the REFIN/REFOUT pin.

The CD76AD06 contain a reference buffer configured to gain the REF voltage up to ~4.5 V, as shown in Figure 14. The REFCAPA and REFCAPB pins must be shorted together externally, and a ceramic capacitor of 10 μ F applied to REFGND, to ensure that the reference buffer is in closed-loop operation. The reference voltage available at the REFIN/REFOUT pin is 2.5 V.

When the CD76AD06 are configured in external reference mode, the REFIN/REFOUT pin is a high input impedance pin. For applications using multiple CD76AD06 devices, the following configurations are recommended, depending on the application requirements.

**External Reference Mode**

One ADR421 external reference can be used to drive the REFIN/REFOUT pins of all CD76AD06 devices (see Figure 15). In this configuration, each REFIN/REFOUT pin of the CD76AD06 should be decoupled with at least a 100 nF decoupling capacitor.

Internal Reference Mode One CD76AD06 device, configured to operate in the internal reference mode, can be used to drive the remaining CD76AD06 devices, which are configured to operate in external reference mode (see Figure 16). The REFIN/ REFOUT pin of the CD76AD06, configured in internal reference mode, should be decoupled using a 10 μF ceramic decoupling capacitor. The other CD76AD06 devices, configured in external reference mode, should use at least a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

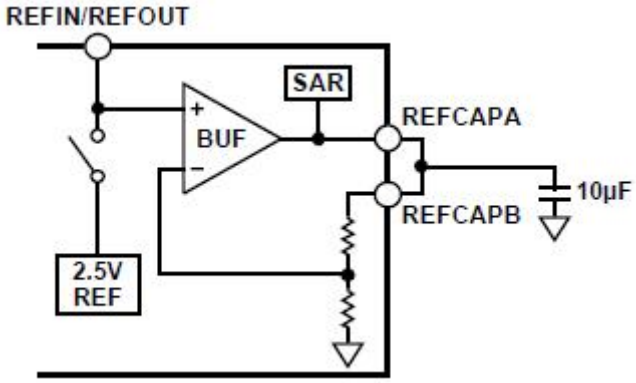


Figure 14. Reference Circuitry

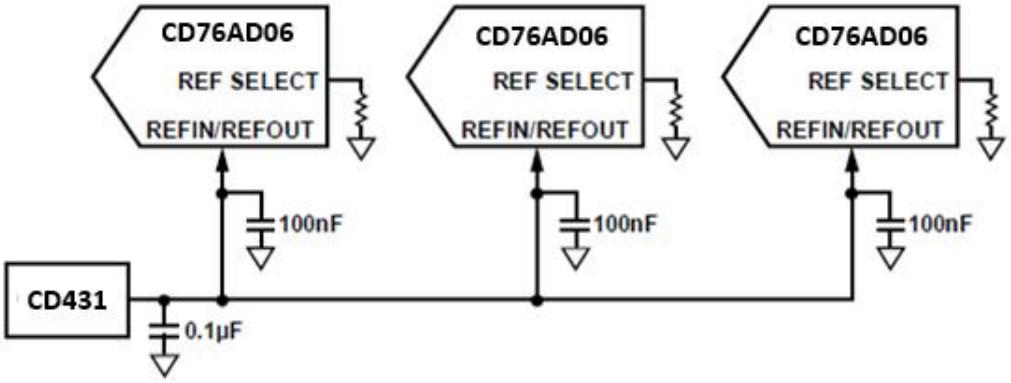


Figure 15. Single External Reference Driving Multiple CD76AD06 REFIN Pins

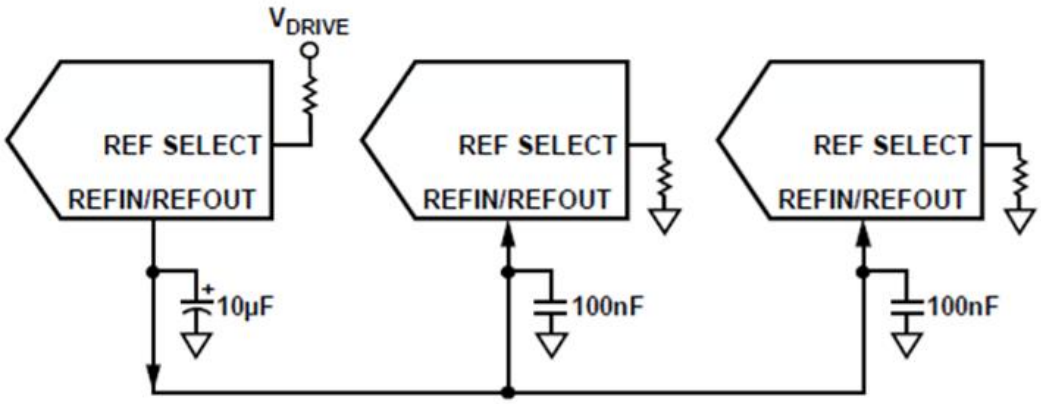


Figure 16. Internal Reference Driving Multiple CD76AD06 REFIN Pins

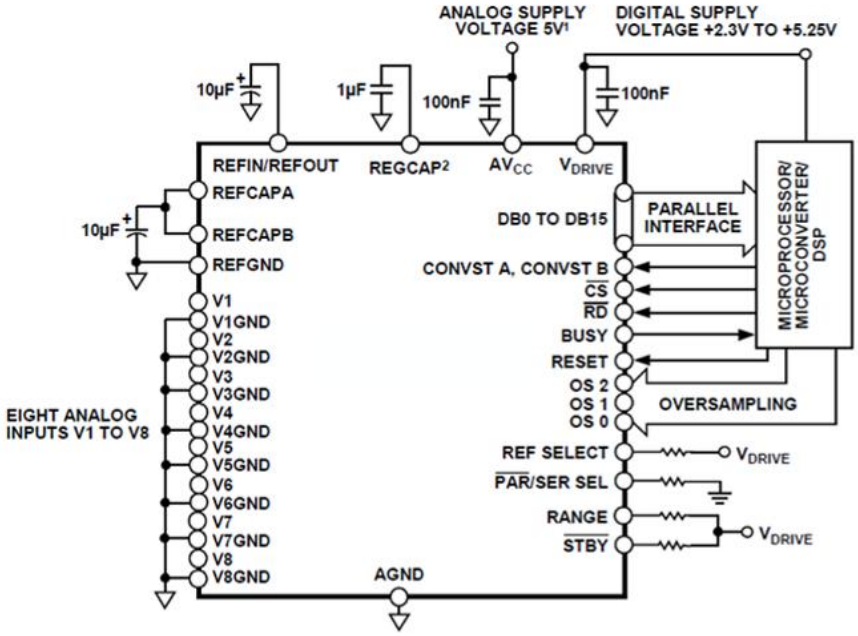


Figure 17. CD76AD06 Typical Connection Diagram

Figure 17 shows the typical connection diagram for the CD76AD06. There are four AVCC supply pins on the part, and each of the four pins should be decoupled using a 100 nF capacitor at each supply pin and a 10µF capacitor at the supply source. The CD76AD06 can operate with the internal reference or an externally applied reference. In this configuration, the CD76AD06 is configured to operate with the internal reference. When using a singleCD76AD06 device on the board, the REFIN/REFOUT pin should be decoupled with a 10 µF capacitor. Refer to the Internal/External Reference section when using an application with multiple CD76AD06 devices. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 µF ceramic capacitor.

The VDRIVE supply is connected to the same supply as the processor. The VDRIVE voltage controls the voltage value of the output logic signals. For layout, decoupling, and grounding hints, see the Layout Guidelines section.After supplies are applied to the CD76AD06,a reset should be applied to the CD76AD06 to ensure that it is configured for the correct mode of operation.

## POWER-DOWN MODES

Two power-down modes are available on the CD76AD06: standby mode and shutdown mode. The $\overline{\text{STBY}}$ pin controls whether the CD76AD06 is in normal mode or in one of the two power-down modes.

The power-down mode is selected through the state of the RANGE pin when the $\overline{\text{STBY}}$ pin is low. Table 3 shows the configurations required to choose the desired power-down mode. When the CD76AD06 is placed in standby mode, the current consumption is 8 mA maximum and power-up time is approximately 100 µs because the capacitor on the REFCAPA and REFCAPB pins must charge up. In standby mode, the on-chip reference and regulators remain powered up, and the amplifiers and ADC core are powered down.

When the CD76AD06 is placed in shutdown mode, the current consumption is 6 µA maximum and power-up time is approximately 13ms (external reference mode). In shut-down mode, all circuitry is powered down. When the CD76AD06 ispowered up from shutdown mode, a RESET signal must be applied to theCD76AD06 after the required power-up time has elapsed.

Table 3. Power-Down Mode Selection

| Power-Down Mode | $\overline{\text{STBY}}$ | RANGE |
|---|---|---|
| Standby | 0 | 1 |
| Shutdown | 0 | 0 |

## CONVERSION CONTROL

### Simultaneous Sampling on All Analog Input Channels

The CD76AD06 allow simultaneous sampling of all analog input channels. All channels are sampled simul-taneously when both CONVST pins (CONVST A, CONVST B) are tied together. A single CONVST signal is used to control both CONVST x inputs. The rising edge of this common CONVST signal initiates simultaneous sampling on all analog input channels.

The CD76AD06 contains an on-chip oscillator that is used to perform the conversions. The conversion time for all ADC channels is tCONV. The BUSY signal indicates to the user when conversions are in progress, so when the rising edge of CONVST is applied, BUSY goes logic high and transitions low at the end of the entire conversion process. The falling edge of the BUSY

signal is used to place all eight track-and-hold amplifiers back into track mode. The falling edge of BUSY also indicates that the new data can now be read from the parallel bus (DB[15:0]), the DOUTA and DOUTB serial data lines, or the parallel byte bus, DB[7:0].

**Simultaneously Sampling Two Sets of Channels**

The CD76AD06 also allow the analog input channels to be sampled simultaneously in two sets. This can be used in power-line protection and measurement systems to compensate for phase differences introduced by PT and CT transformers. In a 50 Hz system, this allows for up to 9° of phase compensation; and in a 60 Hz system, it allows for up to 10° of phase compensation.

This is accomplished by pulsing the two CONVST pins independently and is possible only if oversampling is not in use. CONVST A is used to initiate simultaneous sampling of the first set of channels (V1 to V4 for the CD76AD06); and CONVST B is used to initiate simultaneous sampling on the second set of analog input channels (V5 to V8 for the CD76AD06), as illustrated in Figure 18. On the rising edge of CONVST A, the track-and-hold amplifiers for the first set of channels are placed into hold mode. On the rising edge of CONVST B, the track-and-hold amplifiers for the second set of channels are placed into hold mode. The conversion process begins once both rising edges of CONVST x have occurred; therefore BUSY goes high on the rising edge of the later CONVST x signal. In Timing Specification, Time t5 indicates the maximum allowable time between CONVST x sampling points.

There is no change to the data read process when using two separate CONVST x signals.Connect all unused analog input channels to AGND. The results for any unused channels are still included in the data read because all channels are always converted.

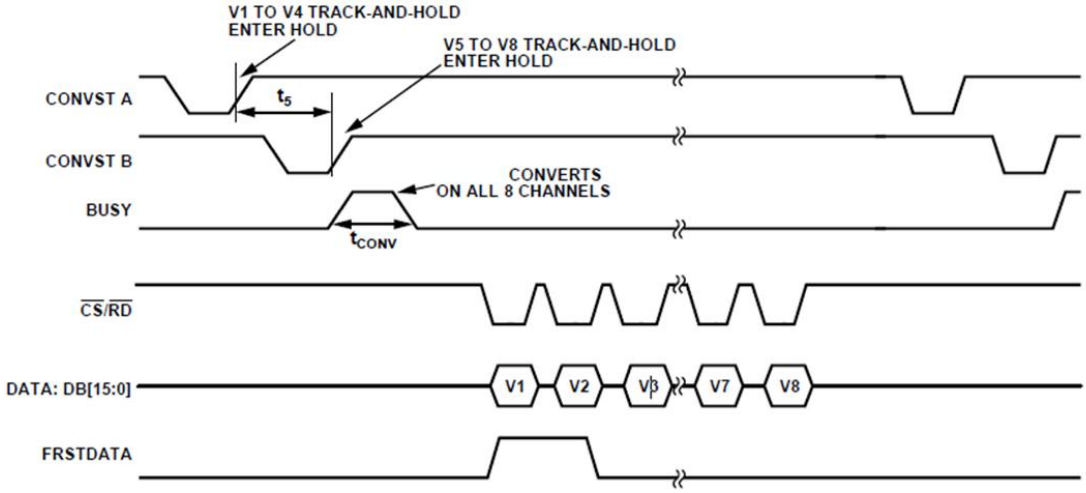


Figure 18. CD76AD06 Simultaneous Sampling on Channel Sets While Using Independent CONVST A and CONVST B Signals—Parallel Mode

## DIGITAL INTERFACE

The CD76AD06 provide three interface options: a parallel interface, a high speed serial interface, and a parallel byte interface. The required interface mode is selected via the $\overline{PAR}$/SER/BYTE SEL and DB15/BYTE SEL pins.

Table 4. Interface Mode Selection

| $\overline{PAR}$ /SER/BYTE SEL | DB15 | Interface Mode |
|---|---|---|
| 0 | 0 | Parallel interface mode |
| 1 | 0 | Serial interface mode |
| 1 | 1 | Parallel byte interface mode |

Table 5. Oversample Bit Decoding

| OS[2:0] | OS Ratio | SNR 5 V Range (dB) | SNR 10V Range (dB) | 3 dB BW 5 V Range (kHz) | 3 dB BW 10 V Range (kHz) | Maximum Throughput CONVST Frequency (kHz) |
|---|---|---|---|---|---|---|
| 000 | No OS | 89 | 90 | 15 | 22 | 200 |
| 001 | 2 | 91.2 | 92 | 15 | 22 | 100 |
| 010 | 4 | 92.6 | 93.6 | 13.7 | 18.5 | 50 |
| 011 | 8 | 94.2 | 95 | 10.3 | 11.9 | 25 |
| 100 | 16 | 95.5 | 96 | 6 | 6 | 12.5 |
| 101 | 32 | 96.4 | 96.7 | 3 | 3 | 6.25 |
| 110 | 64 | 96.9 | 97 | 1.5 | 1.5 | 3.125 |
| 111 | Invalid | -- | -- | -- | -- | -- |

## Package Outline Dimensions

**LQFP-64**

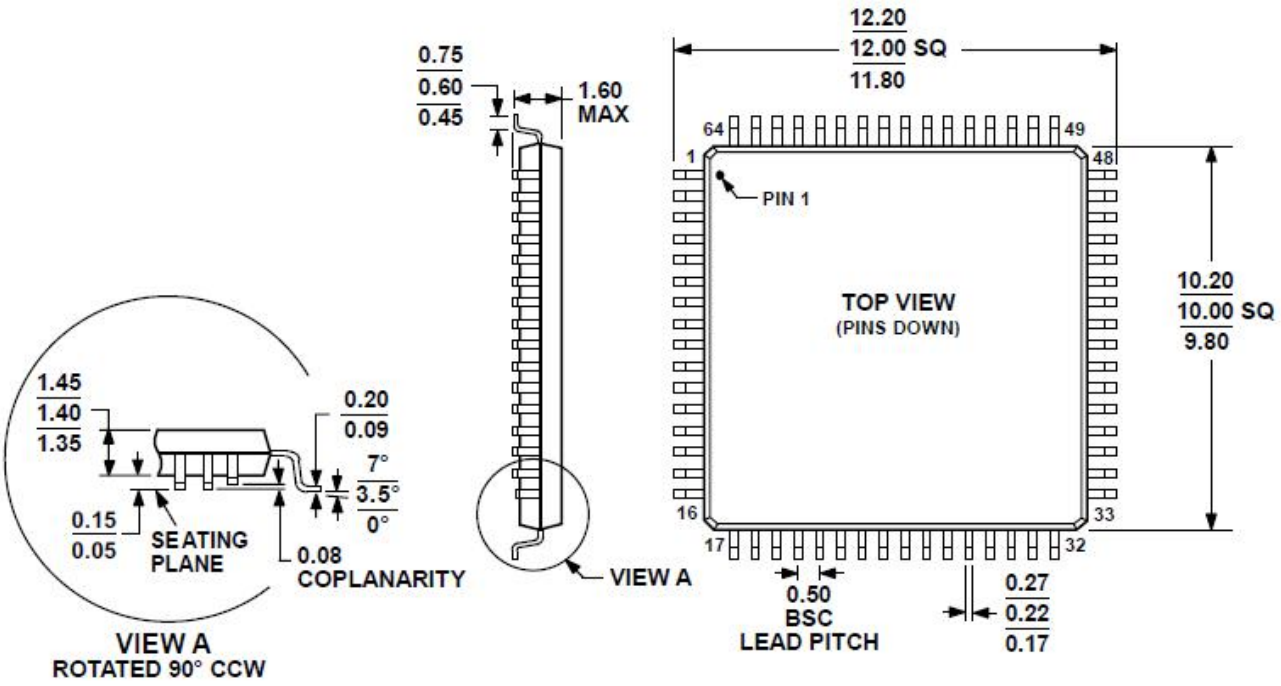


Figure 19.64-Lead Low Profile Quad Flat Package [LQFP]

## Package/Ordering Information

| MODEL | TEMPERATURE | PACKAGE DESCRIPTION | PACKAGE OPTION |
|---|---|---|---|
| **CD76AD06Q** | -40℃-85℃ | LQFP-64 | Tray, 60 |



Chinese version:CD76AD06

## Revision Log

| Version | Revision date | Change content | Reason for Change | Modified by | Reviewed By | Note |
|---|---|---|---|---|---|---|
| V1.0 | 2025.5.20 | Initial version | Regular update | WW | LYL | |
| V1.0 | 2025.6.12 | Update the product pin description and functional block diagram. | Error update | WW | LYL | |