CoreadDvices
承芯微电子

CDG601

SPST Switch

Version: Rev 1.0.0 Date: 2025-10-23

Features

- Low on resistance, 3.3 Ω maximum
- Low on resistance flatness (0.5 Ω Typ)
- Dual ±2.7 V to ±5.5 V or single +2.7 V to
- Rail-to-rail operation
- Low power consumption
- TTL/CMOS compatible

Application

- Automatic test equipment
- Power routing
- Communication systems
- Data acquisition systems
- Sample-and-hold systems
- Avionics
- Relay replacement
- Battery-powered systems

Description

The CBMG601 are monolithic, CMOS single-pole single throw (SPST) switches with on resistance typically less than 3.3 Ω. The low on-resistance flatness makes the CBMG601 ideally suited to many applications, particularly those requiring low distor tion. These switches are ideal replacements for mechanical relays because they are more reliable, have lower power requirements, and are available in much smaller package sizes. The CBMG601 is a normally open (NO) switch.Each switch conducts equally well in both directions when the device is on, with the input signal range extending to the supply rails. The switches are available in tiny, 6-lead SOT-23; 8-lead MSOP;

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Product Highlights

1. Low on resistance (2 Ω typical) On
2. Dual ±2.7 V to ±5.5 V or single +2.7 V to +5.5 V supplies
3. Tiny, 6-lead SOT-23; 8-lead MSOP
4. Rail-to-rail input signal range

Pin Configurations

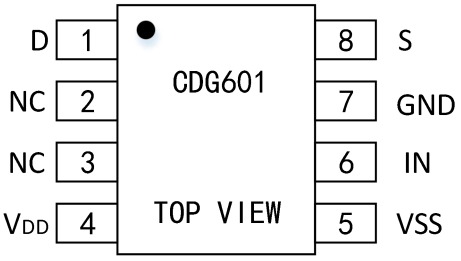


Figure 1. MSOP8 Pin Configuration

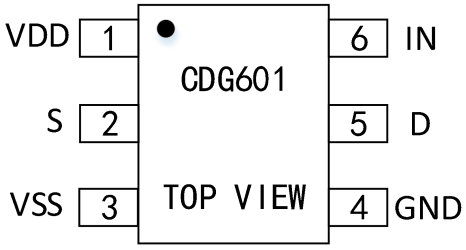


Figure 2. SOT23-6 Pin Configuration

Pin Description

Pin No.		Mnemonic	Description
MSOP-8	SOT23-6		
4	1	VDD	Most Positive Power Supply Potential.
8	2	S	Source Terminal. Can be an input or output.
5	3	VSS	Most Negative Power Supply Potential.
7	4	GND	Ground (0 V) Reference.
1	5	D	Drain Terminal. Can be an input or output.
6	6	IN	Logic Control Input.
2,3	N/A	NC	No Connect.

Functional Block diagram

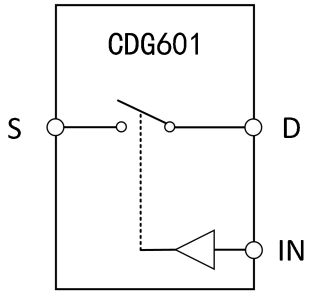


Figure 3.Switches shown for a logic "0" input

Truth Table

CBMG601 In	Switch Condition
0	OFF
1	ON

Absolute Maximum Ratings

Parameter	Rating
V_{DD} to VSS	13V
V_{DD} to GND	−0.3V to +6.5V
V_{SS} to GND	−0.3 V to -6.5 V
Analog Inputs1	−0.3V to VDD + 0.3V
Digital Inputs1	−0.3 V to VDD + 0.3 V or 30 mA
Peak Current, S or D	200 mA(Pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	100mA
Operating Temperature Range	−40°Cto+85°C
Storage Temperature Range	−65°Cto+150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
θ_{JA} Thermal Impedance	229.6°C/W
θ_{JC} Thermal Impedance	91.99°C/W

Lead Temperature, Soldering 10 sec	300°C
IR Reflow, Peak Temperature	260°C
ESD	2 kV

Electrical Characteristics

VDD = +5 V±10%, GND =VSS= 0 V. All specifications −40°C to +85°C, unless otherwise noted.

Table 3.

PARAMETER	+25°C			−40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				0V to V_{DD}				V
On Resistance (R_{ON})	--	3.5	5.5	--	--	8	VDD = 4.5 V,VS = 0 V to 4.5 V, IDS = −10 mA;	Ω
On Resistance Flatness (RFLAT(ON))	--	0.2	--	--	0.2	0.75	VS = 1.5 V to 3.3 V, IDS = −10 mA	Ω
Leakage Currents							V_{DD}=+5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	± 0.25	--	--	±1	V_S=4.5V/1V, V_D=1V/4.5V;	nA
Drain Off Leakage ID (Off)	--	± 0.01	± 0.25	--	--	±1	V_S=4.5V/1V, V_D=1V/4.5V;	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	± 0.25	--	--	±1	V_S=V_D=1V, or 4.5V;	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	110	220	--	--	280	R_L=300 Ω,C_L=35pF,V_S=3.3V	ns
t_{OFF}	--	50	80	--	--	110	R_L=300 Ω,C_L=35pF,V_S=3.3V	ns
Charge Injection	--	20	--	--			V_S=0V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-60	--	--			R_L=50Ω, C_L=5pF, f=10MHz	dB
Bandwidth −3 dB	--	180	--	--			R_L=50Ω, C_L=5pF;	MHz

C_S (OFF)	--	50	--	--			f=1MHz	pF
C_D(OFF)	--	50	--	--			f=1MHz	pF
C_D, C_S (On)	--	38	--	--			f=1MHz	pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+5.5V, Digital inputs=0V or 5V	μA

VDD = 5 V ± 10%, VSS = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 4.

PARAMETER	+25℃			-40° C to +85° C			Test Conditions	UNIT
	Min	Typ	Max	Min	Typ	Max		
Analog Switch								
Analog Signal Range				VSS to V_{DD}				V
On Resistance (R_{ON})	--	2	3.3	--	--	5.5	VDD = +4.5 V,VSS=-4.5V VS = ± 4.5V, IDS = − 10 mA;	Ω
On Resistance Flatness (RFLAT(ON))	--	0.2	--	--	0.2	0.75	VS =±3.3V, IDS = −10 mA;	Ω
Leakage Currents							V_{DD}=+5.5V, VSS=-5.5V	
Source Off Leakage I_S (Off)	--	± 0.01	± 0.25	--	--	±1	V_S=+4.5V/-4.5V, V_D=-4.5V/+4.5V;	nA
Drain Off Leakage ID (Off)	--	± 0.01	± 0.25	--	--	±1	V_D=-4.5V/+4.5V;	nA
Channel On Leakage I_D, I_S (On)	--	± 0.01	± 0.25	--	--	±1	V_S=V_D=+4.5V or -4.5V;	nA
Digital Inputs								
Input High Voltage, V_{INH}				2.4	--	--		V
Input Low Voltage, V_{INL}				--	--	0.8		V
Input Current IINL or I_{INH}	--	0.005	--	--	--	±0.1	V_{IN}=V_{INL} or V_{INH}	μA
Dynamic Characteristics								
t_{ON}	--	80	120	--	--	155	R_L=300 Ω,C_L=35pF,V_S=3.3V	ns
t_{OFF}	--	45	75	--	--	90	R_L=300 Ω,C_L=35pF,V_S=3.3V	ns
Charge Injection	--	250	--	--			V_S=0V; R_S=0Ω, C_L=1nF;	pC
Off Isolation	--	-60	--	--			R_L=50Ω, C_L=5pF, f=1MHz	dB
Bandwidth −3 dB	--	180	--	--			R_L=50Ω, C_L=5pF;	MHz
C_S (OFF)	--	50	--	--			f=1MHz	pF

C_D(OFF)	--	50	--	--			f=1MHz	pF
C_D, C_S (On)	--	145	--	--			f=1MHz	pF
Power Requirements								
I_{DD}	--	0.001	--	--	--	1.0	V_{DD}=+5.5V, V_{SS}=-4.5,Digital inputs=0V or 5V	μA

Typical Characteristics

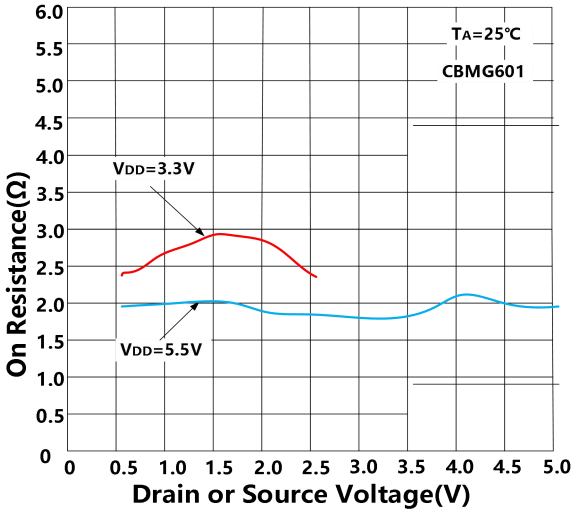
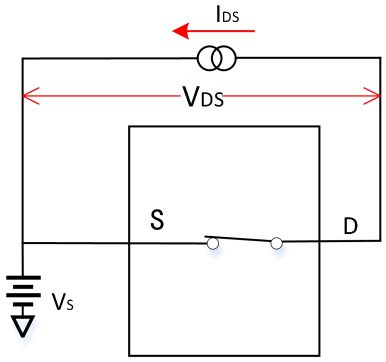


Figure 4.On Resistance vs. V_D (V_S)-(CBMG601)

Test Circuit



RON=V_{DS}/I_{DS}

Figure 5. On Resistance

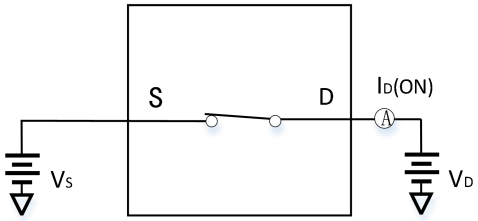


Figure 6. On Leakage

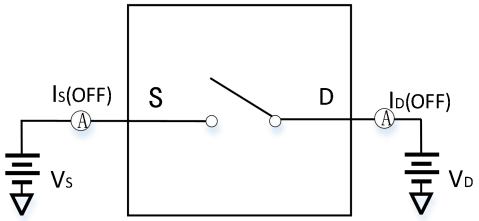


Figure 7. Off Leakage

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Package Outline Dimensions

MSOP-8

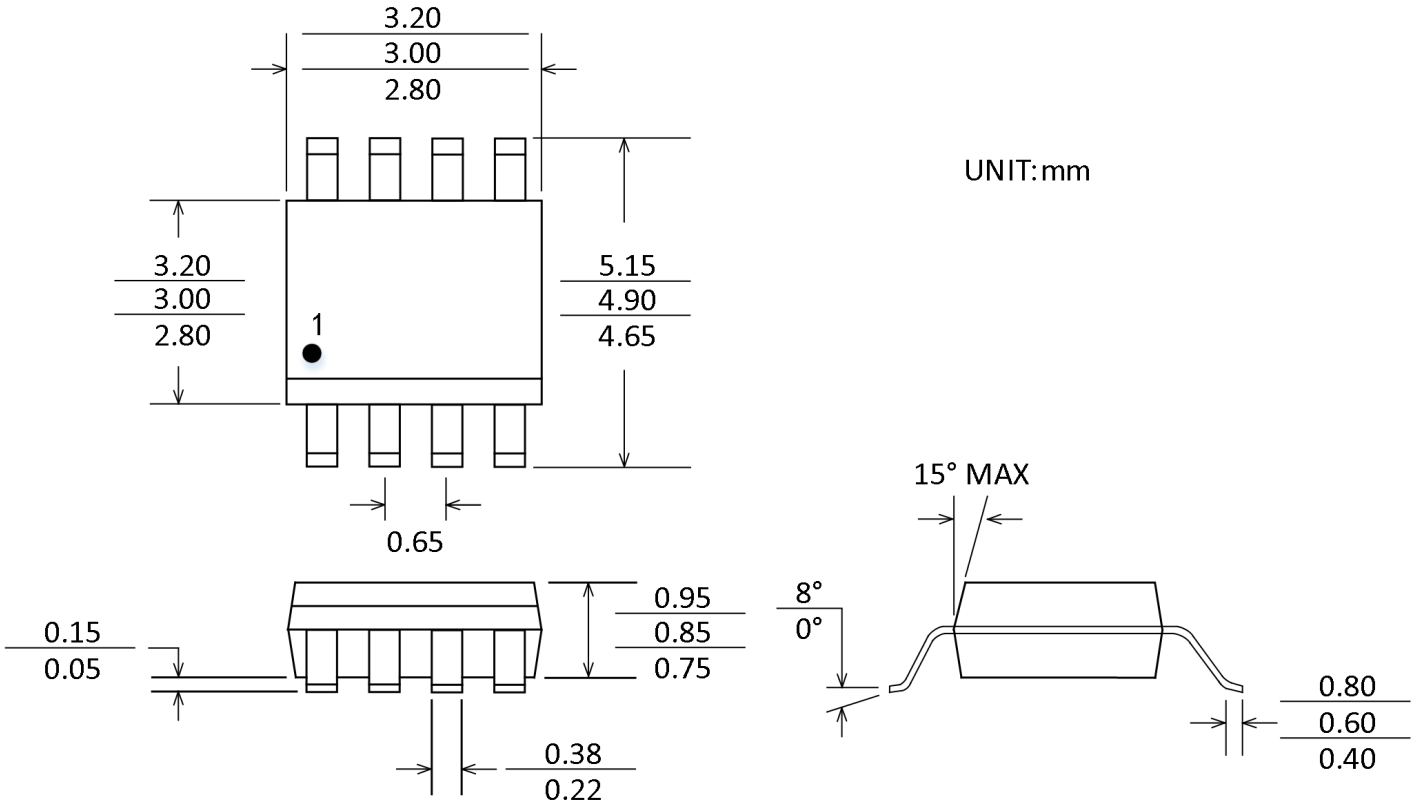

Figure 8. 8-Lead Mini Small Outline Package [MSOP]

Chinese version:CDG601

SOT23-6

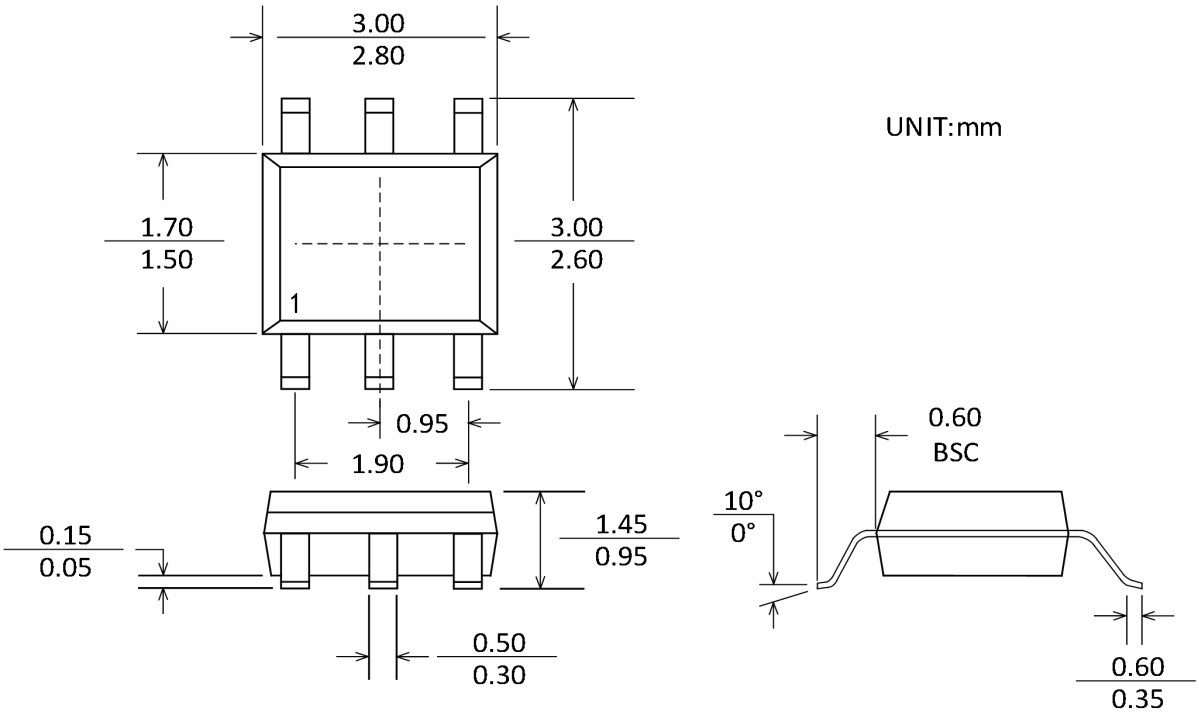

Figure 9. 6-Lead Small Outline Transistor Package [SOT-23]

Chinese version:CDG601

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CBMG601AST6	-40℃~85℃	SOT23-6	Tape and Reel, 3000
CBMG601AMS8	-40℃~85℃	MSOP-8	Tape and Reel, 3000

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.10.23	Initial version	Regular update	WW	LYL	