



CD12AD01_CD12AD02

Weak Signal Acquisition ASIC Chip

Version: Rev 1.0.0 Date: 2025-11-13

Features ■

- CD ADC™ Micro-Signal Direct
- High-Precision Analog-to-Digital
- Output LSB as low as 2.5μV
- Controllable Input Impedance:
- Full-Scale Range (FSR): 82mV
- Flexible Sampling Rate Control
 - High-Performance Mode:
 - High-Speed Mode: Up to 8kHz
- Signal-to-Noise Ratio (SNR): Up to
- Common-Mode Rejection Ratio
- Equivalent Differential Input
Capacitance: <1.5pF
- Dual-Channel Continuous Operating
- I2C Communication Interface for
- SDA Pin Multiplexable as Interrupt
- Conversion Complete Interrupt and
- Single-Wire Transmission Interface
- Built-in Multiple Digital Filters
 - Programmable Low-Pass Filter
 - Programmable High-Pass Filter
- Ultra-Small DFN-8 (2mm * 2mm)
- Die Form Available
- Wide Operating Temperature Range:
- Wide Operating Voltage Range:

Application ■

- Pyroelectric Gas Detector
- Pyroelectric Flame Detector
- Instruments, sensors, and other devices that require detection of microvolt-to-millivolt (μV~mV) level weak signals and demand gigaohm-to-teraohm (GΩ~TΩ) level high input impedance
- Low-Side Current Sensing

Description

The CD12AD0X series is a highly integrated ASIC for weak signal acquisition, corely breaking through the "impossible triangle" dilemma of traditional discrete component solutions — balancing high performance, low power consumption, and design simplicity. Leveraging the proprietary CD ADC™ technology, it enables the shortest path and purest signal chain from sensor to digital domain without requiring an additional PGA (Programmable Gain Amplifier). The single-chip integrated design simplifies the complex analog front-end (AFE) to a user-friendly digital interface. It not only delivers a single-chip solution for femtoampere (fA)-level signal processing at the pyroelectric detector front-end but also offers customers three core advantages: high performance, low power consumption, and cost-effectiveness, facilitating shorter R&D cycles and accelerated product time-to-market.

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Block Diagram

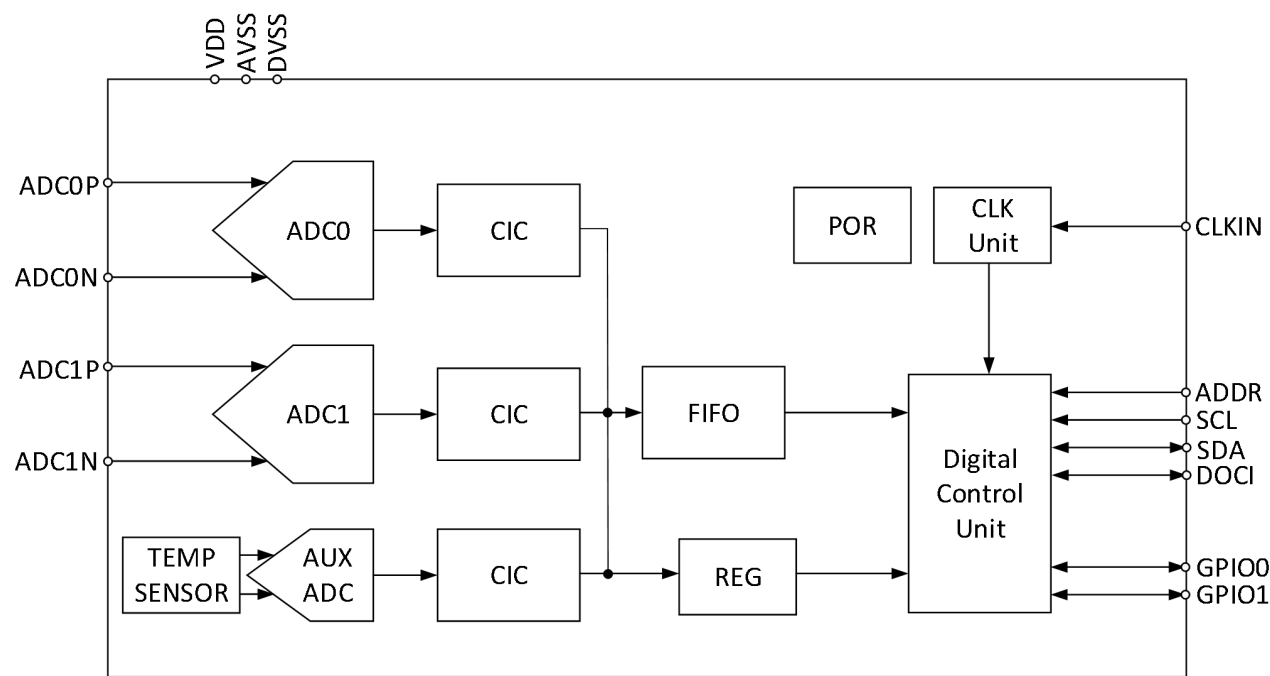


Figure 1 Functional Block Diagram

Pin Configuration and Function Descriptions

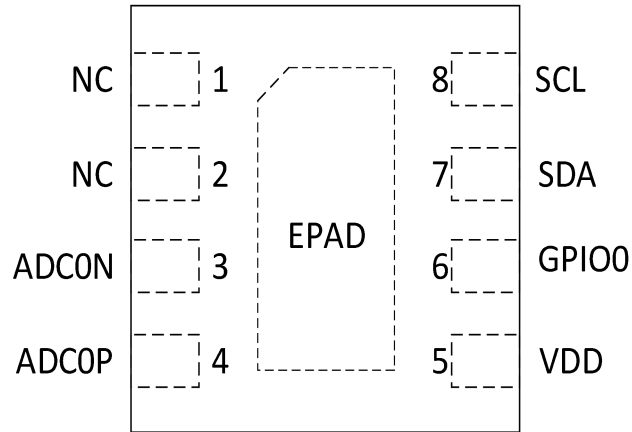


Figure 2 CD12AD01D Pin Configuration
(A1)(Bottom View)

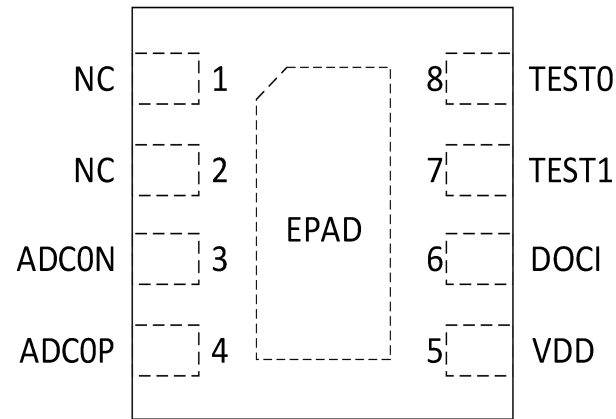


Figure 3 CD12AD01B Pin Configuration
(B1)(Bottom View)

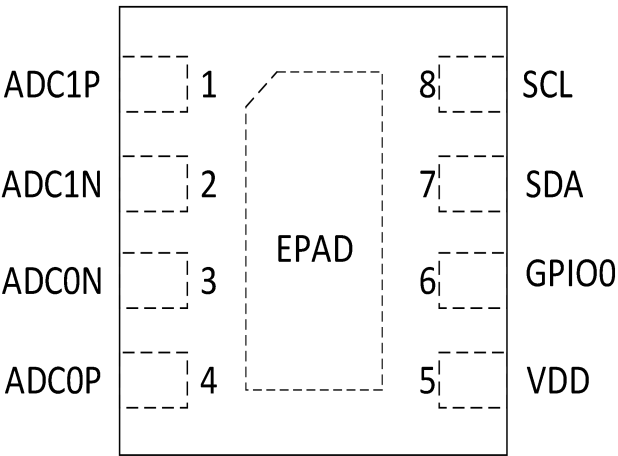


Figure 4 CD12AD02D Pin Configuration
(A2)(Bottom View)

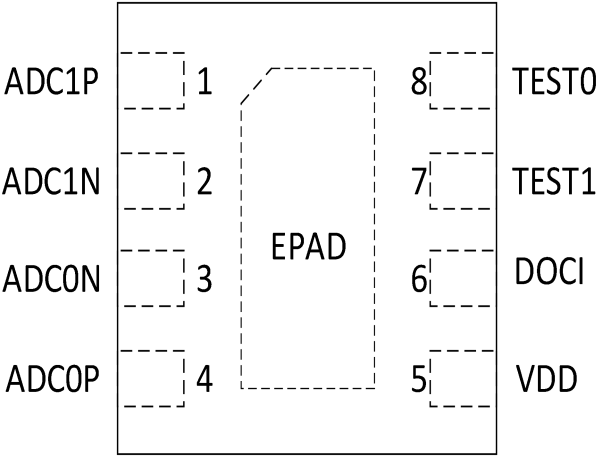


Figure 5 CD12AD02B Pin Configuration
(B2)(Bottom View)

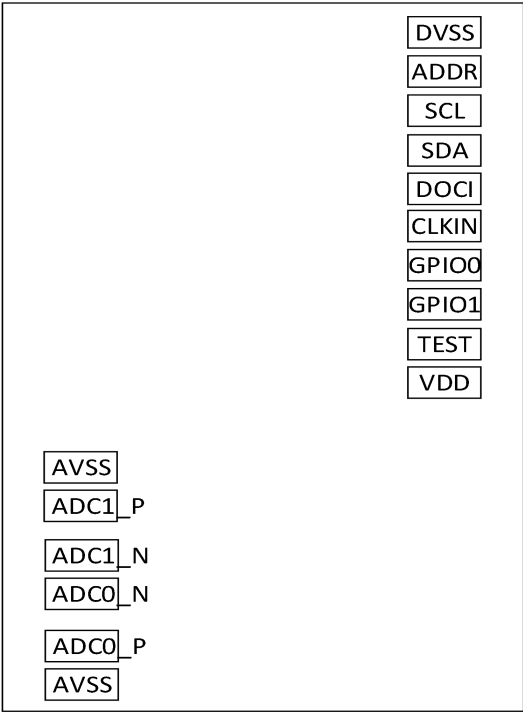


Figure 6 CD12AD01/02-DIE Pin Configuration (Die)(Bottom View)

Pin No. (Die)	Pin No. (A1)	Pin No. (A2)	Pin No. (B1)	Pin No. (B2)	Type	Mnemonic	Description
A1	--	--	--	--	S	AVSS	Analog Ground
A2	--	1	--	1	AI	ADC1P	ADC1 Input+
A3	--	2	--	2	AI	ADC1N	ADC1 Input-
A4	3	3	3	3	AI	ADC0N	ADC0 Input-
A5	4	4	4	4	AI	ADC0P	ADC0 Input+

A6	--	--	--	--	S	AVSS	Analog Ground
C1	--	--	--	--	S	DVSS	Digital Ground
C2	--	--	--	--	DI	ADDR	I ² C Slave Address Selection
C3	8	8	--	--	DI	SCL	I2C SCL
C4	7	7	--	--	DIO	SDA	I2C SDA
--	--	--	8	8	NC	TEST0	Leave Floating
--	--	--	7	7	NC	TEST1	Leave Floating
C5	--	--	6	6	DIO	DOCI	Single-Wire Transmission Interface
C6	--	--	--	--	DI	CLKIN	External Clock Input
C7	6	6	--	--	DIO	GPIO0	User Interface I/O" (I/O=Input/Output) 0
C8	--	--	--	--	DIO	GPIO1	User Interface I/O" (I/O=Input/Output) 1
C9	--	--	--	--	NC	TEST	Leave Floating
C10	5	5	5	5	S	VDD	Supply
--	EPAD	EPAD	EPAD	EPAD	S	VSS	Ground (Analog and Digital Ground Combined)

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply	VDD	-0.3	--	3.6	V	VDD to VSS
ADC Input Voltage	V _{ADC0P/ADC0N/ADC1P/ADC1N}	-0.6	--	0.6	V	Common Mode to VSS
Storage Temperature	T _S	-45	--	125	°C	
Operating Temperature	T _C	-40	--	85	°C	
HBM	ESD _{HBM}	1000	--	--	V	ADC0P/ADC0N/ADC1P /ADC1N
		4000	--	--	V	All Other IO
CDM	ESD _{CDM}	500	--	--	V	ADC0P/ADC0N/ADC1P /ADC1N
		500	--	--	V	All Other IO

Specifications

Unless otherwise specified, all characteristic values are derived under the conditions of $T_A=25^{\circ}\text{C}$ and $2.4\text{V}\leq\text{VDD}\leq 5.5\text{V}$.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply						
Operating Voltage	VDD	2.2	--	3.6	V	VDD to VSS
Operating Current	I _{VDD}	--	2	--	μA	Standby Mode
		--	60	--		1ksps Dual-Channel Continuous Sampling Mode
		--	40	--		1ksps Single-Channel Continuous Sampling Mode
		--	40	--		500sps Dual-Channel Continuous Sampling Mode
		--	30	--		500sps Single-Channel Continuous Sampling Mode
		--	9	--		1ksps Window Sampling Mode
All test conditions for the Analog Input are based on the default configuration, with a data rate of 1ksps and a full-scale range (FSR) of 82mV.						
ADC Input Full-Scale Voltage	V _{ADC0P/ADC0N/ADC1P/ADC1N}	-82	--	82	mV	Differential
Adjustable Range of Equivalent Input Resistance	R _{in_eq}	10G	--	1.28T	Ohm	
Maximum Signal-to-Noise Ratio (SNR)	SNR _{max}	--	84	--	dB	
Common-Mode Voltage Range (CMVR)	CMVR	0	--	150	mV	T _{MIN} ≤T _A ≤T _{MAX}
ADC Effective Number of Bits (ENOB)	ENOB-ADC0/ENOB-ADC1	--	14	--	bits	
Second Harmonic	2 nd HD	60	--	--	dB	

Suppression						
Third Harmonic Suppression	3 rd HD	70	--	--	dB	
Common-Mode Rejection Ratio (CMRR) (0V Input Differential DC Voltage)	CMRR (0Vos)	110	--	--	dB	
Common-Mode Rejection Ratio (CMRR) (40mV Input Differential DC Voltage)	CMRR (40mVos)	91	--	--	dB	
Power Supply Rejection Ratio (PSRR) (0V Input Differential DC Voltage)	PSRR(0Vos)	120	--	--	dB	3.3V Power Supply Ripple Rejection
Power Supply Rejection Ratio (PSRR) (38mV Input Differential DC Voltage)	PSRR(38mVos)	81	--	--	dB	3.3V Power Supply Ripple Rejection
Channel Isolation	CH ISO	120	--	--	dB	
I2C Communication						
Frequency	FSCL	--	--	1000	Kbps	
Bus Load	Cload	--	--	30	pF	
External Pull-Up Resistor	REPU	800	--	--	Ω	
Digital Inputs (GPIO0/GPIO1)						
Input Voltage Range	VDI	0	--	VDD	V	
Schmitt Trigger Low-to-High Threshold	VT+	--	2.0	--	V	VDD = 3.3V
Schmitt Trigger High-to-Low Threshold	VT-	--	1.3	--	V	VDD = 3.3V
Internal Pull-Up Resistor	RPU	39	63	109	KΩ	
Digital Outputs						
Output Low Level (VOL)	VOL	--	--	0.4	V	VDD = 3.3V
Output High Level (VOH)	VOH	2.4	--	--		VDD = 3.3V
Low-Level Output Current (IOL)	IOL	9.4	14.1	--	mA	VOL = Maximum Value, IO_DS = 0
		18.8	28.1	--		VOL = Maximum Value, IO_DS = 1
High-Level Output Current (IOH)	IOH	7.0	9.3	--	mA	VOH = Minimum Value, IO_DS = 0
		13.9	18.6	--		VOH = Minimum Value,

						IO_DS = 1
DOCI Interface						
Schmitt Trigger Low-to-High Threshold	V_{T+}	--	2.0	--	V	VDD = 3.3V
Schmitt Trigger High-to-Low Threshold	V_{T-}	--	1.3	--	V	VDD = 3.3V
Pull-Down Current	I_{PD}	--	41.1	--	μA	
Pull-Up Current	I_{PU}	--	40.7	--	μA	
Input Capacitance	C_{IN}	--	5	--	pF	
DOCI Interface Setup Time	t_s	0	--	--	μs	
Data Clock Low Time	t_L	3	--	--	μs	
Data Clock High Time	t_H	3	--	--	μs	
Data Bit Stability Time	t_{bit}	1	--	--	μs	
Serial Interface Interrupt Time	T_{REP}	128	--	1024	ADC Sampling Clock	The 1M clock is divided by CLK_DIV[1:0] to serve as the ADC sampling clock.

(1) Typical values are for estimation only and not definitive.

(2) Unless otherwise specified, the maximum/minimum values in the data sheet are determined by testing.

(3) Typical values represent the most probable parameter specifications at $T_A = 25^\circ C$ and recommended operating conditions, and are not guaranteed.

Functional Description

The CD12AD02 product consists of two main ADCs (ADC0, ADC1), two FIFO regions (ADC0 FIFO, ADC1 FIFO), and one temperature-measuring ADC. The system timing clock adopts an 8-fold division of either 32kHz or 256kHz. Among them, ADC0 and ADC1 are enabled by default and can be turned on/off via the registers ADC0_DIS and ADC1_DIS.

Details are as follows:

CD12AD01D: ADC0 enabled by default (ADC0_DIS=0, ADC1_DIS=1), with GPIO0 output;

CD12AD02D: Both ADC0 and ADC1 enabled by default (ADC0_DIS=0, ADC1_DIS=0, configurable by user), with GPIO0 output;

CD12AD01B: ADC0 enabled by default (ADC0_DIS=0, ADC1_DIS=1), with DOCI output;

CD12AD02B: Both ADC0 and ADC1 enabled by default (ADC0_DIS=0, ADC1_DIS=0, configurable by user), with DOCI output.

Package Outline Dimensions

Die

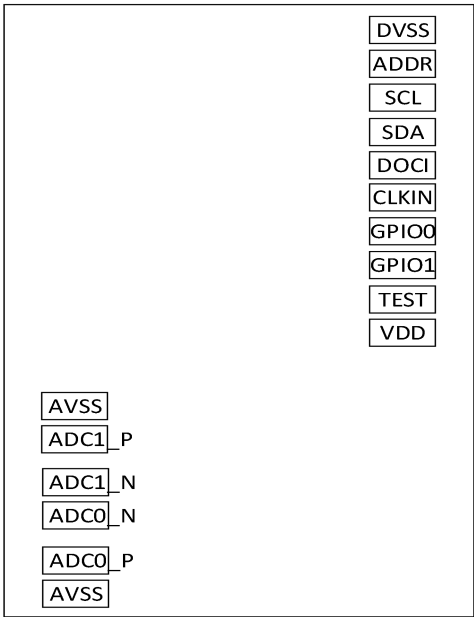


Figure 7: Die Dimensions Drawing
DIE SIZE: 945*1390(μm)

Number	Symbol	X (μm)	Y (μm)	PAD SIZE (μm)
1	AVSS	53.500	101.000	60x60
2	ADC0_P	53.500	181.000	60x60
3	ADC0_N	53.500	289.320	60x60
4	ADC1_N	53.500	369.320	60x60
5	ADC1_P	53.500	477.640	60x60

6	AVSS	53.500	557.640	60x60
7	DVSS	888.000	1328.000	60x60
8	ADDR	888.000	1248.000	60x60
9	SCL	888.000	1168.000	60x60
10	SDA	888.000	1088.000	60x60
11	DOCI	888.000	1008.000	60x60
12	CLKIN	888.000	928.000	60x60
13	GPIO0	888.000	848.000	60x60
14	GPIO1	888.000	768.000	60x60
15	TEST	888.000	688.000	60x60
16	VDD	888.000	608.000	60x60

DFN-8

UNIT:mm

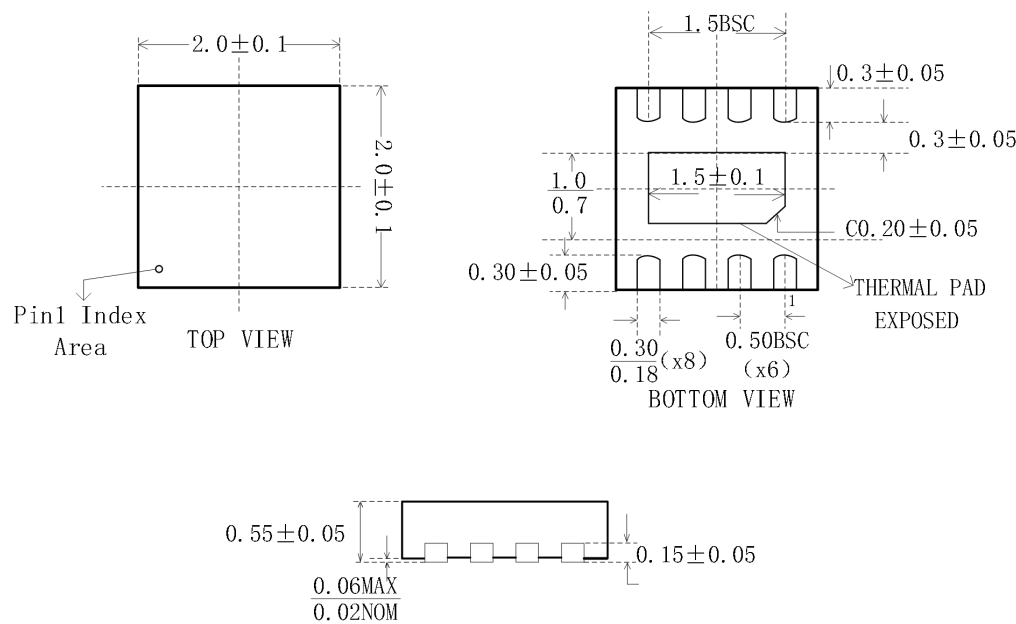


Figure 8: DFN-8 Package Dimensions Drawing

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	Note	PACKAGE OPTION
CD12AD01-DIE	-40℃~85℃	Die	Single Channel	
CD12AD01D	-40℃~85℃	DFN-8	Single Channel, GPIO0 Output	
CD12AD01B	-40℃~85℃	DFN-8	Single Channel, DOCI Output	
CD12AD02-DIE	-40℃~85℃	Die	Dual Channel	
CD12AD02D	-40℃~85℃	DFN-8	Dual Channel, GPIO0 Output	
CD12AD02B	-40℃~85℃	DFN-8	Dual Channel, DOCI Output.	

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.11.13	Initial version	Initial Version	WW	LYL	