CoreadDvices
承芯微电子

CD94AD34

12-Bit, 370 MSPS/500 MSPS, 1.8 V Analog-to-Digital Converter

Version: Rev 1.0.0 Date: 2025-9-10

Features

- Resolution 12 Bits
- Conversion Rate 500MSPS
- SFDR: >65dB
- Programmable (nominal) input voltage
- PIN compatible with AD9434 series

Application

- Receiver
- Radar and satellite subsystems
- Linearization of power amplifiers
- Communication testing equipment
- Wireless and broadband communication

Description

CD94AD34 is a 12 bit, single-chip sampling analog-to-digital converter (ADC) designed specifically for high performance, low power consumption, and ease of use. Its conversion rate can reach 500 MSPS, and it has excellent dynamic performance in broadband applications. All required functions are integrated on the chip, including a sampling and holding amplifier (SHA) and an on chip reference voltage source, to provide a complete signal conversion solution. The V_{REF} pin can be used to change the internal reference voltage or accept a reference voltage from an external source (the external reference mode needs to be enabled through the SPI port).

This ADC requires a 1.8 V analog power supply and a differential clock to maintain excellent overall ADC performance. The digital output is compatible with LVDS (ANSI-644), and the data format is binary complement, Gray code or offset binary. There is a data output clock to ensure that the corresponding data output has the correct timing.

This product is manufactured using SiGe BiCMOS technology, with 56 lead plastic packaging (QFN56), which can effectively replace ADI's AD9434BCPZ-500 in the United States.

Contents

Functional Block Diagram

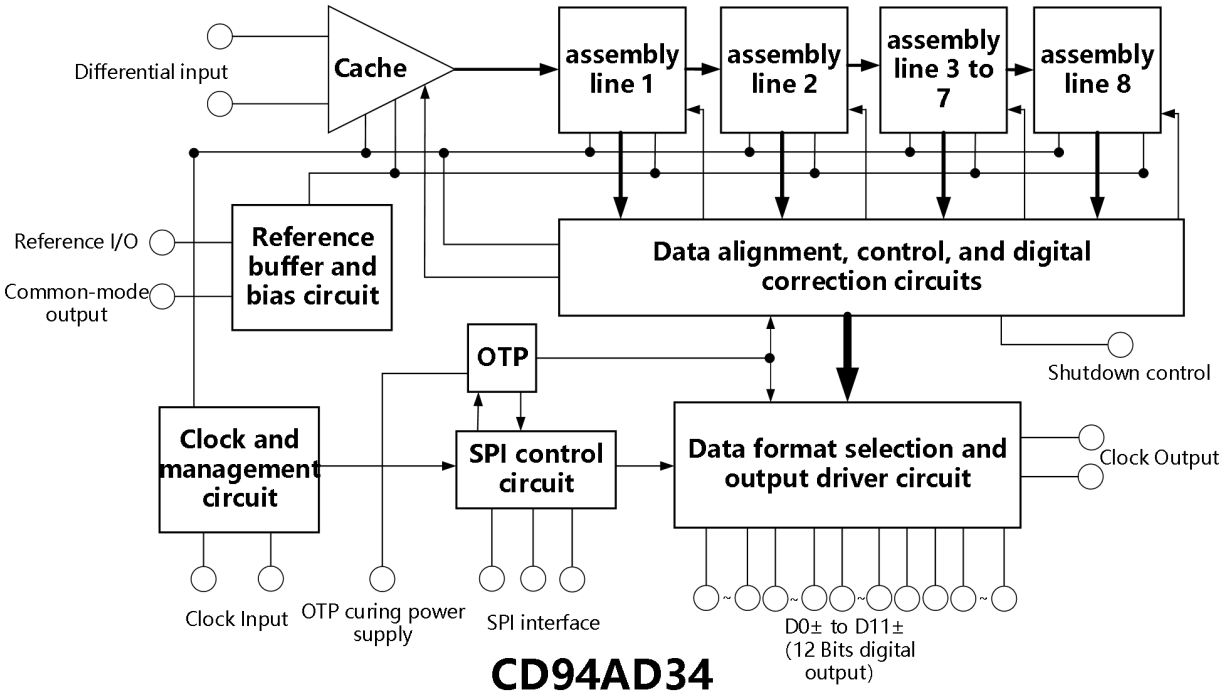

Figure 1. Functional block diagram

Pin Configurations

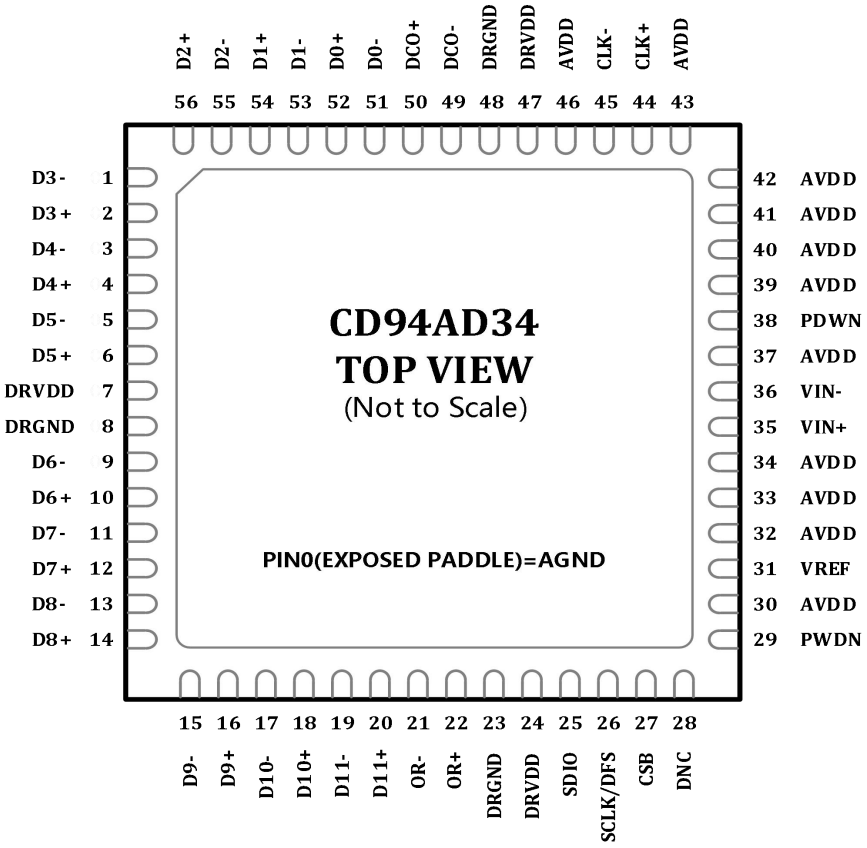

Figure 2. Pin Configuration

ENO	REFIN	Describe of reference voltage mode
0	AGND	Analog Ground. The exposed paddle must be soldered to a ground plane.
1	D3-	D3 Complement Output.
2	D3+	D3 True Output.
3	D4-	D4 Complement Output.
4	D4+	D4 True Output.
5	D5-	D5 Complement Output.
6	D5+	D5 True Output.
7,24,47	DRVDD	1.8 V Digital Output Supply.
8,23,48	DRGND	Digital Output Ground.
9	D6-	D6 Complement Output.
10	D6+	D6 True Output.
11	D7-	D7 Complement Output.
12	D7+	D7 True Output.
13	D8-	D8 Complement Output.

14	D8+	D8 True Output.
15	D9-	D9 Complement Output.
16	D9+	D9 True Output.
17	D10-	D10 Complement Output.
18	D10+	D10 True Output.
19	D11-	D11 Complement Output (MSB).
20	D11+	D11 True Output (MSB).
21	OR-	Overrange Complement Output.
22	OR+	Overrange True Output.
25	SDIO	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode).
26	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode)/Data Format Select (External Pin Mode).
27	CSB	Serial Port Chip Select (Active Low).
28	DNC	Do Not Connect. Do not connect to this pin. This pin should be left floating.
29	PWDN	Chip Power-Down.
30,32 to 34,37 to 39,41 to 43,46	AVDD	1.8 V Analog Supply.
35	VIN+	Analog Input—True.
36	VIN-	Analog Input—Complement.
40	CML	Common-Mode Output. Enabled through the SPI, this pin provides a reference for the optimized internal bias voltage for VIN+/VIN−.
44	CLK+	Clock Input—True.
45	CLK-	Clock Input—Complement.
49	DCO−	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
51	D0-	D0 Complement Output.
52	D0+	D0 True Output.
53	D1-	D1 Complement Output.
54	D1+	D1 True Output.
55	D2-	D2 Complement Output.
56	D2+	D2 True Output.

Recommended Operation Conditions

- Operating Frequency (f_{CLK}): ≤500MHz
- Analog power supply voltage(V_{CC}): 1.75V~1.9V
- Digital power supply voltage(V_{DD}): 1.75V~1.9V
- Analog input common mode voltage(V_{IC}): 1.6V~1.8V
- Operating temperature(T_A): -40℃~85℃
- Input signal amplitude range (peak to peak): ($V_{IN(P-P)}$≤1.5V

Absolute Maximum Ratings

- Analog power supply voltage(V_{CC}): 2V
- Digital power supply voltage(V_{DD}): 2V
- Storage temperature T_S: - 65 ℃~ 150 ℃
- Junction temperature T_J: 175 ℃
- Lead Temperature (Soldering, 10 sec): 300 ℃

Electrical Characteristics

V_{CC}=1.8V，V_{DD}=1.8V，GND=GND_D=0V，$V_{IN(P-P)}$≤1.5V，-40℃≤T_A≤85℃, unless otherwise noted.

Table1.

parameter name	symbol	condition	MIN	TYP	MAX	Unit
Resolution	RES	--	12			bits
Offset Error	E_O	--	-5.0	--	5.0	mV
Gain error	E_G	--	-9	--	9	%FS
Differential linearity error	E_{DL}	--	-1.5	--	1.5	LSB
Integral Linearity Error	E_L	--	-4.5	--	4.5	LSB
Internal reference voltage	V_{REF}	--	0.7	--	0.8	LSB
Power supply current [a]	I	--	--	--	500	mA
LVDS differential output voltage	V_{OD}	--	200	--	500	mV
LVDS common mode output voltage	V_{OS}	--	1.0	--	1.45	V

power dissipation	P_D	--	--	--	900	mW
Standby power	P_{SDB}	--	--	--	60	mW
Powerdown consumption	P_{PDN}	--	--	--	12	mW
Signal to Noise Ratio	SNR	f_{CLK}=500MHz,T_A=25℃,f_{IN}=30.3MHz	63	--	--	dBFS
		f_{CLK}=500MHz,T_A=25℃,f_{IN}=450.3MHz	61	--	--	
		f_{CLK}=500MHz,T_A=-40℃~85℃,f_{IN}=30.3MHz	58	--	--	
Signal-to-noise distortion ratio	SINAD	f_{CLK}=500MHz,T_A=25℃,f_{IN}=30.3MHz	62	--	--	dBFS
		f_{CLK}=500MHz,T_A=25℃,f_{IN}=450.3MHz	60	--	--	
		f_{CLK}=500MHz,T_A=-40℃~85℃,f_{IN}=30.3MHz	57	--	--	
Effective number of bits	ENOB	f_{CLK}=500MHz,T_A=25℃,f_{IN}=30.3MHz	10.0	--	--	bits
		f_{CLK}=500MHz,T_A=25℃,f_{IN}=450.3MHz	9.5	--	--	
		f_{CLK}=500MHz,T_A=-40℃~85℃,f_{IN}=30.3MHz	9.2	--	--	
Spurious free dynamic range	SFDR	f_{CLK}=500MHz,T_A=25℃,f_{IN}=30.3MHz	72	--	--	dBFS
		f_{CLK}=500MHz,T_A=25℃,f_{IN}=450.3MHz	66	--	--	
		f_{CLK}=500MHz,T_A=-40℃~85℃,f_{IN}=30.3MHz	65	--	--	
Data propagation delay	t_{PD}	--	--	--	10	ns
Note [a]:The power supply current is the sum of analog power supply current (I_{CC}) and digital power supply current (I_{DD}).						

Main Characteristic of Curves

1. DNL and INL test results

Test conditions: Sampling rate: f_{CLK}=500MHz; Input signal frequency f_{IN}=30.3MHz; Test result:

DNL: -0.51/+0.49 LSB

INL: -1.1/+1.1 LSB

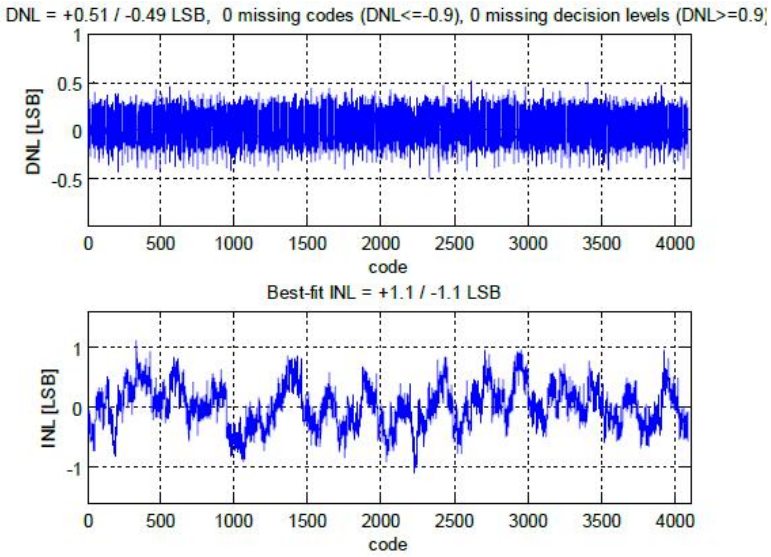

Figure 3. DNL and INL test results

2. Dynamic parameter test results

Test conditions: Sampling rate: f_{CLK}=499.999970304MHz;

Input signal frequency f_{IN}=30.28867830MHz;

Test results: SFDR=79.23dBFS;$HD_{2,\ 3nd}$=78.89dBFS;HD_{4nd}=81.48dBFS;SNR=65.6dBFS;

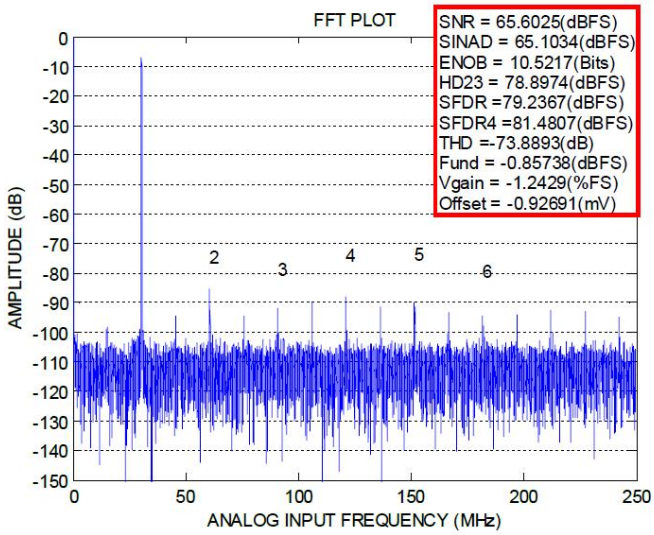

Figure 4. Dynamic Indicator Test Results

3. Curve of SNR and SFDR with sampling frequency

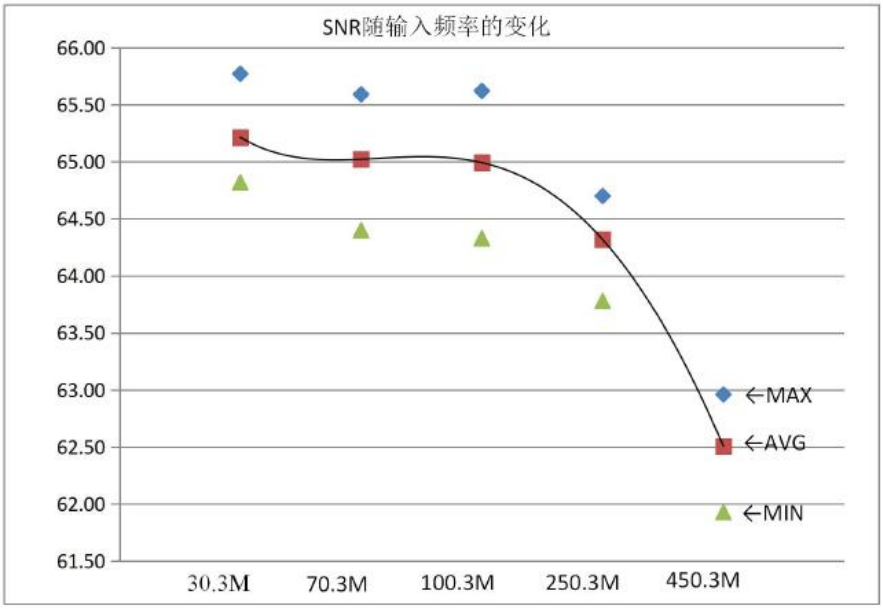

Figure 5. SNR variation curve with sampling frequency

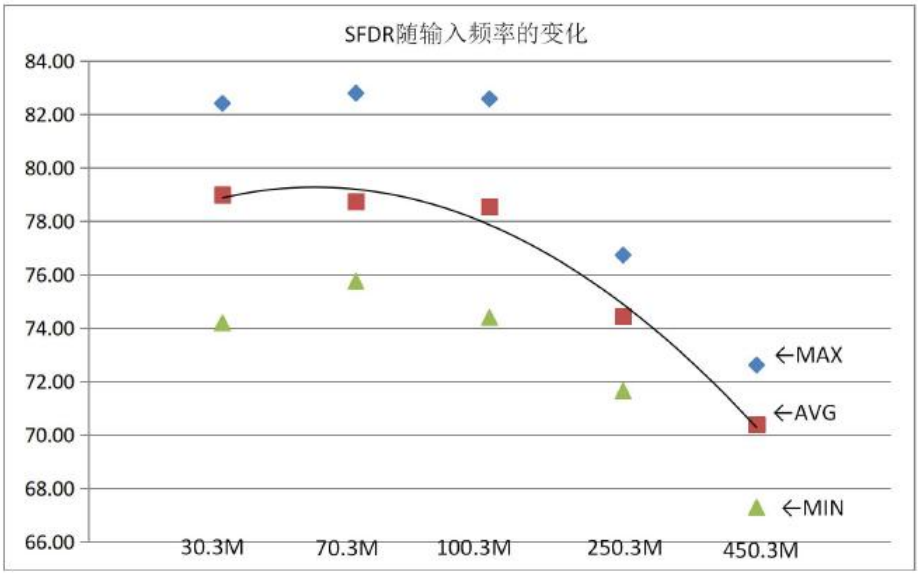

Figure 6. SFDR variation curve with sampling frequency

Typical Application Circuit

1. Analog input circuit

When driving the CD94AD34 through differential input configuration, the optimal performance of the chip can be achieved. In baseband applications, the AD8138 differential driver can provide excellent performance and flexible interfaces for ADC. The output common mode voltage of AD8138 can be easily set to AVDD/2+0.5 V, and this driver can be configured as Sallen Key filter topology circuit structure, so as to Bandwidth throttling of the input signal.

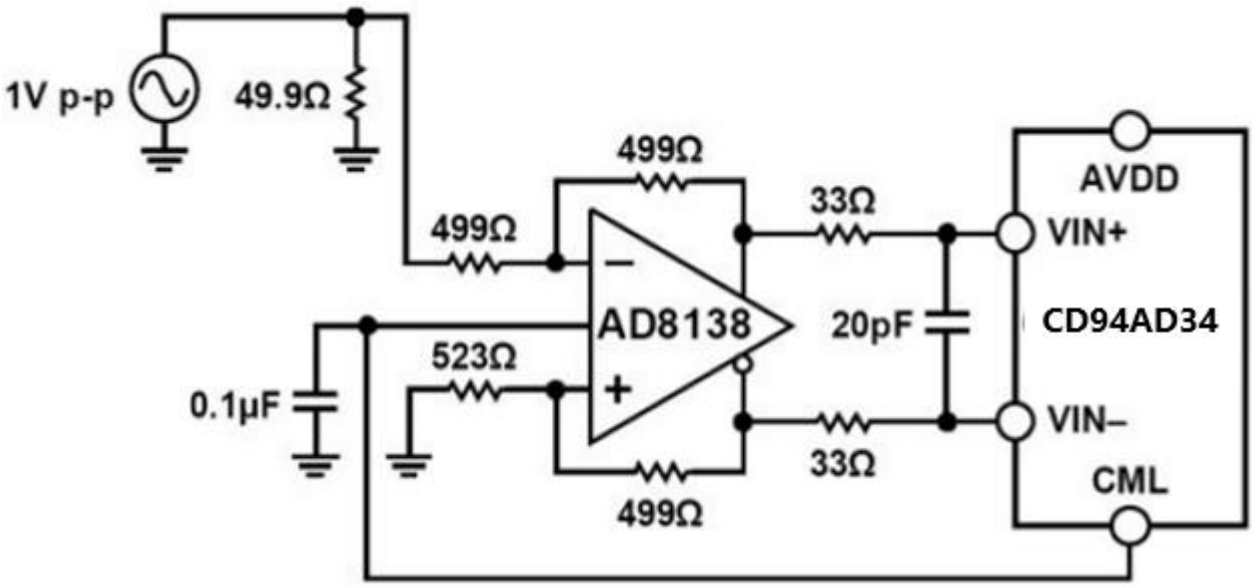

Figure 7. Differential Input Configuration Using AD8138

When the input frequency is in the second or higher Nyquist region, the noise performance of most amplifiers cannot meet the requirements to achieve the true SNR performance of CD94AD34. This phenomenon is particularly evident in intermediate frequency undersampling applications with frequencies ranging from 70 MHz to 100 MHz. For such applications, the recommended input configuration is differential double balun coupling. When selecting a

transformer, it is necessary to consider its signal characteristics. Most RF transformers experience saturation when operating at frequencies below a few megahertz; Excessive signal power can also cause saturation of the core magnetic core, leading to distortion.

In any configuration, the parallel capacitance value C depends on the input frequency and source impedance, and it may be necessary to reduce the capacitance or remove the parallel capacitance.

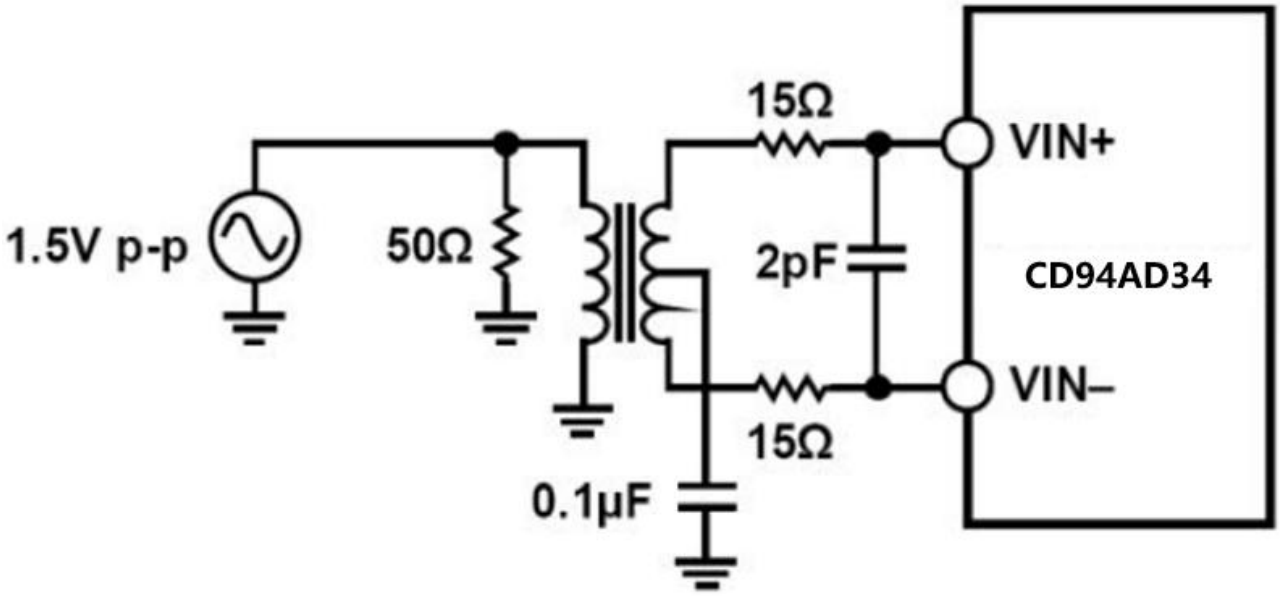

Figure 8 Differential Transformer Coupling Configuration

When the frequency is within the second Nyquist region, in addition to coupling the input with a transformer, an AD8352 differential driver can also be used, as shown in Figure 9.

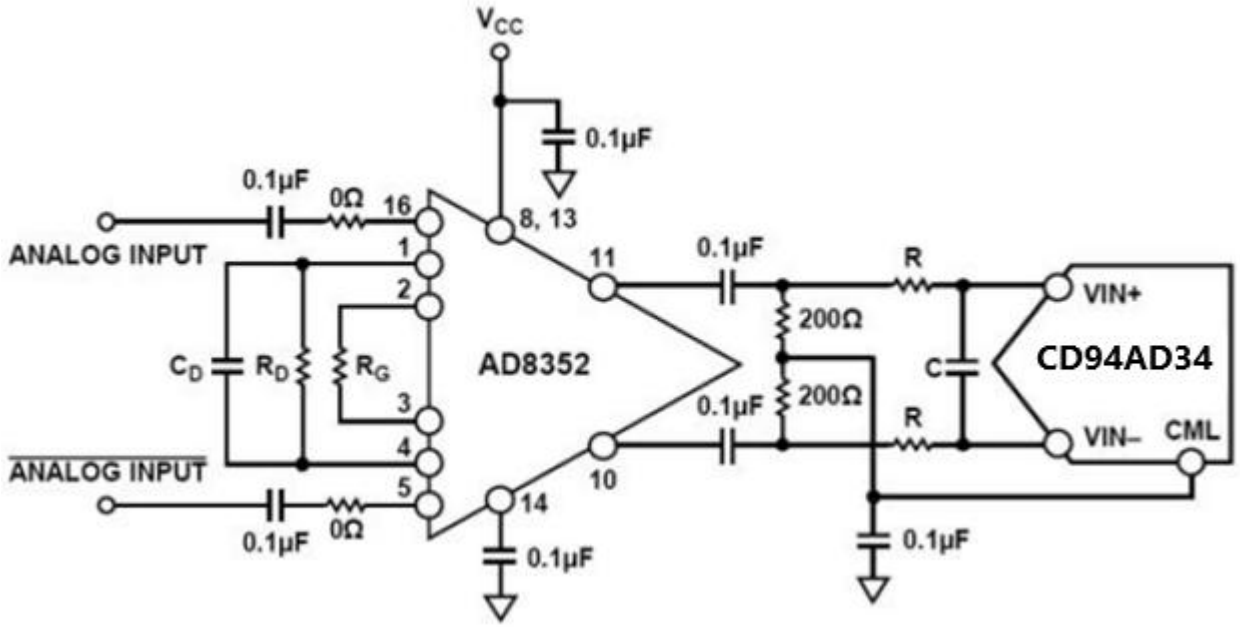

Figure 9. Differential Input Configuration Using AD8352

Clock input circuit

In order to fully utilize the performance of the chip, a differential signal should be used as the clock signal for the CD94AD34 sampling clock inputs (CLK+and CLK -). Usually, a transformer or two capacitors should be used to AC couple the signal to the CLK+pin and CLK - pin. The CLK+and CLK - pins have an internal bias of approximately 0.9 V and do not require external bias. If the clock signal is DC coupled, it is necessary to maintain the common mode voltage within the range of 0.9 V.

Figure 10 shows a preferred method for providing clock signals for CD94AD34. By using an RF transformer, the single ended signal of a low jitter clock source can be converted into a differential signal. The back to back Schottky diode connected across the transformer secondary can limit the clock signal input to CD94AD34 to approximately 0.8 V differential peak to peak. In this way, not only the fast rise and Fall time time of the signal can be reserved, but also the large

voltage swing of the clock can be prevented from feeding to other parts of the CD94AD34, which is very important for low jitter performance.

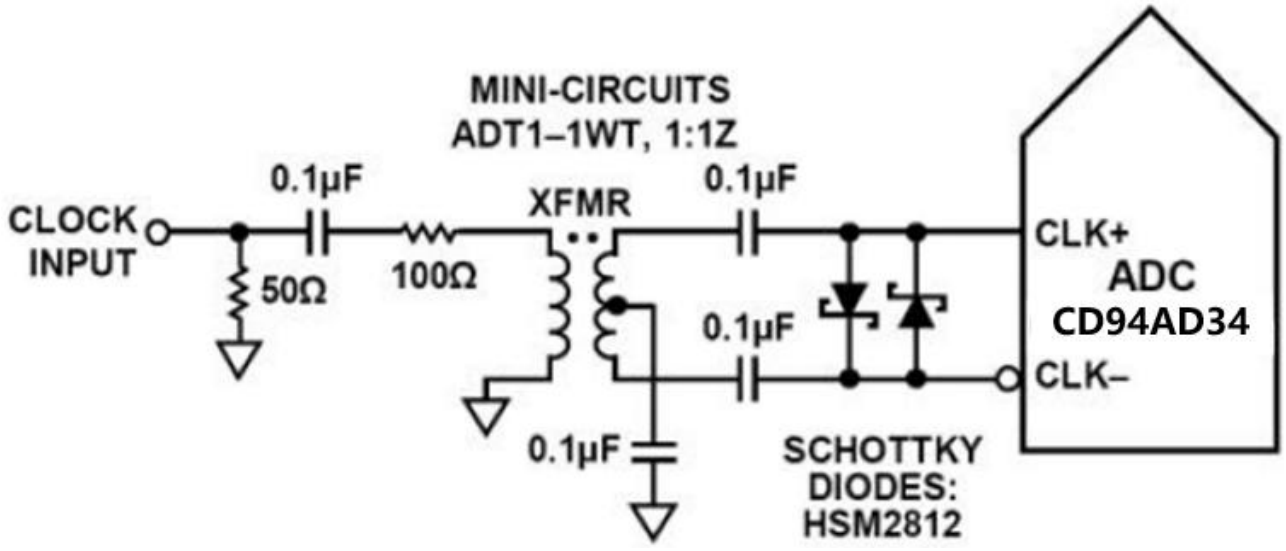

Figure 10. Transformer coupled differential clock configuration

If there is no low jitter clock source, another method is to AC couple the differential PECL signal and transmit it to the sampling clock input pin (as shown in Figure 11). The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 series clock drivers have excellent jitter performance.

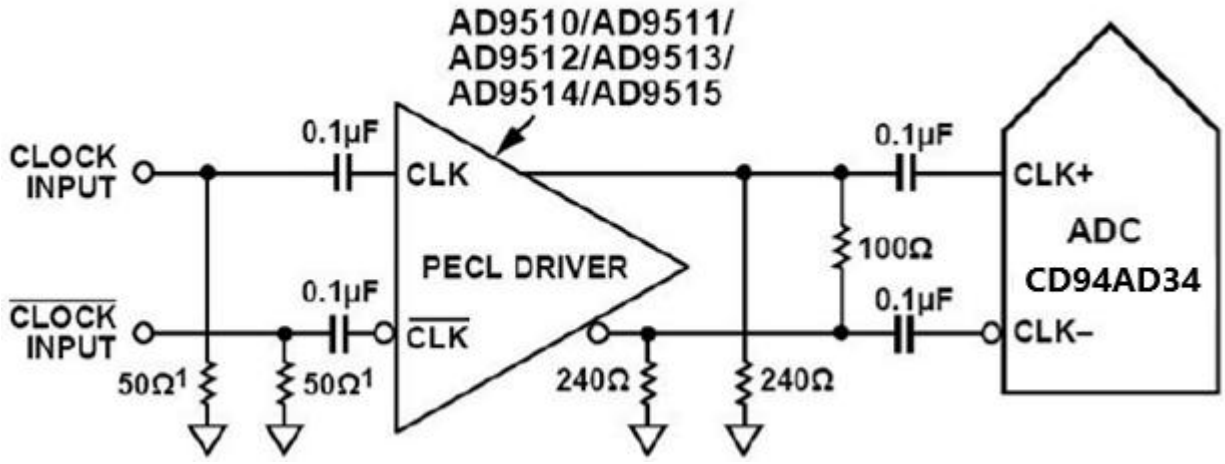

Figure 11. Differential PECL sampling clock

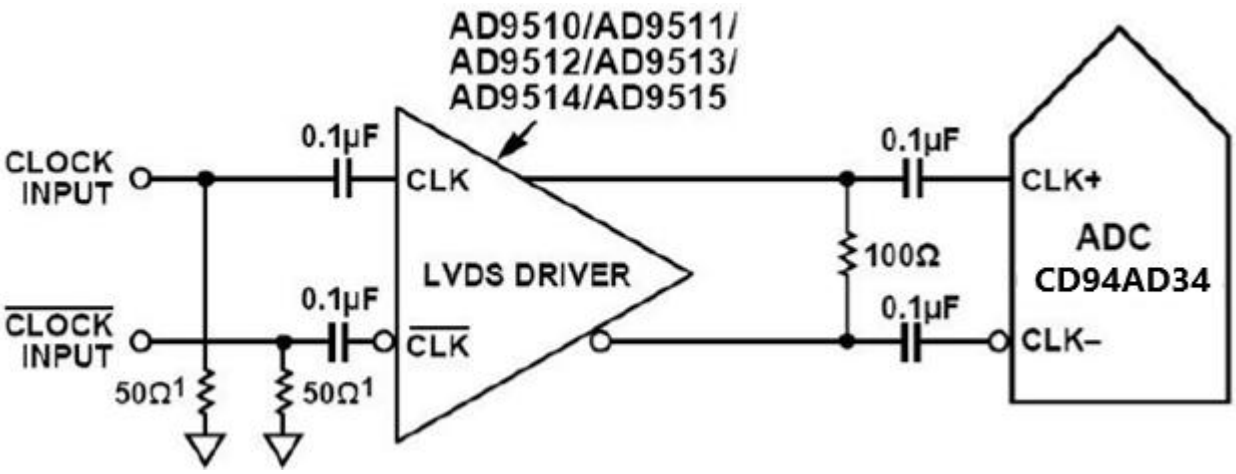

Figure 12. Differential LVDS sampling clock

In some applications, a single ended CMOS signal can be used to drive the sampling clock input. In such applications, the CLK+pin is directly driven by a CMOS gate circuit, while the CLK pin is bypassed to ground through a 0.1 F capacitor. When driving CLK+with a 1.8 V CMOS signal, a parallel biased CLK pin with a 0.1 F capacitor and a 39 k resistor is required (see Figure 13).

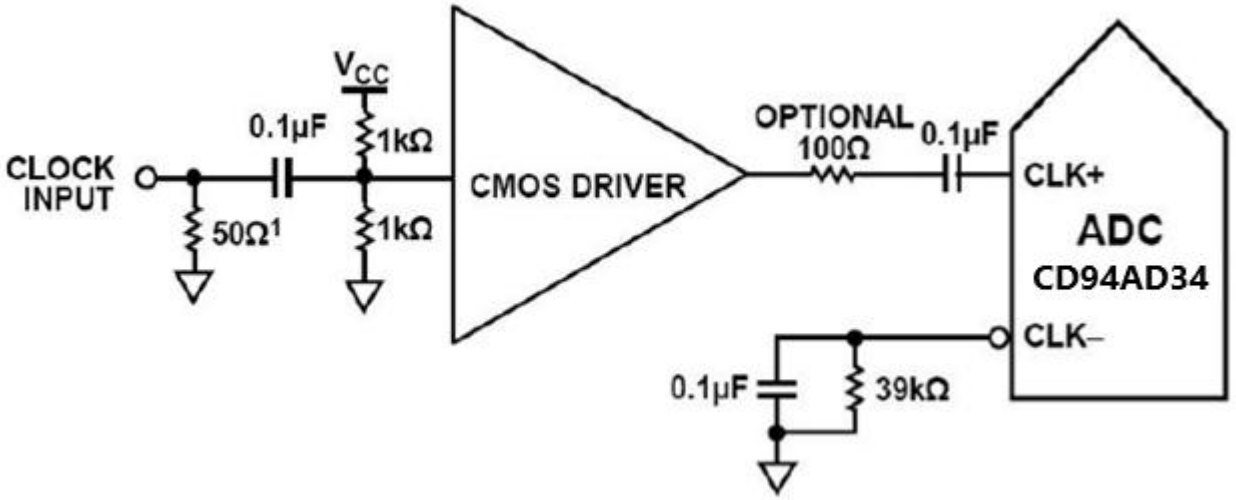

Figure 13. Single ended 1.8 V CMOS input clock

Digital Output

By default, the differential output data format of CD94AD34 complies with the ANSI-644 LVDS standard. The data format can be changed to a low-power, less signal selection, and format similar to the IEEE 1596.3 standard through SPI. This LVDS standard can further reduce the power consumption of the chip, approximately 39mW. For more relevant information, please refer to the overseas AD9434BCPZRL7-500 memory address function section. The current of the LVDS driver comes from within the chip, and the output current size of each output bit is generally set to 3.5 mA. Adding a 100 Ω terminal resistor to the input of the LVDS receiver will generate a 350 mV swing. The LVDS output data format of CD94AD34 is conducive to connecting with LVDS receivers in customized ASICs and FPGAs, and can have good switching performance in noisy environments. It is recommended to place a single point-to-point network topology with a terminal resistor of 100 Ω as close to the receiver as possible. Placing the receiver's terminal too far or with poor differential distribution lines will result in timing errors. It is recommended that the wiring length should not exceed 24 inches, and the differential output wiring should be placed together and of the same length.

Relationship table between output code and analog input

Input	Conditions	Offset binary mode, D11 to D0	Binary complement mode, D11 to D0	OR±
V_{IN+} to V_{IN-}	< −0.75-0.5 LSB	0000 0000 0000	1000 0000 0000	1
V_{IN+} to V_{IN-}	= −0.75	0000 0000 0000	1000 0000 0000	0
V_{IN+} to V_{IN-}	= 0	1000 0000 0000	0000 0000 0000	0
V_{IN+} to V_{IN-}	= 0.75	1111 1111 1111	0111 1111 1111	0
V_{IN+} to V_{IN-}	> 0.75+0.5 LSB	1111 1111 1111	0111 1111 1111	1

Data output format

The default format for output data is offset binary.

The typical application circuit of this circuit is shown in the figure below. For detailed information, please refer to the product manual of AD9434BCPZ-500 abroad.

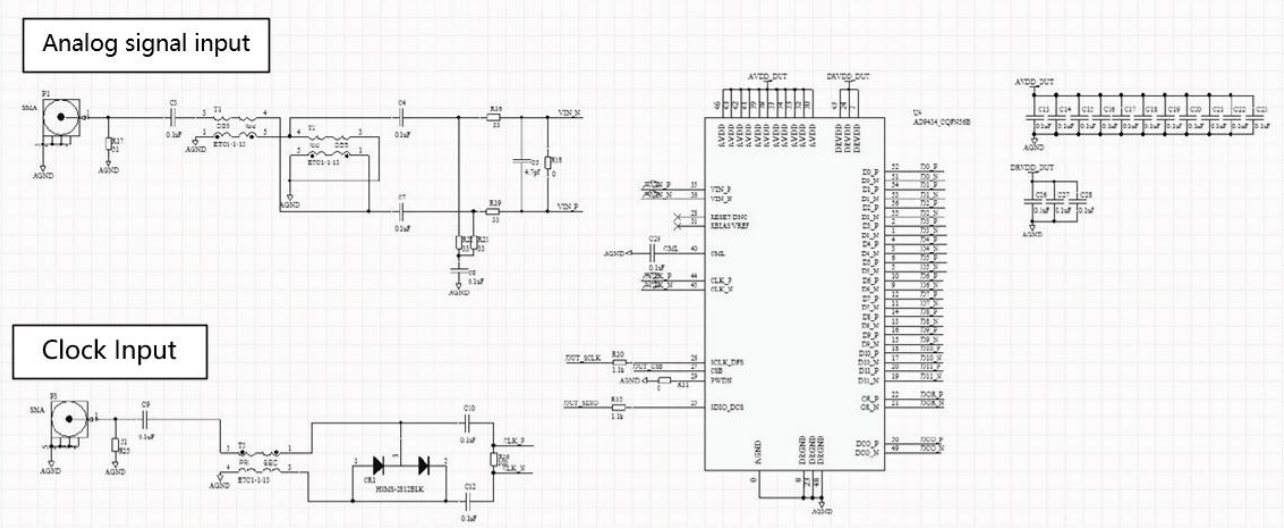

Figure 14. Typical Application Circuit

Notes

1. Product installation precautions:

(1).It is required that the application object circuit board has a complete and clean ground.

(2).It is required that the application object is a multi-layer wiring board and contains independent layers.

(3).It is required to separate the digital ground and analog ground of the application object circuit board as much as possible, and not place the digital line next to the analog line or under

the ADC.

(4).AVDD, DRVDD, and VCM should be connected to high-quality ceramic bypass capacitors, and the bypass capacitors should be as close to the pins as possible. The shorter and wider the connection between the pins and the bypass capacitors, the better.

2. Precautions for product use:

(1).Differential inputs should be as close and parallel as possible.

(2).The input wiring should be as short as possible to minimize parasitic capacitance and noise introduction.

(3).In order to achieve better heat dissipation and electrical performance, the bottom plate of the chip should be welded to a large ground end of the PCB board, in order to maximize the thermal performance of the package.

(4).It is important that the ground of the chip should be connected to the PCB board through as many channels and sufficient area as possible.

3. Precautions for product protection:

(1).Electrostatic charges can easily accumulate on the human body and testing equipment, and may discharge unnoticed. Although this product has a dedicated ESD protection circuit, permanent device damage may occur when encountering high-energy electrostatic discharge. Therefore, it is recommended to take appropriate ESD prevention measures to avoid device performance degradation or loss of function.

(2).Exceeding the absolute maximum rating may result in permanent damage to the device. This is only the maximum rated value and does not mean that the device can operate normally under

these conditions or any other conditions beyond those shown in this product manual. Long term operation under absolute maximum rated conditions can affect the reliability of the device.

4.Common faults and solutions

1.No signal output: Check if the power voltage, input signal, and clock are loaded correctly.

2.Overflow signal: check whether the benchmark works normally and whether the input signal amplitude is correct.

3.Unstable device operation: Check the power supply to ensure stable power voltage.

Package Outline Dimensions

QFN-56

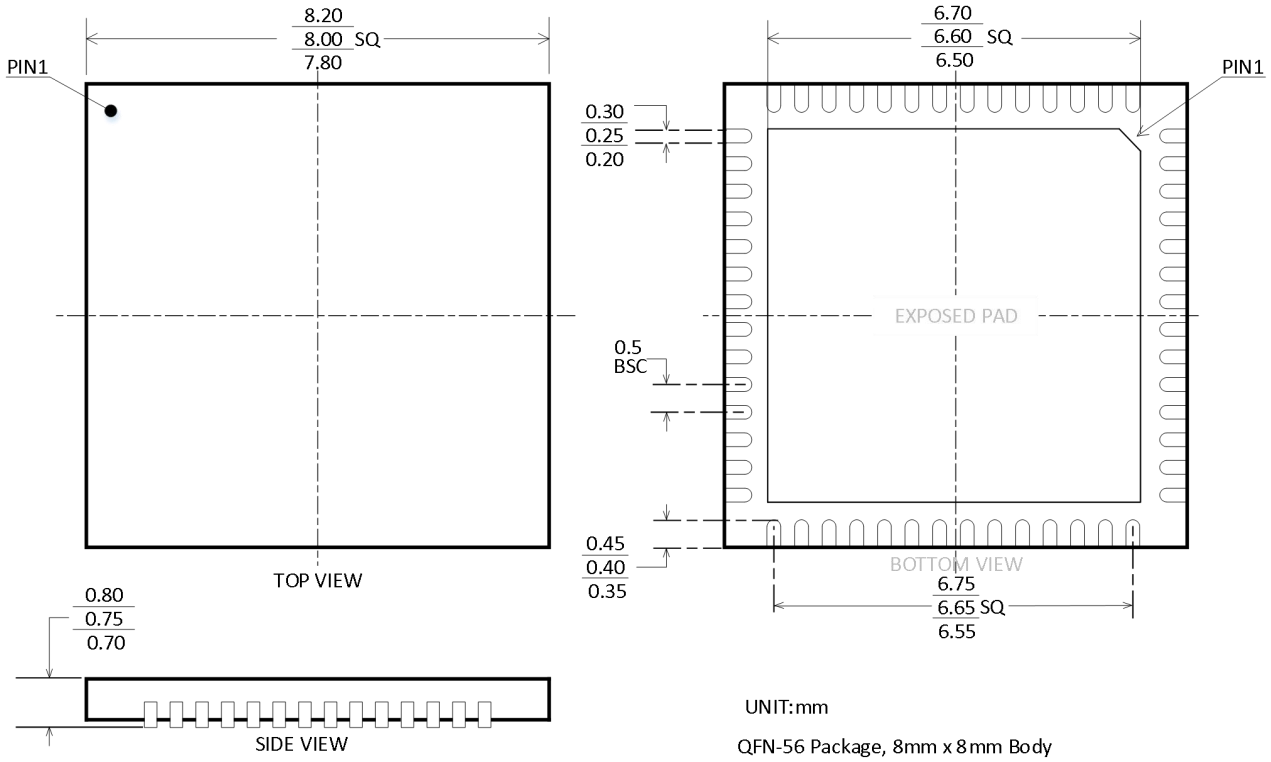

Figure 15. 56 Pin lead packaging (plastic packaging)
8mm×8mm，Dimensions shown in millimeters

Package/Ordering Information

MODEL	TEMPERATURE	PACKAGE DESCRIPTION	PACKAGE OPTION
CD94AD34-500	-40℃-85℃	QFN-56	Tray, 260
CD94AD34-370	-40℃-85℃	QFN-56	Tray, 260

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.9.10	Initial version	Regular update	WW	LYL	
V1.0	2025.9.10	Update QFN-56 POD	updates and upgrades	WW	LYL	